

## **Features**

- 8 Simultaneously Sampled Inputs
- Single 5V Analog Supply and 1.71-V to 5-V VDRIVE
- 16-Bit ADC with 500 kSPS on All Channels
- Bipolar Inputs Ranges: ±10 V, ±5 V
- High Analog Bandwidth: 200 kHz
- Analog Input Clamp Protection
- 1 MΩ Analog Input Impedance
- On-Chip Reference and Buffer
- On-Chip Oversampling Digital Filter
- SPI Compatible Interface
- Temperature Range: -40°C to 125°C
- Package: LQFP10X10-64

# Applications

- Power Line Monitor
- Power Line Protection Relays
- Motor Control
- Data Acquisition System (DAS)
- Industrial Automation and Controls

### Description

TPAFE5165 is a 16-bit, 8-channel simultaneous sampling, successive approximation (SAR) ADC. Each channel has a complete analog front end, as well as an ADC operating at 500 kSPS per channel. The analog front end features an input clamp, a programmable gain amplifier (PGA) with high input impedance of 1 M $\Omega$ , low pass filter with 200 kHz bandwidth, and an ADC input driver.

The device features an internal precision reference with a buffer to drive the ADC. A digital interface supports serial, parallel, and parallel byte communication, which can be used with various host controllers.

The TPAFE5165 can accept  $\pm 10$  V or  $\pm 5$  V true bipolar inputs with a single 5 V supply. Also, the high input impedance allows direct connection to transformers or other sensors without external driver circuits.

The zero-latency conversion with high performance also makes the device suitable for industrial automation and control applications.



# **Typical Application Circuit**



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# **Product Family Table**

Order Number	Input Range (V)	Package	
TPAFE5165H8-QP5R	±10, ±5	LQFP10X10-64	

# **Revision History**

Date	Revision	Notes
2024-04-01	Rev.Pre.0	Pre-release version.



# **Pin Configuration and Functions**



#### **Table 1. Pin Functions**

	Pin	1/0	Description
No.	Name	1/0	Description
1	AVDD	Р	Analog supply pin.
2	AGND	Р	Analog ground pin.
3	OS0	DI	Oversampling control pin.
4	OS1	DI	Oversampling control pin.
5	OS2	DI	Oversampling control pin.
6	PAR/SER/BYTE SEL	DI	Control pin to select the serial, parallel, or parallel byte interface mode.
7	STBY	DI	Control pin to select the standby or shutdown mode, active low.



	Pin		Description				
No.	Name	1/0	Description				
8	RANGE	DI	Multi-function logic input pin: When STBY is low, this pin selects between the standby and shutdown modes. When STBY is high, this pin selects input range of $\pm 10$ V or $\pm 5$ V.				
9	CONVSTA	DI	ctive high logic input to control the start of the conversion for the first half count of the nput channels of the device.				
10	CONVSTB	DI	Active high logic input to control the start of the conversion for the second half count of the input channels of the device.				
11	RESET	DI	Active high logic input to reset the digital logic of the device.				
12	RD/SCLK	DI	Multi-function logic input pin: This pin is active-low ready input pin in the parallel and parallel byte interface. This pin is clock input pin in the serial interface mode.				
13	CS	DI	Active low logic input chip-select signal.				
14	BUSY	DO	Active high digital output indicating ongoing conversion.				
15	FRSTDATA	DO	Active high digital output indicating data read back from channel 1 of the device.				
16	DB0	DO	Data output DB0 (LSB) in the parallel interface mode.				
17	DB1	DO	Data output DB1 in the parallel interface mode.				
18	DB2	DO	Data output DB2 in the parallel interface mode.				
19	DB3	DO	Data output DB3 in the parallel interface mode.				
20	DB4	DO	Data output DB4 in the parallel interface mode.				
21	DB5	DO	Data output DB5 in the parallel interface mode.				
22	DB6	DO	Data output DB6 in the parallel interface mode.				
23	DVDD	Р	Digital supply pin; decouple with AGND on pin 26.				
24	DB7/DOUTA	DO	Multi-function logic output pin: This pin is data output DB7 in the parallel and parallel byte interface mode. This pin is a data output pin in serial interface mode.				
25	DB8/DOUTB	DO	Multi-function logic output pin: This pin is data output DB8 in the parallel and parallel byte interface mode. This pin is a data output pin in the serial interface mode.				
26	AGND	Р	Analog ground pin.				
27	DB9	DO	Data output DB9 in the parallel interface mode.				
28	DB10	DO	Data output DB10 in the parallel interface mode.				
29	DB11	DO	Data output DB11 in the parallel interface mode.				
30	DB12	DO	Data output DB12 in the parallel interface mode.				
31	DB13	DO	Data output DB13 in the parallel interface mode.				
32	DB14/HBEN	DO	Multi-function logic input or output pin: This pin is data output DB14 in the parallel interface mode. This pin is a control input pin for byte selection (high or low) in the parallel byte interface mode.				
33	DB15/BYTE SEL	DO	Multi-function logic input or output pin:				



	Pin		Description
No.	Name	1/0	Description
			This pin is data output DB15 (MSB) in parallel interface mode.
			This pin is an active high-control input pin to enable the parallel byte interface mode.
34	REFSEL	DI	Active high logic input to enable the internal reference.
35	AGND	Р	Analog ground pin.
36	REGCAP1	AO	Output pin 1 for the internal voltage regulator; decouple separately to AGND using a 1- $\mu$ F capacitor. Typical 4 V.
37	AVDD	Р	Analog supply pin.
38	AVDD	Р	Analog supply pin.
39	REGCAP2	AO	Output pin 2 for the internal voltage regulator; decouple separately to AGND using a 1- $\mu$ F capacitor. Typical 4 V.
40	AGND	Р	Analog ground pin.
41	AGND	Р	Analog ground pin.
42	REFIN/REFOUT	AIO	This pin acts as an internal 2.5 V reference output when REFSEL is high. This pin functions as input pin for the external reference when REFSEL is low; decouple with REFGND on pin 43 using a $10-\mu$ F capacitor.
43	REFGND	Р	Reference GND pin. This pin must be shorted to the analog GND plane and decoupled with REFIN/REFOUT on pin 42 using a $10-\mu$ F capacitor.
44	REFCAPA	AO	Reference amplifier output pins. This pin must be shorted to REFCAPB and decoupled to AGND using a low ESR, $10-\mu$ F ceramic capacitor. Typical 4 V.
45	REFCAPB	AO	Reference amplifier output pins. This pin must be shorted to REFCAPA and decoupled to AGND using a low ESR, $10-\mu$ F ceramic capacitor. Typical 4 V.
46	REFGND	Р	Reference GND pin. This pin must be shorted to the analog GND plane and decoupled with REFIN/REFOUT on pin 42 using a 10- $\mu$ F capacitor.
47	AGND	Р	Analog ground pin.
48	AVDD	Р	Analog supply pin.
49	AIN_1P	AIO	Analog input channel 1: positive input.
50	AIN_1GND	AIO	Analog input channel 1: negative input.
51	AIN_2P	AIO	Analog input channel 2: positive input.
52	AIN_2GND	AIO	Analog input channel 2: negative input.
53	AIN_3P	AIO	Analog input channel 3: positive input.
54	AIN_3GND	AIO	Analog input channel 3: negative input.
55	AIN_4P	AIO	Analog input channel 4: positive input.
56	AIN_4GND	AIO	Analog input channel 4: negative input.
57	AIN_5P	AIO	Analog input channel 5: positive input.
58	AIN_5GND	AIO	Analog input channel 5: negative input.
59	AIN_6P	AIO	Analog input channel 6: positive input.
60	AIN_6GND	AIO	Analog input channel 6: negative input.
61	AIN_7P	AIO	Analog input channel 7: positive input.



	Pin	1/0	Description	
No.	Name	1/0		
62	AIN_7GND	AIO	Analog input channel 7: negative input.	
63	AIN_8P	AIO	Analog input channel 8: positive input.	
64	AIN_8GND	AIO	Analog input channel 8: negative input.	



# **Specifications**

### Absolute Maximum Ratings

All test conditions: At  $T_A = 25^{\circ}$ C, unless otherwise noticed.

	Parameter	Min	Max	Unit
AVDD to A	AGND	-0.3	7	V
DVDD to I	DGND	-0.3	7	V
AGND to I	DGND	-0.3	0.3	V
Analog In	out Voltage to AGND	-15	15	V
Digital Inp	ut to DGND	-0.3	DVDD + 0.3	V
REFIN to	AGND	-0.3	AVDD + 0.3	V
Input Curr	ent to Any Pin Except Supplies	-10	10	mA
TJ	Maximum Junction Temperature	-40	150	°C
T <sub>A</sub> Operating Temperature Range		-40	125	°C
T <sub>STG</sub>	Storage Temperature Range	-65	150	°C
TL	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) This data was taken with the JEDEC low effective thermal conductivity test board.

(3) This data was taken with the JEDEC standard multilayer test boards.

### ESD, Electrostatic Discharge Protection

Symbol	Parameter	Parameter Condition		
НВМ	Human Body Model ESD for all pins except analog input pins	ANSI/ESDA/JEDEC JS-001 (1)	±5000	V
НВМ	Human Body Model ESD for analog input pins only	ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±7000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### **Recommended Operating Conditions**

Parameter			Тур	Max	Unit
AVDD	Analog Supply Voltage	4.75	5	5.25	V
DVDD	Digital Supply Voltage	1.71	3.3	AVDD	V



### **Thermal Information**

Package Type	θ <sub>JA</sub>	θյς	Unit
LQFP10X10-64	46	7.8	°C/W



### **Electrical Characteristics**

All test conditions:  $V_{REF} = 2.5 \text{ V}$  external/internal, AVDD = 4.75 V to 5.25 V,  $V_{DRIVE} = 1.71 \text{ V}$  to AVDD,  $f_{SAMPLE} = 500 \text{ kSPS}$ ,  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , Default Analog Bandwidth unless otherwise noted.

Symbol	Parameter	Test condition		MIN	TYP	MAX	Unit	
Dynamic Performance								
		fin = 1 kHz Sine Wave,	±10 V	81	84		dB	
		No Oversampling	±5 V	79.5	82.3		dB	
	Oinn al ta Nais a Datia	fin = 20 kHz Sine Wave,	±10 V	80.5	83.3		dB	
SNR	Signal to Noise Ratio	No Oversampling	±5 V	79	82		dB	
		fin = 130 Hz	±10 V		93.4		dB	
		Oversampling by 16	±5 V		92.3		dB	
		fin = 1 kHz Sine Wave,	±10 V		84		dB	
	Signal to Noise +	No Oversampling	±5 V		82.2		dB	
SINAD	Distortion ratio	fin = 20 kHz Sine Wave,	±10 V		83		dB	
		Unless Otherwise Noted No Oversampling	±5 V		81.4		dB	
Т	Total Harmonic	All Input Range, fin = 1 K⊦	łz		-100		dB	
IHD	Distortion	All Input Range, fin = 20 K	Hz		-93		dB	
SFDR	Spurious Free Dynamic Range	fin = 1 KHz			-103		dB	
Analog In	put Filter						1	
		−3 dB, ±10 V			200		kHz	
BVV(-3 dB)	Small Signal Bandwidth	−3 dB, ±5 V			200		kHz	
DIA	0 11 0: 1 0 1 : 111	−0.1 dB, ±10 V			18		kHz	
BVV(-0.1 dB)	Small Signal Bandwidth	−0.1 dB, ±5 V			18		kHz	
-	One Deleve	±10 V			1.7		μs	
I group_delay	Group Delay	±5 V			1.7		μs	
DC Accura	асу							
Resolution		No Missing Code			16		bit	
DNL	Differential Nonlinearity	f <sub>SAMPLE</sub> = 500 kSPS, −10~8	35°C	-0.99	±0.7	1	LSB	
INL	Integral Nonlinearity	f <sub>SAMPLE</sub> = 500 kSPS, −10~8	35°C	-3	±1.4	3	LSB	
Positive ar	nd Negative Full Scale	Ext Reference			±10	±43	LSB	
Error		Int Reference			±20		LSB	
Dogitivo Eu	III Soolo Error Drift	Ext Reference			±2		ppm/°C	
FOSILIVE FU		Int Reference			±10		ppm/°C	
Negative E	ull Scale Error Drift	Ext Reference			±2		ppm/°C	
		Int Reference			±10		ppm/°C	
Bipolar Zei	ro Code Error	±10 V			±2	±13	LSB	



Symbol	Parameter	Test condition		MIN	TYP	MAX	Unit
		±5 V					
Din elen Ze	re Cada Errer Drift	±10 V			±10		µV/℃
Bipolar Ze	ro Code Error Drill	±5 V			±5		µV/℃
Bipolar Fu	I Scale Error Matching				±6	±23	LSB
Bipolar Zero Code Error matching		All Input Range			±2	±22	LSB
Analog In	put					-	
			RANGE = 1,	-10		10	
Input Rang	je	V <sub>x</sub> -V <sub>xGND</sub>	±10 V Range				v
			RANGE = $0,$	-5		5	
		+10 V Range	10 V Mange				
Analog Inp	out Current	±10 V Range		_	(V <sub>IN</sub> -2)/Rin		
CIN	Input Capacitance				5		nF
	Input Resistance				1 M		ohm
Input Impe	dance Drift				+20		ppm/°C
Reference Input/Output						11	
		REF SELECT = 0, Select Ext Ref, Force Voltage on REFIN/REFOUT		2.475			
Reference	Input Voltage				2.5	2.525	V
Reference Output Voltage		REF_SELECT = 1, REFIN/REFOUT Output Voltage, $T_A = 25^{\circ}C$		2.495	2.5	2.505	v
Reference	Voltage TC				±10		ppm/°C
		Voltage on REFCAPA and REFCAPB,					
V(REFCA	РА/В)	Also Used for ADC			4		V
Logic Inp	ut						
VIH	Input High Voltage	Input Logic High Voltage		$0.7^*V_{\text{DRIVE}}$			V
VIL	Input Low Voltage	Input Logic Low Voltage				0.3*VDRIVE	V
Cı	Input Capacitance	Input Capacitance			5		pF
h	Input Current	Input Current				±2	μA
Logic Out	put					1	
V <sub>OH</sub>	Output High Voltage	Current Source = 100 uA		V <sub>DRIVE</sub> -0.2			V
V <sub>OL</sub>	Output Low Voltage	Current Sink = 100 uA				0.2	V
	Float State Leakage				±1	±20	uА
	Current						F
Co	Output Capacitance				5		pF
Conversio	on Rate						
Conversion	n Time				1.37		μs
Acquisition					0.63	500	μs
Throughpu	it Rate	Per Channel				500	kSPS
Timing Sp	ecifications						



Symbol	I Parameter Test condition MIN				MAX	Unit
SCLK	Frequency of Serial	V <sub>DRIVE</sub> > 2.7 V			23.5	MHz
	Interface	V <sub>DRIVE</sub> > 1.7 V			15	MHz
AVCC Normal				40	50	mA
AVCC Standby				7	8	mA
AVCC Shutdown				13	18	μA



## Timing Specifications <sup>(1)</sup>

All test conditions:  $AV_{CC} = 5 V$ ,  $V_{DRIVE} = 1.7 V$  to 5.5 V,  $V_{REF} = 2.5 V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noticed.

Symbol	mbol Parameter Description				Limit at T <sub>MIN</sub> , T <sub>MAX</sub> (0.1 x V <sub>DRIVE</sub> and 0.9 x V <sub>DRIVE</sub> Logic Input Levels)			
			Min	Тур	Max			
Parallel/Se	erial/Byte Mo	de						
		1/Throughput Rate Parallel mode, reading during or after conversion; or serial mode: $V_{DRIVE}$ = 2.7 V to 5.5 V, reading during a conversion using DoutA and Dout B lines		2		μs		
tcycle		Serial mode: $V_{DRIVE}$ = 2.7 V, reading after a conversion using $D_{OUT}A$ and $D_{OUT}B$ lines		6.2		μs		
		Serial mode: $V_{DRIVE}$ = 1.7 V, reading after a conversion using $D_{OUT}A$ and $D_{OUT}B$ lines		7.7		μs		
		Conversion time						
		Oversampling off		1.37		μs		
		Oversampling by 2		4.56		μs		
		Oversampling by 4		8.53		μs		
LCONV		Oversampling by 8		16.51		μs		
		Oversampling by 16		32.4		μs		
		Oversampling by 32		64.4		μs		
		Oversampling by 64		128.3		μs		
t <sub>wake-up</sub> standby		STBY rising edge to CONVST x rising edge; power-up time from standby mode		100		μs		
t <sub>wake-up</sub>	Internal Reference	STBY rising edge to CONVST x rising edge; power-up time from shutdown mode		180		ms		
SHUTDOWN	External Reference	STBY rising edge to CONVST x rising edge; power-up time from shutdown mode		13		ms		
t <sub>RESET</sub>		RESET high pulse width		85		ns		
t1		CONVST x high to BUSY high		40		ns		
t <sub>2</sub>		Minimum CONVST x low pulse	25			ns		
t <sub>3</sub>		Minimum CONVST x high pulse	25			ns		
t4		BUSY falling edge to $\overline{CS}$ falling edge setup time	45			ns		
t <sub>5</sub>		Maximum delay allowed between CONVST A, CONVST B rising edges		0.5		ms		
t <sub>6</sub>		Minimum time between last $\overline{\text{CS}}$ rising edge and BUSY falling edge	110			ns		
t <sub>7</sub>		Minimum delay between RESET low to CONVST x high	200			ns		



Symbol	Parameter	neter Description		at T <sub>MIN</sub> , T <sub>M</sub> ₌ and 0.9 c Input Le	iax (0.1 x V <sub>drive</sub> evels)	Unit
			Min	Тур	Max	
Parellel/By	te Read Ope	ration				
t <sub>8</sub>		CS to RD setup time	0			ns
t <sub>9</sub>		$\overline{\text{CS}}$ to $\overline{\text{RD}}$ hold time	0			ns
		RD low pulse width				
t <sub>10</sub>		V <sub>DRIVE</sub> above 2.7 V	22			ns
		V <sub>DRIVE</sub> above 1.7 V	32			ns
t <sub>11</sub>		RD high pulse width	10			ns
t <sub>12</sub>		$\overline{\text{CS}}$ high pulse width; $\overline{\text{CS}}$ and $\overline{\text{RD}}$ linked	10			ns
		Delay from $\overline{\text{RD}}$ until DB[15:0] three-state disabled				
t <sub>13</sub>		V <sub>DRIVE</sub> above 2.7 V			21	ns
		V <sub>DRIVE</sub> above 1.7 V			30	ns
		Data access time after $\overline{RD}$ falling edge				
t <sub>14</sub>		V <sub>DRIVE</sub> above 2.7 V			21	ns
		V <sub>DRIVE</sub> above 1.7 V			30	ns
t <sub>15</sub>		Data hold time after $\overline{RD}$ falling edge	6			ns
t <sub>16</sub>		CS to DB[15:0] hold time	3[15:0] hold time 6			ns
t <sub>17</sub>		Delay from $\overline{\text{CS}}$ rising edge to DB[15:0] three-state enabled	ed 20		20	ns
Serial Rea	d Operation					
		Frequency of serial read clock				
fsclk		V <sub>DRIVE</sub> above 2.7 V			23.5	MHz
		V <sub>DRIVE</sub> above 1.7 V			15	MHz
		Delay from $\overline{CS}$ until $D_{OUT}A/D_{OUT}B$ three-state disabled/ delay from $\overline{CS}$ until MSB valid				
t <sub>18</sub>		V <sub>DRIVE</sub> above 2.7 V			10	ns
		V <sub>DRIVE</sub> above 1.7 V			15	ns
		Data access time after SCLK rising edge				
t		V <sub>DRIVE</sub> above 2.7 V			21	ns
19		V <sub>DRIVE</sub> above 1.7 V			30	ns
t <sub>20</sub>		SCLK low pulse width	0.4t <sub>SCLK</sub>			ns
t <sub>21</sub>		SCLK high pulse width	0.4tsclk			ns
t <sub>22</sub>		SCLK rising edge to DOUTA/DOUTB valid hold time	6			ns
t <sub>23</sub>		$\overline{\text{CS}}$ rising edge to $D_{\text{OUT}}A/D_{\text{OUT}}B$ three-state enabled			15	ns
Frstdata O	peration					
t <sub>24</sub>		Delay from $\overline{\text{CS}}$ falling edge until FRSTDATA three-state disabled				



Symbol	Parameter	Description	Limit a x V <sub>DRIVI</sub> Logi	Unit		
			Min	Тур	Max	
		V <sub>DRIVE</sub> above 2.7 V			11	ns
		V <sub>DRIVE</sub> above 1.7 V			20	ns
		Delay from $\overline{\text{CS}}$ falling edge until FRSTDATA high, serial mode				
t <sub>25</sub>		V <sub>DRIVE</sub> above 2.7 V			11	ns
		V <sub>DRIVE</sub> above 1.7 V			20	ns
		Delay from $\overline{RD}$ falling edge to FRSTDATA high				
t <sub>26</sub>		V <sub>DRIVE</sub> above 2.7 V			22	ns
		V <sub>DRIVE</sub> above 1.7 V			32	ns
		Delay from $\overline{RD}$ falling edge to FRSTDATA low				
t <sub>27</sub>		V <sub>DRIVE</sub> above 2.7 V			22	ns
		V <sub>DRIVE</sub> above 1.7 V			32	ns
		Delay from 16 <sup>th</sup> SCLK falling edge to FRSTDATA low				
t <sub>28</sub>		V <sub>DRIVE</sub> above 2.7 V			22	ns
		V <sub>DRIVE</sub> above 1.7 V			32	ns
t <sub>29</sub>		Delay from $\overline{\text{CS}}$ rising edge until FRSTDATA three-state enabled			20	ns

(1) Parameters are provided by lab bench test and design simulation.



### **Timing Diagrams**







#### Figure 2. CONVST Timing—Reading During a Conversion



Figure 3. Parallel Mode, Separate CS and RD Pulses





#### Figure 4. CS and RD, Linked Parallel Mode



#### Figure 5. Serial Read Operation (Channel 1)



Figure 6. BYTE Mode Read Operation



# **Detailed Description**

### Overview

TPAFE5165 is a 16-bit, 8-channel simultaneous sampling, successive approximation (SAR) ADC. Each channel has a complete analog front end, as well as an ADC operating at 500 kSPS per channel. The analog front end features an input clamp, a programmable gain amplifier (PGA) with high input impedance of 1 M $\Omega$ , a low pass filter, and an ADC input driver.

The device features an internal precision reference with a buffer to drive the ADC. A digital interface supports serial, parallel, and parallel byte communication, which can be used with various host controllers.

The TPAFE5165 can accept  $\pm 10$  V or  $\pm 5$  V true bipolar inputs with a single 5 V supply. Also, the high input impedance allows direct connection to transformers or other sensors without external driver circuits.

### Feature Description

#### Analog Inputs

The TPAFE5165 has 8 analog input channels, and positive inputs  $AIN_nP$  (n = 1 to 8) are the single-ended analog inputs and the negative inputs  $AIN_nGND$  should be tied to GND.

The input voltage range can be configured to bipolar ±10 V or ±5 V by the RANGE pin.

The device allows a ±0.3-V range on the AIN\_nGND

#### Analog Input Impedance

Each analog input channel in the device presents a constant resistive impedance of 1 M $\Omega$ .

Matching the external source impedance on the AIN\_nP input pin with an equivalent resistance on the AIN\_nGND pin is recommended to cancel any additional offset error contributed by the external resistance.

#### Input Clamp Protection Circuit

The input clamp protection circuit allows analog input to swing up to  $\pm 30$  V (typical). The input clamp circuit turns on beyond the clamp voltage.

For input voltages above the clamp threshold, make sure that the input current never exceeds the absolute maximum rating to prevent any damage to the device.

Don't keep the device in a state such that the clamp circuit is activated for extended periods of time, because this fault condition can degrade device performance and reliability.

#### Programmable Gain Amplifier (PGA)

The device has a programmable gain amplifier (PGA) at each individual input channel. The PGA converts the single-ended input signal into a fully-differential signal to drive internal ADC. The PGA also adjusts the common-mode voltage feeding into the ADC to ensure maximum usage of the ADC input dynamic range. The PGA gain is adjusted by configuring the RANGE pin of the ADC accordingly.

#### Low Pass Filter

Each channel of the TPAFE5165 features a second-order antialiasing low pass filter (LPF) at the output of the PGA, to remove the noise of the front-end amplifiers and gain resistors of the PGA.



#### ADC Driver

There is an integrated ADC input driver before each ADC channel. This integrated ADC driver eliminates the need any external amplifier, helping inputs of the ADC to settle to better than 16-bit accuracy before any sampled analog voltage gets converted. And thus the signal chain design for the user is simplified.

#### Digital Filter

The TPAFE5165 has an optional digital averaging filter that can be used in slower throughput applications requiring lower noise and higher dynamic range. The oversampling ratio of the digital filter is determined by the configuration of the OS[2:0] pins.

In oversampling mode, the samples are averaged to reduce the noise of the signal chain as well as to improve the SNR of the ADC. The final output is also decimated to provide data for each channel.

OS[2:0]	OS RATIO	MAX THROUGHPUT PER CHANNEL (kSPS)
000	NO OS	500
001	2	250
010	4	125
011	8	62.5
100	16	31.25
101	32	15.63
110	64	7.82
111	NA	500

#### Table 2. Oversample Bit Decoding

#### Reference

The TPAFE5165 can operate with either an internal voltage reference or an external voltage reference. The internal or external reference selection is determined by an external REFSEL pin,

The REFIN/REFOUT pin outputs the internal band-gap voltage (in internal reference mode) or functions as an input pin to the external reference voltage (in external reference mode). The on-chip amplifier is enabled in both modes to drive the actual reference input of the internal ADC core. The REFCAPA and REFCAPB pins must be shorted together externally and a ceramic capacitor of a minimum 10  $\mu$ F should be connected between this node and REFGND to ensure that the internal reference buffer is operating as a closed loop.

#### ADC Transfer Function

The TPAFE5165 outputs 16-bit data in binary twos complement format for both bipolar input ranges. The format for the output codes is the same across all analog channels.

#### Table 3. LSB Size

Input Range (V)	Full-Scale Range (V)	LSB (µV)		
±10	20	305.18		
±5	10	152.59		



### **Device Functional Modes**

#### Device Interface: Pin Description

#### • REFSEL (Input)

The REFSEL pin selects between the internal and external reference modes of the device.

If the REFSEL pin is set to logic high, then the internal reference is enabled and selected.

If the REFSEL pin is set to logic low, then the internal reference circuit is disabled and powered down. In this mode, an external reference voltage must be provided to the REFIN/REFOUT pin.

The internal reference buffer is always enabled under both conditions.

The reference mode after power-up depends on the state of the REFSEL input pin.

#### • REFSEL (Input)

The RANGE pin selects the input range for all analog input channels.

If this pin is set to logic high, the device is configured to operate in the ±10-V input range.

If this pin is set to logic low, the device is configured to operate in the ±5-V input range.

The RANGE pin is also used to put the device in standby or shutdown mode depending on the state of the STBY input pin, as explained in the Power-Down Modes section.

#### • STBY (Input)

The STBY pin puts the device into one of two power-down modes: standby and power down.

If this pin is set to logic high, the device is in normal operation mode.

If this pin is set to logic low, the device is in standby or power down mode, depending on the state of the RANGE pin.

In shutdown mode, all internal circuitry is powered down,

In standby mode, the internal reference remains powered up to enable a relatively quicker recovery to normal operation mode.

#### • PAR/SER/BYTE SEL (Input)

The PAR/SER/BYTE SEL pin selects between the parallel, serial, and parallel byte interface modes for reading data from the device.

If this pin is set to logic high, then the serial or parallel byte interface mode is selected depending on the state of the DB15/BYTE SEL pin. If the DB15/BYTE SEL pin is high, the parallel byte interface is selected, and if the DB15/BYTE SEL is low, then serial mode is selected.

#### • CONVSTA, CONVSTB (Input)

CONVSTA and CONVSTB (Input) are conversion control input pins.

CONVSTA can be used to simultaneously sample and initiate the conversion process for the first half count of device input channels (channels 1-4), and CONVSTB can be used to simultaneously sample and initiate the conversion process for the latter half count of device input channels (channels 5-8).

On the rising edge of the CONVSTA, CONVSTB signals, the internal track-and-hold circuits for each analog input channel are placed into hold mode and the sampled input signal is converted.



The CONVSTA, CONVSTB signals can be pulled low when the internal conversion is over, as indicated by the BUSY signal. At this point, the front-end circuit for all analog input channels acquires the respective input signals and the internal ADC is not converting.

The output data can be read from the device irrespective of the status of the CONVSTA, CONVSTB pins.

#### • RESET (Input)

The RESET pin can be used to reset the device at any time in an asynchronous manner. When the RESET pin is set to logic high, the device is in reset mode, and remains the state until the pin returns low.

The device should be reset after power-up or recovery from shut down mode when all the supplies and references have settled to the required accuracy.

#### • RD/SCLK(Input)

RD/SCLK(Input) is dual function pin to be used in different interface mode.

#### Table 4. RD/SCLK Pin Functionality

Device Operat	Device Operating Condition		
Parallel Interface	PAR/SEL/BYTE = 0 DB15/BYTE = 0	Active-low digital input pin to read the output data from the device.	
Parallel Byte Interface	PAR/SEL/BYTE = 1 DB15/BYTE = 1	In parallel or parallel byte interface mode, the output bus is enabled when both the $\overline{CS}$ and $\overline{RD}$ inputs are tied to a logic low input.	
Serial Interface	PAR/SEL/BYTE = 0 DB15/BYTE = 0	External clock input for the serial data interface. In serial mode, all synchronous accesses to the device are timed with respect to the rising edge of the SCLK signal.	

### • CS (Input)

The  $\overline{CS}$  pin is an active-low, chip-select signal.

A rising edge on the  $\overline{CS}$  signal outputs all the data lines in tri-state mode.

A falling edge of the  $\overline{CS}$  signal marks the beginning of the output data transfer frame in any interface mode of operation for the device.

#### • OS[2:0]

The OS[2:0] pins are active-high digital input pins used to configure the oversampling ratio for the internal digital filter on the device.

When OS[2:0] = 111, a higher filter bandwidth of ~30kHz is selected.



#### **Device Modes of Operation**

#### Power Down Modes

The device supports two power-down modes: standby mode and shutdown mode. The device can enter either power-down mode by pulling the  $\overline{\text{STBY}}$  pin to a logic level. Additionally, the selection between these two power-down modes is done by the state of the RANGE pin.

#### Table 5. Power-Down Mode Selection

Power Down Mode	STBY	Range		
Standby	0	1		
Shutdown	0	0		

#### Standby mode

In standby mode, only internal reference of the circuit is powered up, and analog front-end, signal-conditioning circuit for each channel remains powered down.

#### Shutdown mode

In shutdown mode, the entire internal circuitry is powered down.

#### **Conversion Control**

The device offers precise control of simultaneously sampling all analog input channels.

#### Simultaneous Sampling on All Input Channels

All the analog input channels to be simultaneously sampled by connecting CONVSTA and CONVSTB signals together, and a single CONVST signal should be used to control the sampling of all analog input channels of the device.

#### Simultaneous Sampling Two Sets of Input Channels

Two sets of analog input channels can be simultaneously sampled by separating CONVSTA and CONVSTB signals. And the device could not operate in oversampling mode in this state.

#### **Data Read Operation**

The device updates the internal data registers with the conversion data for all analog channels at the end of every conversion phase (when BUSY goes low).

If the output data are read after BUSY goes low, then the device outputs the conversion results for the current sample.

If the output data are read when BUSY is high, then the device outputs conversion result for the previous sample.

There are three interface mode:

Interface mode	PAR/SER/BYTE SEL	DB15/BYTE SEL
Parallel Interface	0	0
Parallel Byte Interface	1	1
Serial Interface	1	0

#### Table 6. Data Read Back Interface Mode Selection



#### **Data Read Operation**

The device updates the internal data registers with the conversion data for all analog channels at the end of every conversion phase (when BUSY goes low).

If the output data are read after BUSY goes low, then the device outputs the conversion results for the current sample.

If the output data are read when BUSY is high, then the device outputs conversion result for the previous sample.

There are three interface mode:

#### Table 7. Data Read Back Interface Mode Selection

Interface mode	PAR/SER/BYTE SEL	DB15/BYTE SEL		
Parallel Interface	0	0		
Parallel Byte Interface	1	1		
Serial Interface	1	0		

#### Parallel Data Read

The device supports a parallel interface mode for reading the device output data using the control inputs ( $\overline{CS}$  and  $\overline{RD}$ ), the parallel output bus (DB[15:0]), and the BUSY indicator.

For applications that use only one device in the system and does not share the parallel output bus with any other devices, the  $\overline{CS}$  and  $\overline{RD}$  input signals can be tied together, or the  $\overline{CS}$  signal can be permanently tied low. At the first falling edge of the  $\overline{CS}$  and  $\overline{RD}$  signal, the output data of channel 1 becomes available on the parallel bus to be read by the digital host. At this instant the FRSTDATA output also goes high, indicating channel 1 data are ready to be read back. The output data for the remaining channels are clocked out on the parallel bus on subsequent falling edges of the  $\overline{CS}$  and  $\overline{RD}$  signal in a sequential manner.

For applications that use multiple devices in the system, the  $\overline{CS}$  and  $\overline{RD}$  input signals must be driven separately.

#### Parallel Byte Data Read

The parallel byte interface mode is very similar to the parallel interface mode, except that the output data for each channel is read in two data transfers of 8-bit byte sizes.

In parallel byte mode, the DB14/HBEN pin decides the order of most significant byte (MSB byte) and least significant byte (LSB byte). When DB14/HBEN pin is tied high, the MSB byte of the conversion results is output first followed by the LSB byte. This order is reversed when DB14/HBEN is tied to logic low.

At the first falling edge of the  $\overline{\text{RD}}$  signal, the first byte of the channel 1 conversion result becomes available on DB[7:0]. This byte is followed by the second byte of conversion data on the next falling edge of the RD signal.

#### Serial Data Read

This interface mode uses a  $\overline{CS}$  control input, a communication clock input (SCLK), BUSY and FRSTDATA output indicators, and serial data output lines DOUTA and DOUTB.

A total of 16 SCLK cycles are required to clock out 16 bits of conversion result for each channel and the same process can be repeated for the remaining channels in an ascending order.

The conversion results from the first set of channels appear first on DOUTA, followed by the second set of channels if only DOUTA is used for reading data. This order is reversed for DOUTB, in which the second set of channels appear first followed by the first set of channels. The use of both data output lines reduces the time needed for data retrieval and a higher throughput can therefore be achieved in this mode.



#### **Data Read During Conversion**

The device allows data read when and the ADC is converting, and the BUSY output is high status. In this case, the ADC outputs conversion results for previous samples.

The data read back during conversion mode allows faster throughput to be achieved from the device.

#### Data Read During Conversion

The device can be configured in oversampling mode by the OS[2:0] pins. The input on the OS pins is latched on the falling edge of the BUSY signal to configure the oversampling rate for the next conversion.

In this mode, the CONVST A and CONVST B signals should be tied or driven together.

The BUSY signal duration varies with the OSR setting because the conversion time increases with OSR setting.

Oversampling the input signal reduces noise during the conversion process, thus reducing the histogram code spread for a DC input signal to the ADC.



# Tape and Reel Information





Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPAFE5165H8-QP5R	LQFP10X10-64	330	30.4	10.36	10.36	2.1	16	24	Q1



## Package Outline Dimensions

### LQFP10x10-64





## **Order Information**

Order Number	Junction Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPAFE5165H8-QP5R	−40 to 125°C	LQFP 10X10-64	AFE5165	MSL3	Tape and Reel, 1000	Green

**Green**: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.



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