16-Bit, 8-Channel, Simultaneous Sampling ADC with Bipolar Inputs

Features

- 8 Simultaneously Sampled Inputs
- Single 5-V Analog Supply and 1.71-V to 5-V V_{DRIVE}
- 16-Bit ADC with 350 kSPS on All Channels
- Bipolar Inputs Ranges: ±10 V, ±5 V
- Analog Input Clamp Protection
- 1-MΩ Analog Input Impedance
- On-Chip Reference and Buffer
- On-Chip Oversampling Digital Filter
- SPI Compatible Interface
- Temperature Range: −40°C to 125°C
- Package: LQFP10×10-64

Applications

- Power Line Monitor
- Power Line Protection Relays
- Motor Control
- Data Acquisition System (DAS)
- Industrial Automation and Controls

Description

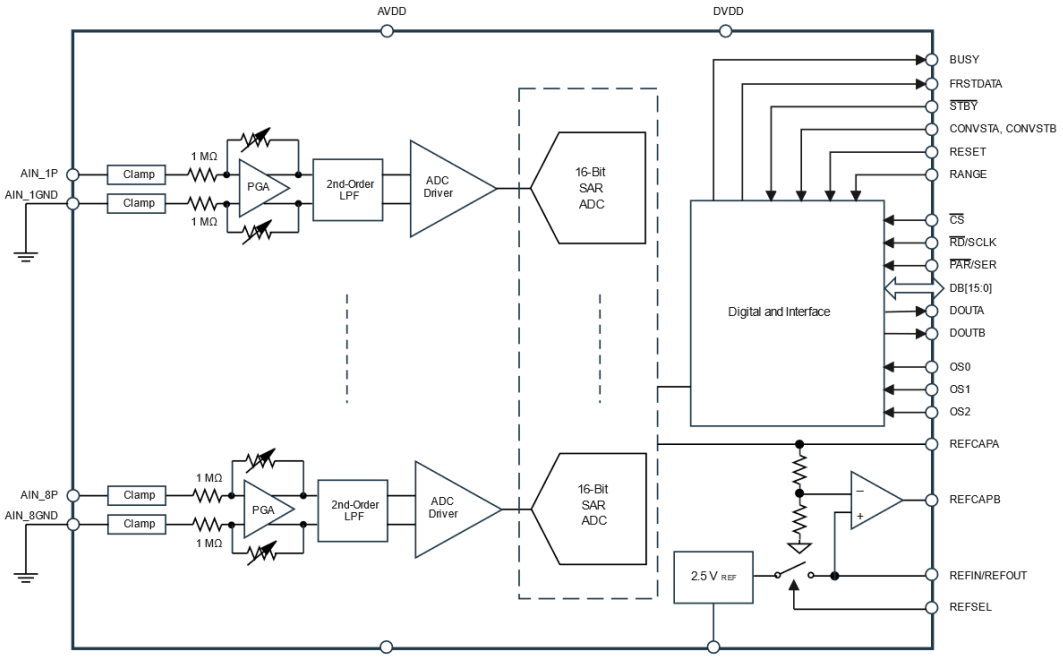
The TPAFE5160 is a 16-bit, 8-channel simultaneous sampling, successive approximation (SAR) ADC. Each channel has a complete analog front end, as well as an ADC operating at 350 kSPS per channel. The analog front end features the input clamp, a programmable gain amplifier (PGA) with a high input impedance of 1 MΩ, a low pass filter, and an ADC input driver.

The device features an internal precision reference with buffer to drive the ADC. A digital interface supports serial, parallel and parallel byte communication, which can be used with various host controllers.

The TPAFE5160 can accept ±10-V or ± 5-V true bipolar inputs with a single 5-V supply. Also, the high input impedance allows direct connection to transformers or other sensors without external driver circuits.

The zero-latency conversion with high performance also makes the device suitable for industrial automation and control applications.

Typical Application Circuit



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Product Family Table

Order Number	Input Range (V)	Package
TPAFE5160SI08-QP7R	±10, ±5	LQFP10×10-64

Revision History

Date	Revision	Notes
2021-11-15	Rev.Pre.0	Pre-release version.
2022-03-01	Rev.Pre.1	Updated the diagram and the EC table.
2022-05-10	Rev.Pre.2	Updated the EC table.
2022-05-22	Rev.Pre.3	Updated the tape and reel parameters.
2022-06-20	Rev.Pre.4	Updated the EC table.
2022-11-21	Rev.Pre.5	Updated Timing Specifications and Timing Diagrams.
2023-07-10	Rev.A.0	Initial released version.
2024-11-26	Rev.A.1	Updated to a new datasheet format. Updated Timing Specifications.

Pin Configuration and Functions

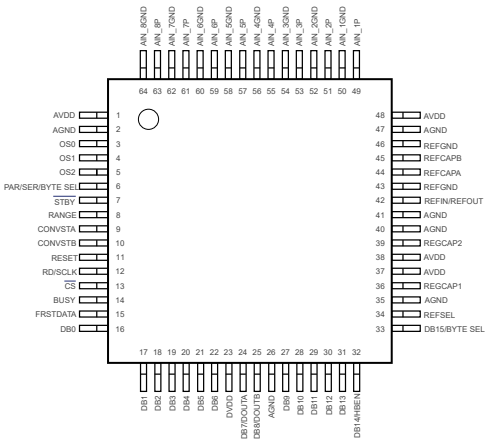


Table 1. Pin Functions

Pin		I/O	Description
No.	Name		
1	AVDD	P	Analog supply pin.
2	AGND	P	Analog ground pin.
3	OS0	DI	Oversampling control pin.
4	OS1	DI	Oversampling control pin.
5	OS2	DI	Oversampling control pin.
6	$\overline{\text{PAR}}$/SER/ BYTE SEL	DI	Control pin to select the serial, parallel, or parallel byte interface mode.
7	$\overline{\text{STBY}}$	DI	Control pin to select the standby or shutdown mode, active low.
8	RANGE	DI	Multi-function logic input pin: When STBY is low, this pin selects between the standby and shutdown modes. When STBY is high, this pin selects an input range of ±10 V or ±5 V.
9	CONVSTA	DI	Active high logic input to control the start of the conversion for the first half count of the input channels of the device.
10	CONVSTB	DI	Active high logic input to control the start of the conversion for the second half count of the input channels of the device.
11	RESET	DI	Active high logic input to reset the digital logic of the device.
12	$\overline{\text{RD}}$/SCLK	DI	Multi-function logic input pin: This pin is active-low ready input pin in the parallel and parallel byte interface. This pin is the clock input pin in the serial interface mode.
13	$\overline{\text{CS}}$	DI	Active low logic input chip-select signal.
14	BUSY	DO	Active high digital output indicating ongoing conversion.
15	FRSTDAT A	DO	Active high digital output indicating data read back from channel 1 of the device.
16	DB0	DO	Data output DB0 (LSB) in the parallel interface mode.

Pin		I/O	Description
No.	Name		
17	DB1	DO	Data output DB1 in the parallel interface mode.
18	DB2	DO	Data output DB2 in the parallel interface mode.
19	DB3	DO	Data output DB3 in the parallel interface mode.
20	DB4	DO	Data output DB4 in the parallel interface mode.
21	DB5	DO	Data output DB5 in the parallel interface mode.
22	DB6	DO	Data output DB6 in the parallel interface mode.
23	DVDD	P	Digital supply pin; decouple with AGND on pin 26.
24	DB7/ DOUTA	DO	Multi-function logic output pin: This pin is data output DB7 in the parallel and parallel byte interface mode. This pin is a data output pin in serial interface mode.
25	DB8/ DOUTB	DO	Multi-function logic output pin: This pin is data output DB8 in the parallel and parallel byte interface mode. This pin is a data output pin in the serial interface mode.
26	AGND	P	Analog ground pin.
27	DB9	DO	Data output DB9 in the parallel interface mode.
28	DB10	DO	Data output DB10 in the parallel interface mode.
29	DB11	DO	Data output DB11 in the parallel interface mode.
30	DB12	DO	Data output DB12 in the parallel interface mode.
31	DB13	DO	Data output DB13 in the parallel interface mode.
32	DB14/ HBEN	DO	Multi-function logic input or output pin: This pin is data output DB14 in the parallel interface mode. This pin is a control input pin for byte selection (high or low) in the parallel byte interface mode.
33	DB15/ BYTE SEL	DO	Multi-function logic input or output pin: This pin is data output DB15 (MSB) in parallel interface mode. This pin is an active high-control input pin to enable the parallel byte interface mode.
34	REFSEL	DI	Active high logic input to enable the internal reference.
35	AGND	P	Analog ground pin.
36	REGCAP1	AO	Output pin 1 for the internal voltage regulator; decouple separately to AGND using a 1-μF capacitor. Typical 4 V.
37	AVDD	P	Analog supply pin.
38	AVDD	P	Analog supply pin.
39	REGCAP2	AO	Output pin 2 for the internal voltage regulator; decouple separately to AGND using a 1-μF capacitor. Typical 4 V.
40	AGND	P	Analog ground pin.
41	AGND	P	Analog ground pin.
42	REFIN/ REFOUT	AIO	This pin acts as an internal 2.5 V reference output when REFSEL is high. This pin functions as an input pin for the external reference when REFSEL is low; decouple with REFGND on pin 43 using a 10-μF capacitor.

Pin		I/O	Description
No.	Name		
43	REFGND	P	Reference GND pin. This pin must be shorted to the analog GND plane and decoupled with REFIN/REFOUT on pin 42 using a 10-μF capacitor.
44	REFCAPA	AO	Reference amplifier output pins. This pin must be shorted to REFCAPB and decoupled to AGND using a low ESR, 10-μF ceramic capacitor. Typical 4 V.
45	REFCAPB	AO	Reference amplifier output pins. This pin must be shorted to REFCAPA and decoupled to AGND using a low ESR, 10-μF ceramic capacitor. Typical 4 V.
46	REFGND	P	Reference GND pin. This pin must be shorted to the analog GND plane and decoupled with REFIN/REFOUT on pin 42 using a 10-μF capacitor.
47	AGND	P	Analog ground pin.
48	AVDD	P	Analog supply pin.
49	AIN_1P	AIO	Analog input channel 1: positive input.
50	AIN_1GND	AIO	Analog input channel 1: negative input.
51	AIN_2P	AIO	Analog input channel 2: positive input.
52	AIN_2GND	AIO	Analog input channel 2: negative input.
53	AIN_3P	AIO	Analog input channel 3: positive input.
54	AIN_3GND	AIO	Analog input channel 3: negative input.
55	AIN_4P	AIO	Analog input channel 4: positive input.
56	AIN_4GND	AIO	Analog input channel 4: negative input.
57	AIN_5P	AIO	Analog input channel 5: positive input.
58	AIN_5GND	AIO	Analog input channel 5: negative input.
59	AIN_6P	AIO	Analog input channel 6: positive input.
60	AIN_6GND	AIO	Analog input channel 6: negative input.
61	AIN_7P	AIO	Analog input channel 7: positive input.
62	AIN_7GND	AIO	Analog input channel 7: negative input.
63	AIN_8P	AIO	Analog input channel 8: positive input.
64	AIN_8GND	AIO	Analog input channel 8: negative input.

Specifications

Absolute Maximum Ratings (1)

All test conditions: T_A = 25℃, unless otherwise noted.

Parameter		Min	Max	Unit
	AVDD to AGND	−0.3	7	V
	DVDD to DGND	−0.3	7	V
	AGND to DGND	−0.3	0.3	V
	Analog Input Voltage to AGND	−15	15	V
	Digital Input to DGND	−0.3	DVDD + 0.3	V
	REFIN to AGND	−0.3	AVDD + 0.3	V
	Input Current to Any Pin Except Supplies	−10	10	mA
T_J	Maximum Junction Temperature	−40	150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD for all pins except analog input pins	ANSI/ESDA/JEDEC JS-001 (1)	±5000	V
HBM	Human Body Model ESD for analog input pins only	ANSI/ESDA/JEDEC JS-001 (1)	±7000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
AVDD	Analog Supply Voltage	4.75	5	5.25	V
DVDD	Digital Supply Voltage	1.71	3.3	AVDD	V

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
LQFP10×10-64	46	7.8	°C/W

Electrical Characteristics

All test conditions: V_{REF} = 2.5 V external/internal, AVDD = 4.75 V to 5.25 V, V_{DRIVE} = 1.71 V to AVDD, f_{SAMPLE} = 350 kSPS, T_A = −40℃ to 125℃, Low Bandwidth Mode, unless otherwise noted.

Symbol	Parameter	Test condition		Min	Typ	Max	Unit
Dynamic Performance							
SNR	Signal-to-Noise Ratio	fin = 1 kHz sine wave, unless otherwise noted	±10 V No oversampling	86	89.7		dB
			±5 V No oversampling	85.5	89.5		dB
		fin = 130 Hz	Oversampling by 16, ±10-V Range	91	95.2		dB
		fin = 130 Hz	Oversampling by 16, ±5-V Range	91	94.7		dB
SINAD	Signal to Noise + Distortion Ratio	fin = 1 kHz sine wave, unless otherwise noted	±10 V No oversampling		89.5		dB
			±5 V No oversampling		89.4		dB
THD	Total Harmonic Distortion	All input range, fin =1 kHz			−106		dB
SFDR	Spurious Free Dynamic Range	fin = 1 kHz			−106		dB
Analog Input Filter							
BW (−3 dB)	Small Signal Bandwidth	Low Bandwidth Mode	−3 dB, ±10 V		20.0		kHz
		Low Bandwidth Mode	−3 dB, ±5 V		12.7		kHz
		High Bandwidth Mode	−3 dB, ±10 V		26.5		kHz
		High Bandwidth Mode	−3 dB, ±5 V		16.4		kHz
BW (−0.1 dB)	Small Signal Bandwidth	Low Bandwidth Mode	−0.1 dB, ±10 V		3.3		kHz
		Low Bandwidth Mode	−0.1 dB, ±5 V		2.2		kHz
		High Bandwidth Mode	−0.1 dB, ±10 V		4.3		kHz
		High Bandwidth Mode	−0.1 dB, ±5 V		2.6		kHz
Tgroup_delay	Group Delay	Low Bandwidth Mode	±10 V		10		µs
		Low Bandwidth Mode	±5 V		16		µs
		High Bandwidth Mode	±10 V		8		µs
		High Bandwidth Mode	±5 V		12		µs
DC Accuracy							
	Resolution		NO missing code		16		bit
DNL	Differential Nonlinearity	f_{SAMPLE} = 200 kSPS, −40~85℃		−0.99	±0.5	1.5	LSB
INL	Integral Nonlinearity	f_{SAMPLE} = 200 kSPS, −40~85℃			±0.7	±2	LSB
		f_{SAMPLE} = 350 kSPS, −40~85℃			±1	±2.5	LSB

	Positive and Negative Full-Scale Error	Ext reference			±4	±50	LSB
		Int reference			±15		LSB
	Positive Full-Scale Error Drift	Ext reference			±2		ppm/C
		Int reference			±10		ppm/C
	Negative Full-Scale Error Drift	Ext reference			±2		ppm/C
		Int reference			±10		ppm/C
	Bipolar Zero Code Error		±10 V		±1	±15	LSB
			±5 V				
	Bipolar Zero Code Error Drift		±10 V		±10		µV/C
			±5 V		±5		µV/C
	Bipolar Full-Scale Error Matching				±6	±22	LSB
	Bipolar Zero Code Error matching		±5 V ±10 V		±3	±20	LSB
Analog Input							
	Input Range	Vx − VxGND	RANGE = 1, ±10-V range	−10		10	V
			RANGE = 0, ±5-V range	−5		5	
	Analog Input Current		10-V range		(V_{IN} − 2) / R_{IN}		µA
			5-V range				µA
C_{IN}	Input Capacitance				5		pF
R_{IN}	Input Resistance				1		Mohm
	Input Impedance Drift				±20		ppm/C
Reference Input/Output							
	Reference Input Voltage	REF SELECT = 0, select Ext Ref, force voltage on REFIN/REFOUT		2.475	2.5	2.525	V
	Reference Output Voltage	REF_SELECT = 1, REFIN/REFOUT output voltage T_A = 25°C		2.495	2.5	2.505	V
	Reference Voltage TC				±10		ppm/C
	V (REFCAPA/B)	Voltage on REFCAPA and REFCAPB, also used for ADC			4		V
Logic Input							
V_{IH}	Input High Voltage	Input logic high voltage		0.7 × V_{DRIVE}			V
V_{IL}	Input Low Voltage	Input logic low voltage				0.3 × V_{DRIVE}	V
C_I	Input Capacitance	Input capacitance			5		pF
I_I	Input Current	Input current				±2	µA

Logic Output							
V_{OH}	Output High Voltage		Current source = 100 µA	V_{DRIVE} − 0.2			V
V_{OL}	Output Low Voltage		Current sink = 100 µA			0.2	V
	Float State Leakage Current				±1	±20	µA
C_O	Output Capacitance				5		pF
Conversion Rate							
	Conversion Time				1.65		µs
	Acquisition Time				1.2		µs
	Throughput Rate	Per channel				350	kSPS
Timing specifications							
SCLK	Frequency of Serial Interface		V_{DRIVE} > 2.7 V			23.5	MHz
			V_{DRIVE} > 1.7 V			15	MHz
	AVCC Normal				41	51	mA
	AVCC Standby				5	9	mA
	AVCC Shutdown				11	25	µA

(1) 100% tested at T_A = 25℃.

Timing Specifications

All test conditions: AV_{CC} = 5 V, V_{DRIVE} = 1.7 V to 5.5 V, V_{REF} = 2.5 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	Limit at T_{MIN}, T_{MAX} (0.1 × V_{DRIVE} and 0.9 × V_{DRIVE} Logic Input Levels)			Unit	Description
	Min	Typ	Max		
Parallel/Serial/Byte Mode					
t_{CYCLE}					1/throughput rate
		2.85		μs	Parallel mode, reading during or after conversion; or serial mode: V_{DRIVE} = 2.7 V to 5.5 V, reading during conversion using $D_{OUT}A$ and $D_{OUT}B$ lines
		4.5		μs	Serial mode: V_{DRIVE} = 2.7 V, reading after a conversion using $D_{OUT}A$ and $D_{OUT}B$ lines
		6		μs	Serial mode: V_{DRIVE} = 1.7 V, reading after a conversion using $D_{OUT}A$ and $D_{OUT}B$ lines
t_{CONV}					Conversion time
		1.74		μs	Oversampling off
		4.4		μs	Oversampling by 2
		9.6		μs	Oversampling by 4
		20		μs	Oversampling by 8
		41		μs	Oversampling by 16
		83		μs	Oversampling by 32
		167		μs	Oversampling by 64
$t_{WAKE-UP\ STANDBY}$		100		μs	$\overline{STBY}$ rising edge to CONVST × rising edge; power-up time from standby mode
$t_{WAKE-UP\ SHUTDOWN}$ Internal Reference		180		ms	$\overline{STBY}$ rising edge to CONVST × rising edge; power-up time from shutdown mode
$t_{WAKE-UP\ SHUTDOWN}$ External Reference		13		ms	$\overline{STBY}$ rising edge to CONVST × rising edge; power-up time from shutdown mode
t_{RESET}		100		ns	RESET high pulse width
t_1		40		ns	CONVST × high to BUSY high
t_2	25			ns	Minimum CONVST × low pulse
t_3	25			ns	Minimum CONVST × high pulse
t_4	45			ns	BUSY falling edge to $\overline{CS}$ falling edge setup time
t_5		0.5		ms	Maximum delay allowed between CONVST A, CONVST B rising edges

t_6	110			ns	Minimum time between last $\overline{CS}$ rising edge and BUSY falling edge
t_7	200			ns	Minimum delay between RESET low to CONVST × high
Parallel/Byte Read Operation					
t_8	0			ns	$\overline{CS}$ to $\overline{RD}$ setup time
t_9	0			ns	$\overline{CS}$ to $\overline{RD}$ hold time
t_{10}					$\overline{RD}$ low pulse width
	22			ns	V_{DRIVE} above 2.7 V
	32			ns	V_{DRIVE} above 1.7 V
t_{11}	10			ns	$\overline{RD}$ high pulse width
t_{12}	10			ns	$\overline{CS}$ high pulse width; $\overline{CS}$ and $\overline{RD}$ linked
t_{13}					Delay from $\overline{CS}$ until DB [15:0] three-state disabled
			21	ns	V_{DRIVE} above 2.7 V
			30	ns	V_{DRIVE} above 1.7 V
t_{14}					Data access time after $\overline{RD}$ falling edge
			21	ns	V_{DRIVE} above 2.7 V
			30	ns	V_{DRIVE} above 1.7 V
t_{15}	6			ns	Data hold time after $\overline{RD}$ falling edge
t_{16}	6			ns	$\overline{CS}$ to DB [15:0] hold time
t_{17}			20	ns	Delay from $\overline{CS}$ rising edge to DB [15:0] three-state enabled
Serial Read Operation					
f_{SCLK}					Frequency of serial read clock
			23.5	MHz	V_{DRIVE} above 2.7 V
			15	MHz	V_{DRIVE} above 1.7 V
t_{18}					Delay from CS until $D_{OUT}A/D_{OUT}B$ three-state disabled/ delay from $\overline{CS}$ until MSB valid
			10	ns	V_{DRIVE} above 2.7 V
			15	ns	V_{DRIVE} above 1.7 V
t_{19}					Data access time after SCLK rising edge
			21	ns	V_{DRIVE} above 2.7 V
			30	ns	V_{DRIVE} above 1.7 V
t_{20}	$0.4t_{SCLK}$			ns	SCLK low pulse width
t_{21}	$0.4t_{SCLK}$			ns	SCLK high pulse width
t_{22}	6			ns	SCLK rising edge to $D_{OUT}A/D_{OUT}B$ valid hold time
t_{23}			15	ns	$\overline{CS}$ rising edge to $D_{OUT}A/D_{OUT}B$ three-state enabled
FRATDATA Operation					
t_{24}					Delay from $\overline{CS}$ falling edge until FRSTDATA three-state disabled

t_{24}			11	ns	V_{DRIVE} above 2.7 V
			20	ns	V_{DRIVE} above 1.7 V
t_{25}					Delay from $\overline{CS}$ falling edge until FRSTDATA high, serial mode
			11	ns	V_{DRIVE} above 2.7 V
			20	ns	V_{DRIVE} above 1.7 V
t_{26}					Delay from $\overline{RD}$ falling edge to FRSTDATA high
			22	ns	V_{DRIVE} above 2.7 V
			32	ns	V_{DRIVE} above 1.7 V
t_{27}					Delay from $\overline{RD}$ falling edge to FRSTDATA low
			22	ns	V_{DRIVE} above 2.7 V
			32	ns	V_{DRIVE} above 1.7 V
t_{28}					Delay from the 16^{th} SCLK falling edge to FRSTDATA low
			22	ns	V_{DRIVE} above 2.7 V
			32	ns	V_{DRIVE} above 1.7 V
t_{29}			20	ns	Delay from $\overline{CS}$ rising edge until FRSTDATA three-state enabled

Timing Diagrams

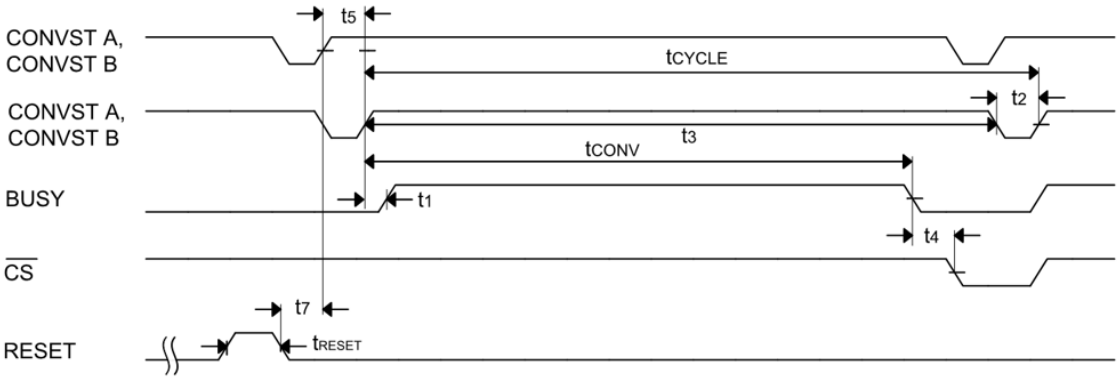


Figure 1. CONVST Timing-Reading After a Conversion

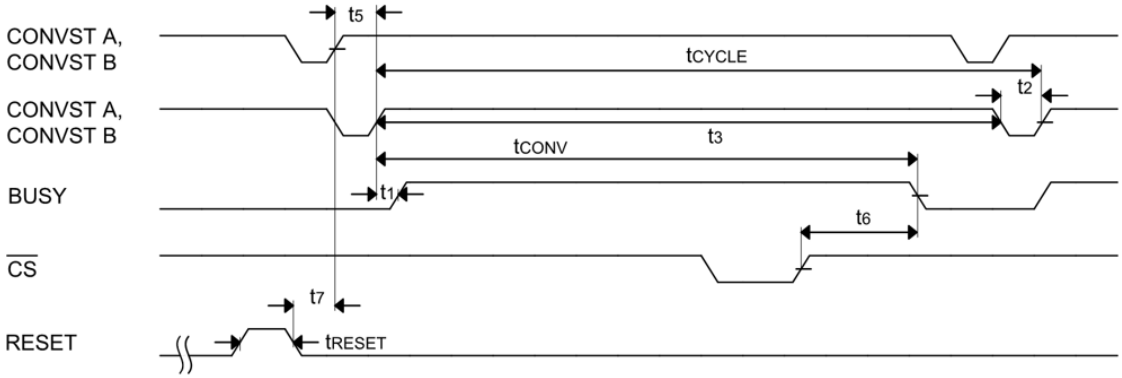


Figure 2. CONVST Timing-Reading During a Conversion

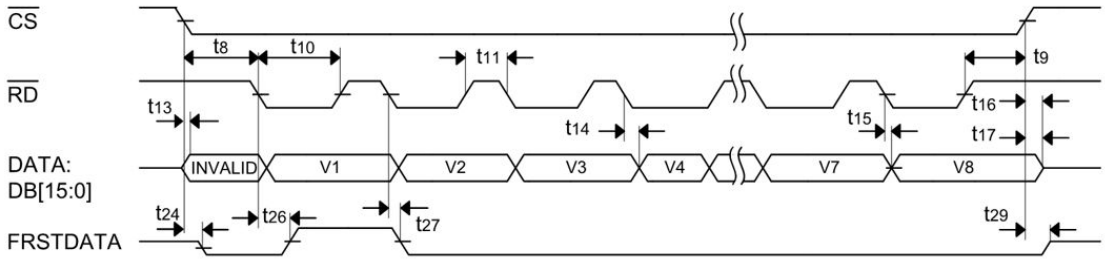


Figure 3. Parallel Mode, Separate $\overline{CS}$ and $\overline{RD}$ Pulses

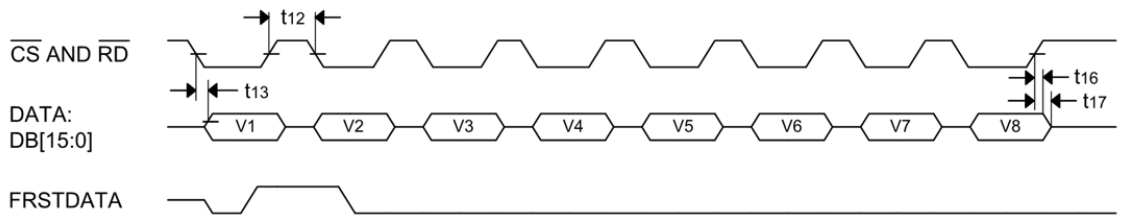


Figure 4. $\overline{CS}$ and $\overline{RD}$, Linked Parallel Mode

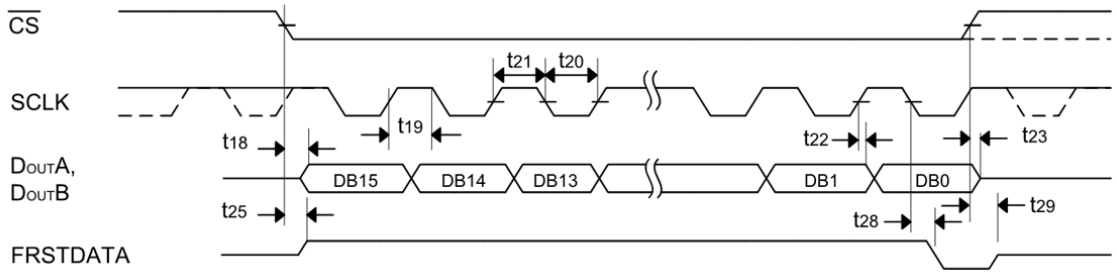


Figure 5. Serial Read Operation (Channel 1)

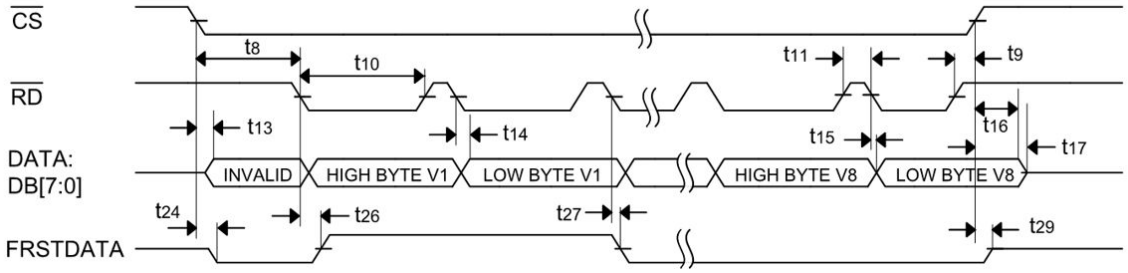


Figure 6. BYTE Mode Read Operation

Detailed Description

Overview

The TPAFE5160 is a 16-bit, 8-channel simultaneous sampling, successive approximation (SAR) ADC. Each channel has a complete analog front end, as well as an ADC operating at 350 kSPS per channel. The analog front end features the input clamp, a programmable gain amplifier (PGA) with a high input impedance of 1 MΩ, a low pass filter, and an ADC input driver.

The device features an internal precision reference with a buffer to drive the ADC. A digital interface supports serial, parallel, and parallel byte communication, which can be used with various host controllers.

The TPAFE5160 can accept ±10-V or ±5-V true bipolar inputs with a single 5-V supply. Also, the high input impedance allows direct connection to transformers or other sensors without external driver circuits.

Feature Description

Analog Inputs

The TPAFE5160 has 8 analog input channels, and positive inputs AIN_*n*P (n = 1 to 8) are the single-ended analog inputs. The negative inputs AIN_*n*GND should be tied to GND.

The input voltage range can be configured to bipolar ±10 V or ±5 V by the RANGE pin.

The device allows a ±0.3-V range on the AIN_*n*GND.

Analog Input Impedance

Each analog input channel in the device presents a constant resistive impedance of 1 MΩ.

Matching the external source impedance on the AIN_*n*P input pin with an equivalent resistance on the AIN_*n*GND pin is recommended to cancel any additional offset error contributed by the external resistance.

Input Clamp Protection Circuit

The input clamp protection circuit allows the analog input to swing up to ±30 V (typical). The input clamp circuit turns on beyond the clamp voltage.

For input voltages above the clamp threshold, make sure that the input current never exceeds the absolute maximum rating to prevent any damage to the device.

Don’t keep the device in a state such that the clamp circuit is activated for extended periods of time, because this fault condition can degrade the performance and reliability of the device.

Programmable Gain Amplifier (PGA)

The device has a programmable gain amplifier (PGA) at each individual input channel. The PGA converts the single-ended input signal into a fully-differential signal to drive internal ADC. The PGA also adjusts the common-mode voltage feeding into the ADC to ensure maximum usage of the ADC input dynamic range. The PGA gain is adjusted by configuring the RANGE pin of the ADC accordingly.

Low Pass Filter

Each channel of the TPAFE5160 features a second-order antialiasing low pass filter (LPF) at the output of the PGA, to remove the noise of the front-end amplifiers and gain resistors of the PGA.

ADC Driver

There is an integrated ADC input driver before each ADC channel. This integrated ADC driver eliminates the need of any external amplifier, helping inputs of the ADC to settle to better than 16-bit accuracy before any sampled analog voltage gets converted. And thus, the signal chain design for the user is simplified.

Digital Filter

The TPAFE5160 has an optional digital averaging filter that can be used in slower throughput applications requiring lower noise and higher dynamic range. The oversampling ratio of the digital filter is determined by the configuration of the OS[2:0] pins.

In oversampling mode, the samples are averaged to reduce the noise of the signal chain as well as to improve the SNR of the ADC. The final output is also decimated to provide data for each channel.

OS [2:0]	OS RATIO	MAX THROUGHPUT PER CHANNEL (kSPS)
000	NO OS	350
001	2	175
010	4	87.5
011	8	43.75
100	16	21.875
101	32	10.94
110	64	5.47
111	NA	350

Reference

The TPAFE5160 can operate with either an internal voltage reference or an external voltage reference. The internal or external reference selection is determined by an external REFSEL pin,

The REFIN/REFOUT pin outputs the internal band-gap voltage (in the internal reference mode) or functions as the input pin to the external reference voltage (in the external reference mode). The on-chip amplifier is enabled in both modes to drive the actual reference input of the internal ADC core. The REFCAPA and REFCAPB pins must be shorted together externally and a ceramic capacitor of a minimum 10 μF should be connected between this node and REFGND to ensure that the internal reference buffer is operating as a closed loop.

ADC Transfer Function

The TPAFE5160 outputs 16-bit data in binary twos complement format for both bipolar input ranges. The format for the output codes is the same across all analog channels.

Input Range (V)	Full-Scale Range (V)	LSB (μV)
±10	20	305.18
±5	10	152.59

Device Functional Modes

Device Interface: Pin Description

REFSEL (Input)

The REFSEL pin selects between the internal and external reference modes of the device.

If the REFSEL pin is set to logic high, then the internal reference is enabled and selected.

If the REFSEL pin is set to logic low, then the internal reference circuit is disabled and powered down. In this mode, an external reference voltage must be provided to the REFIN/REFOUT pin.

The internal reference buffer is always enabled under both conditions.

The reference mode after power-up depends on the state of the REFSEL input pin.

RANGE (Input)

The RANGE pin selects the input range for all analog input channels.

If this pin is set to logic high, the device is configured to operate in the ±10-V input range.

If this pin is set to logic low, the device is configured to operate in the ±5-V input range.

The RANGE pin is also used to put the device in standby or shutdown mode depending on the state of the STBY input pin, as explained in the Power Down Modes.

$\overline{\text{STBY}}$ (Input)

The $\overline{\text{STBY}}$ pin puts the device into one of the two power-down modes: standby and power down.

If this pin is set to logic high, the device is in normal operation mode.

If this pin is set to logic low, the device is in the standby or power down mode, depending on the state of the RANGE pin.

In the shutdown mode, all internal circuitry is powered down,

In the standby mode, the internal reference remains powered up to enable a relatively quicker recovery to normal operation mode.

$\overline{\text{PAR}}$/SER/BYTE SEL (Input)

The $\overline{\text{PAR}}$/SER/BYTE SEL pin selects between the parallel, serial, and parallel byte interface modes for reading data from the device.

If this pin is set to logic high, then the serial or parallel byte interface mode is selected depending on the state of the DB15/BYTE SEL pin. If the DB15/BYTE SEL pin is high, the parallel byte interface is selected, and if the DB15/BYTE SEL is low, then the serial mode is selected.

CONVSTA, CONVSTB (Input)

CONVSTA, and CONVSTB (Input) are conversion control input pins.

CONVSTA can be used to simultaneously sample and initiate the conversion process for the first half count of the input channels (channels 1-4), and CONVSTB can be used to simultaneously sample and initiate the conversion process for the latter half count of the input channels (channels 5-8).

On the rising edge of the CONVSTA, CONVSTB signals, the internal track-and-hold circuits for each analog input channel are placed into the hold mode and the sampled input signal is converted.

The CONVSTA, and CONVSTB signals can be pulled low when the internal conversion is over, as indicated by the BUSY signal. At this point, the front-end circuit for all analog input channels acquires the respective input signals and the internal ADC is not converting.

The output data can be read from the device irrespective of the status of the CONVSTA and CONVSTB pins.

RESET (Input)

The RESET pin can be used to reset the device at any time in an asynchronous manner. When the RESET pin is set to logic high, the device is in the reset mode and remains in the state until the pin returns low.

The device should be reset after power-up or recovery from the shut down mode when all the supplies and references have settled to the required accuracy.

$\overline{\text{RD}}$/SCLK (Input)

$\overline{\text{RD}}$/SCLK (Input) is a dual-function pin to be used in different interface modes.

Device Operating Condition		Functionality of $\overline{RD}$/SCLK(Input)
Parallel Interface	$\overline{PAR}$/SER/BYTR SEL = 0 DB15/BYTE = 0	The active-low digital input pin to read the output data from the device. In the parallel or parallel byte interface mode, the output bus is enabled when both the CS and RD inputs are tied to a logic-low input.
Parallel Byte Interface	$\overline{PAR}$/SER/BYTR SEL = 1 DB15/BYTE = 1	
Serial Interface	$\overline{PAR}$/SER/BYTR SEL = 1 DB15/BYTE = 0	The external clock input for the serial data interface. In the serial mode, all synchronous accesses to the device are timed with respect to the rising edge of the SCLK signal.

$\overline{CS}$ (Input)

The $\overline{CS}$ pin is an active-low, chip-select signal.

A rising edge on the $\overline{CS}$ signal outputs all the data lines in tri-state mode.

A falling edge of the $\overline{CS}$ signal marks the beginning of the output data transfer frame in any interface mode of operation for the device.

OS [2:0]

The OS [2:0] pins are active-high digital input pins used to configure the oversampling ratio for the internal digital filter on the device.

When OS [2:0] = 111, a higher filter bandwidth of ~30 kHz is selected.

Device Modes of Operation

Power Down Modes

The device supports two power-down modes: standby mode and shutdown mode. The device can enter either power-down mode by pulling the $\overline{STBY}$ pin to a logic level. Additionally, the selection between these two power-down modes is done by the state of the RANGE pin.

Power Down Mode	$\overline{STBY}$	Range
Standby	0	1
Shutdown	0	0

Standby Mode

In the standby mode, only the internal reference of the circuit is powered up, and the analog front-end, signal-conditioning circuit for each channel remains powered down.

Shutdown Mode

In the shutdown mode, the entire internal circuitry is powered down.

Conversion Control

The device offers precise control of simultaneously sampling all analog input channels.

Simultaneous Sampling on All Input Channels

All the analog input channels are to be simultaneously sampled by connecting CONVSTA and CONVSTB signals together, and a single CONVST signal should be used to control the sampling of all analog input channels of the device.

Simultaneous Sampling Two Sets of Input Channels

Two sets of analog input channels can be simultaneously sampled by separating CONVSTA and CONVSTB signals. And the device could not operate in oversampling mode in this state.

Data read operation

The device updates the internal data registers with the conversion data for all analog channels at the end of every conversion phase (when BUSY goes low).

If the output data are read after BUSY goes low, then the device outputs the conversion results for the current sample.

If the output data are read when BUSY is high, then the device outputs conversion results for the previous sample.

There are three interface modes:

Interface mode	$\overline{\text{PAR}}$/SER/BYTE SEL	DB15/BYTE SEL
Parallel Interface	0	0
Parallel Byte Interface	1	1
Serial Interface	1	0

Parallel Data Read

The device supports a parallel interface mode for reading the output data of the device using the control inputs ($\overline{\text{CS}}$ and $\overline{\text{RD}}$), the parallel output bus (DB [15:0]), and the BUSY indicator.

For applications that use only one device in the system and do not share the parallel output bus with any other devices, the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ input signals can be tied together, or the $\overline{\text{CS}}$ signal can be permanently tied low. At the first falling edge of the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signal, the output data of channel 1 becomes available on the parallel bus to be read by the digital host. At this instant, the FRSTDATA output also goes high, indicating channel 1 data is ready to be read back. The output data for the remaining channels are clocked out on the parallel bus on subsequent falling edges of the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signal in a sequential manner.

For applications that use multiple devices in the system, the CS and RD input signals must be driven separately.

Parallel Byte Data Read

The parallel byte interface mode is very similar to the parallel interface mode, except that the output data for each channel is read in two data transfers of 8-bit byte sizes.

In the parallel byte mode, the DB14/HBEN pin decides the order of the most significant byte (MSB byte) and the least significant byte (LSB byte). When the DB14/HBEN pin is tied high, the MSB byte of the conversion results is output first followed by the LSB byte. This order is reversed when DB14/HBEN is tied to logic low.

At the first falling edge of the $\overline{\text{RD}}$ signal, the first byte of the channel 1 conversion result becomes available on DB [7:0]. This byte is followed by the second byte of conversion data on the next falling edge of the RD signal.

Serial Data Read

This interface mode uses a CS control input, a communication clock input (SCLK), BUSY and FRSTDATA output indicators, and serial data output lines DOUTA and DOUTB.

A total of 16 SCLK cycles are required to clock out 16 bits of conversion result for each channel and the same process can be repeated for the remaining channels in an ascending order.

The conversion results from the first set of channels appear first on DOUTA, followed by the second set of channels if only DOUTA is used for reading data. This order is reversed for DOUTB, in which the second set of channels appear first followed by the first set of channels. The use of both data output lines reduces the time needed for data retrieval and a higher throughput can therefore be achieved in this mode.

Data Read During Conversion

The device allows data read when the ADC is converting and the BUSY output is high status. In this case, the ADC outputs conversion results for previous samples.

The data read back during conversion mode allows faster throughput to be achieved from the device.

Data Read During Conversion

The device can be configured in the oversampling mode by the OS [2:0] pins. The input on the OS pins is latched on the falling edge of the BUSY signal to configure the oversampling rate for the next conversion.

In this mode, the CONVST A and CONVST B signals should be tied or driven together.

The BUSY signal duration varies with the OSR setting because the conversion time increases with the OSR setting.

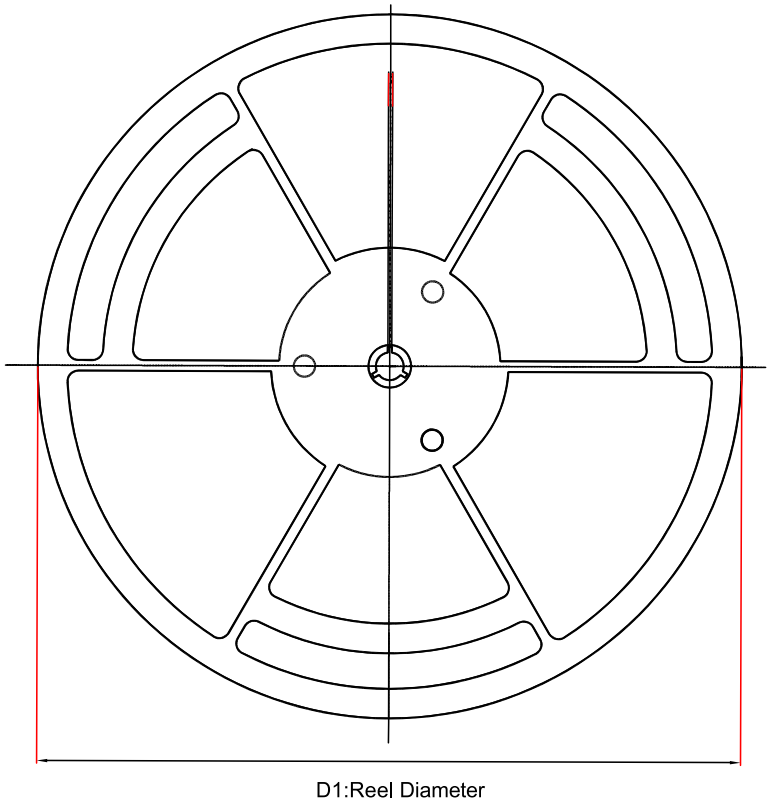
Oversampling the input signal reduces noise during the conversion process, thus reducing the histogram code spread for a DC input signal to the ADC.

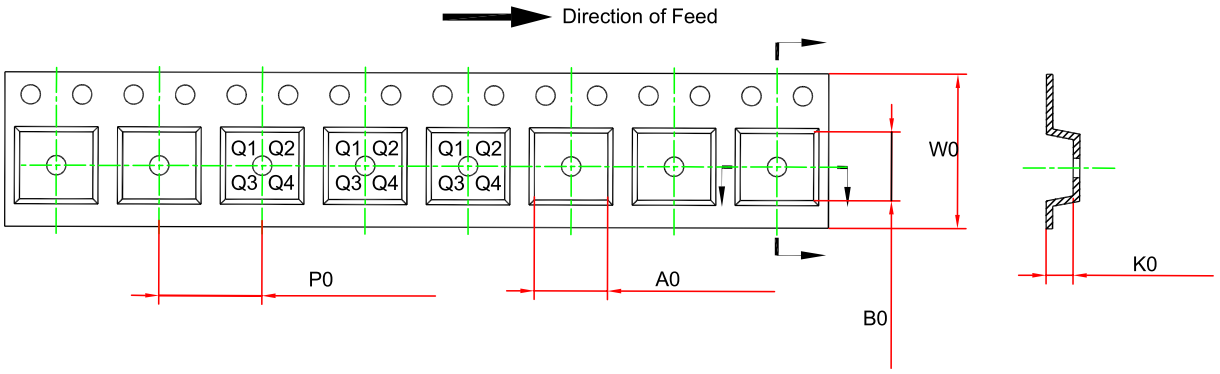
Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Tape and Reel Information



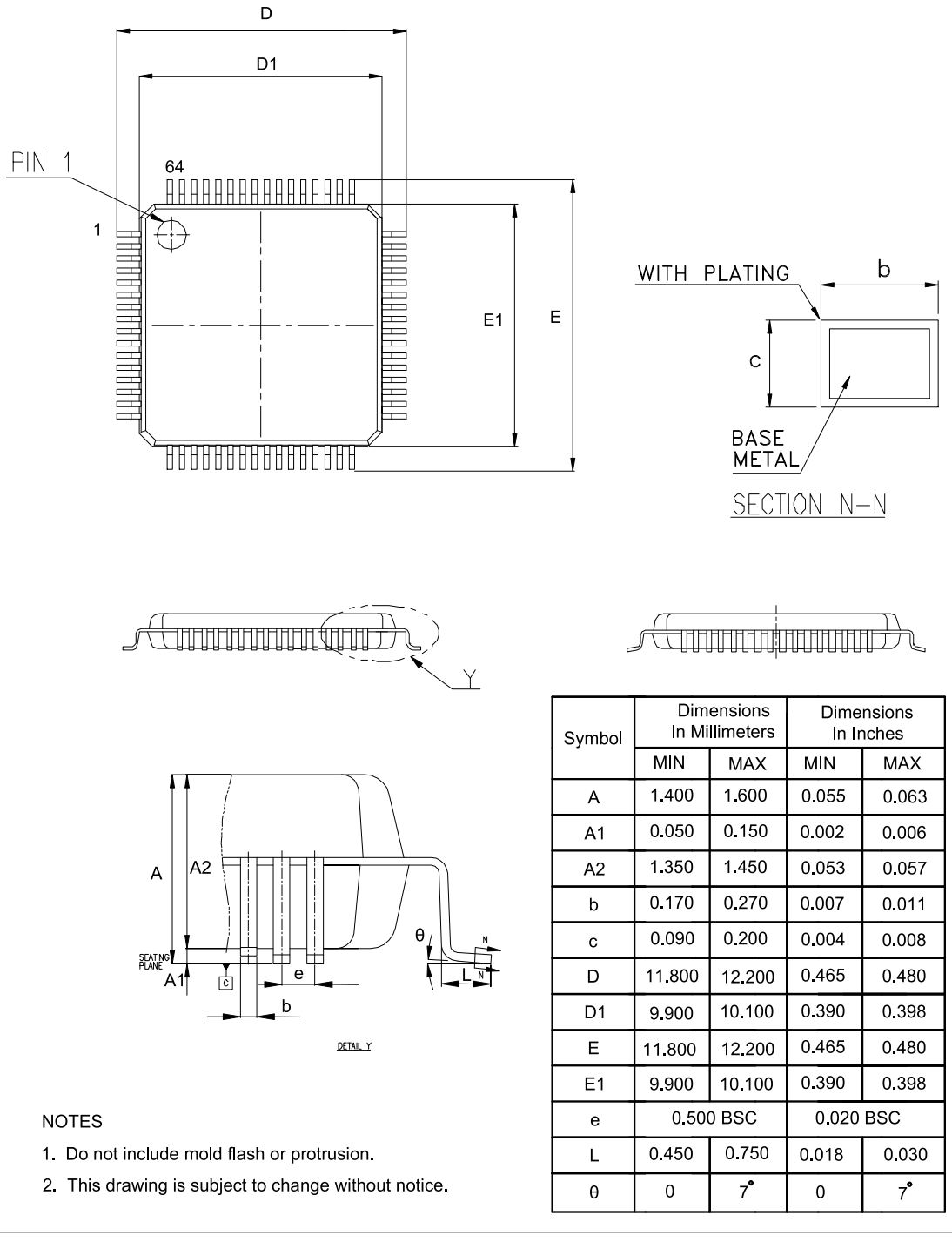


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPAFE5160SI08-QP7R	LQFP10×10-64	330	28.4	12.085	12.085	2.1	16	24	Q2

Package Outline Dimensions

LQFP10x10-64

Package Outline Dimensions QP5(LQFP10X10-64-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.400	1.600	0.055	0.063
A1	0.050	0.150	0.002	0.006
A2	1.350	1.450	0.053	0.057
b	0.170	0.270	0.007	0.011
c	0.090	0.200	0.004	0.008
D	11.800	12.200	0.465	0.480
D1	9.900	10.100	0.390	0.398
E	11.800	12.200	0.465	0.480
E1	9.900	10.100	0.390	0.398
e	0.500 BSC		0.020 BSC	
L	0.450	0.750	0.018	0.030
θ	0	7°	0	7°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPAFE5160SI08-QP7R	−40 to 125°C	LQFP10×10-64	AFE5160	3	Tape and Reel, 1000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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