8-Channel Configurable ADC/DAC with I²C interface

Features

- 8-channel, configurable ADC/DAC/GPIO
- 8 12-bit DAC channels
- 8 12-bit ADC channels
- 8 general-purpose I/O pins
- Integrated temperature sensor
- 16-lead MIS 3x3 and 16-ball WLCSP 2x2 package
- I²C interface

Applications

- General-purpose analog and digital I/O
- Multi channels Control and monitor

Description

The TPAFE0808 has eight input/output pins, which can be configured to be ADC input, or DAC output, or General purpose I/O pins.

A 12bit ADC is integrated in TPAFE0808, which can be connected to each input/output pin by an eight–channel multiplexer. The ADC input range is 0~VREF or 0~2*VREF.

TPAFE0808 has eight channel 12bit DAC, which can be connected to corresponding input/output pin. The DAC output range is 0~VREF or 0~2*VREF.

TPAFE0808 has an internal 2.5V reference, and it can also use external reference when internal reference is turned off.

It also has an internal temperature sensor which can measure die temperature.

The TPAFE0808 is available in 16-lead MIS 3x3, as well as a 16-ball WLCSP, and operates over a temperature range of −40°C to +125°C.

Function Block Diagram

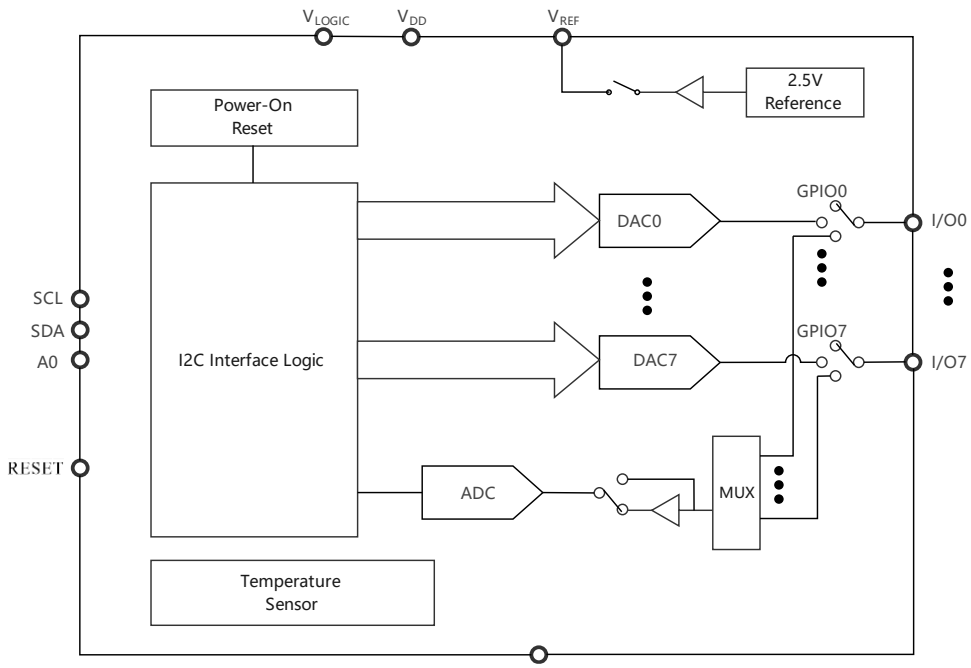

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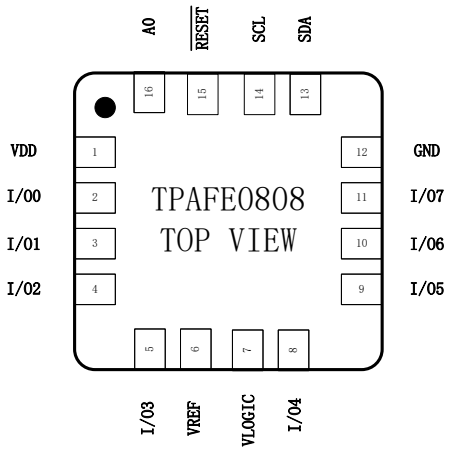
Table of Contents

Revision History

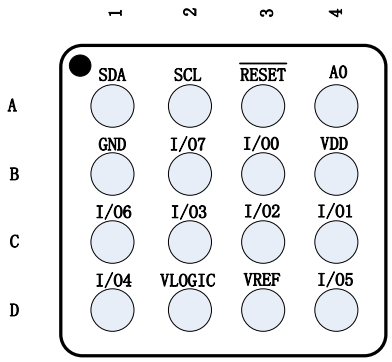
Date	Revision	Notes
2020/8/2	Rev.A.1	1.0 Version
2020/9/11	Rev.A.2	Refine parameters, and update register definition details
2021/1/19	Rev.A.3	Update serial interface diagram
2021/5/20	Rev.A.4	Update Product description and diagram.
2021/7/22	Rev.A.5	Update t3 tLOW Max limit
2022/7/28	Rev.A.6	Update tape and reel information

Pin Configuration and Functions

MIS3X3-16L Configuration



WLCSP 2x2-16L (Top View, Ball side down)



Pin Functions

Pin No.		Pin Name	Description
MIS3X3-16L	WLCSP 2x2-16L		
1	B4	VDD	Power Supply Input.
2 to 5, 8 to 11	B3, C4, C3, C2, D1, D4, C1, B2	I/O0 to I/O7	Input/Output pin. These pins can be configured as DACs, ADCs, or GPIO independently.
6	D3	VREF	Reference Input/Output. When the internal reference is enabled, the 2.5 V voltage is available on the pin. When the internal reference is disabled, an external reference should be used and connected to the pin.
7	D2	VLOGIC	Digital interface Power Supply.
12	B1	GND	Ground.
13	A1	SDA	Serial Data Line. This pin is open drain input/output.
14	A2	SCL	Serial Clock Line. This pin is open drain input.
15	A3	/RESET	Reset Pin. Low effective. When this pin is tied low, the chip is reset to default condition.
16	A4	A0	Address pin. It can be connected to GND or VLOGIC. It sets LSB of I²C address.

Specifications

Absolute Maximum Ratings(1)

Parameter	Rating
VDD to GND	−0.3 V to +7 V
VLOGIC to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to VDD + 0.3 V
Digital Input Voltage to GND	−0.3 V to VLOGIC + 0.3 V
Digital Output Voltage to GND	−0.3 V to VLOGIC +0.3 V
VREF to GND	−0.3 V to VDD +0.3 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	+150°C

Note (1): Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	6	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	1.5	kV

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
MIS3X3-16L	100.1	37.4	°C/W
WLCSP 2x2-16L	70	28.6	°C/W

Electrical Characteristics

VDD = 2.7 V to 5.5 V, VREF = 2.5 V (internal), $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
ADC DC SPECIFICATIONS[1]					
Resolution		12			bit
Full scale input range		0		2xVREF	V
		0		VREF	V
INL				±2	LSB
DNL				±1	LSB
Offset error				±5	mV
Offset error temperature drift			10		uV/°C
Gain error				±0.3	%FSR
Gain error temperature drift			±20		ppm/°C
Conversion time			2		us
Acquisition time	500K SPS conversion rate	500			ns
Signal-Noise Ratio			60		dB
Total Harmonic Distortion			80		dB
SFDR			80		dB
Channel to channel isolation			-70		dB
Full Power bandwidth			8		MHz
Input buffer dead band	from 0 or from VCC		20	40	mV
DAC DC SPECIFICATIONS[1]					
Resolution		12			bit
Full-scale output voltage range	power up or reset through auto-range detection	0		5	V
INL				±3	LSB
DNL				±1	LSB
Offset error	End point fit between codes 16 to 4031. DAC outputs unloaded.		±2	±15	mv
Offset error temperature drift	Mid scale output		8		uV/°C
Gain error	full temp		±0.1	±0.5	%FSR
Gain error temperature drift			±20		ppm/°C
Zero-scale error	Code=000h full temp		4	10	mv
Zero-scale error temperature drift			±2		uV/°C
Load current 1	Middle code, drop out=2 mV, sink or source	10			mA
Load current 2	VDD=3.45 V, drop out=0.45 V, sink or source	11			mA

Electrical Characteristics (Continued)

VDD = 2.7 V to 5.5 V, VREF = 2.5 V (internal), $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Parameter	Test conditions	Min	Typ	Max	Unit
Short circuit current	Normal mode(default)		25		mA
Capacitive load stability	RL = ∞			1	nf
Output voltage settling time	1/4 to 3/4 scale settling to ±0.5 LSB. RL=2 kΩ, Cl=200 pf		10		μs
Slew rate	Transition: 1/4 to 3/4 scale, 10% to 90%.RL=2 kΩ, Cl=200 pf		0.5		V/μs
Output noise	0.1 Hz to 10 Hz, DAC code at mid-scale		200		μVpp
Output noise density	10 kHz, DAC code at mid-scale		700		nV/√Hz
DAC enable overshoot			50		mV
DAC enable time			100		uS
DAC Glitch			20		nV*S
Temperature sensor					
Accuracy			±3		°C
Update time			45		ms
Reference voltage					
Internal reference voltage		2.49	2.5	2.51	V
Internal reference temperature coefficient			20		ppm/°C
Capacitive load stability		0.1		1	uF
Load regulation	No load ability		NA		
GPIO					
Voh	ISOURCE = 1 mA	VDD − 0.2			V
Vol	Isink = 1 mA			0.4	V
Vih		VDD*0.7			V
Vil				VDD*0.3	V
Hysteresis			0.2		V
Logic input					
Vih		VLOGIC*0.7			V
Vil				VLOGIC*0.3	V
Logic output					
Output High Voltage, VOH	ISOURCE = 200 μA; VDD = 2.7 V to 5.5 V	VLOGIC − 0.2			V
Output Low Voltage, VOL	ISINK = 200 μA			0.4	V

Electrical Characteristics (Continued)

VDD = 2.7 V to 5.5 V, VREF = 2.5 V (internal), $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	UNIT
Power	VCC = 3 V, ADC enabled, internal reference @500 kHz		2.15	3.5	mA
	VCC = 3 V, ADC enabled, external reference @500 kHz		1.85	3	mA
	VCC = 3 V, DAC enabled		2.9	4.5	mA
	VCC = 3 V， ADC + DAC + Bg		4.5	7	mA
	VCC = 3 V， ADC + DAC + Bg + temperature sensor		5	7.5	mA
Tready	Ready time after hardware reset		1	2	ms

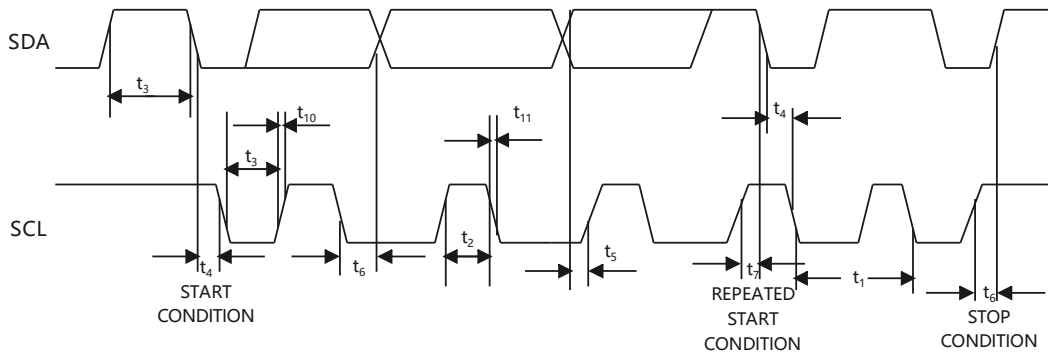
Timing Characteristics (1)

VDD = 2.7 V to 5.5 V, VREF = 2.5 V (internal), $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Parameter	Min	Typ	Max	Unit	Conditions/Comments
tscl	2.5			μs	SCL cycle time
t_2 t_{HIGH}	0.6			μs	SCL high time
t_3 t_{LOW}	1.3		13000	μs	SCL low time
t_4 $t_{HD,STA}$ (2)	0.6			μs	start and restart condition hold time
t_5 $t_{SU,DAT}$	100			ns	data setup time
t_6 $t_{HD,DAT}$			0.9	μs	data hold time
t_7 $t_{SU,STA}$	0.6			μs	setup time for repeated start
t_8 $t_{SU,STO}$	0.6			μs	stop condition setup time
t_9 t_{BUF}	1.3			μs	bus free time between stop and start
t_{10} t_R			300	ns	Data and clock rise time
t_{11} t_F			250	ns	Data and clock fall time

Note (1): Specified by design and characterization.
Note (2): If this hold time is < 10nS, a start condition maybe recognized.

Timing Diagram



Typical Performance Characteristics

VDD = 2.7 V to 5.5 V, VREF = 2.5 V (internal), $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

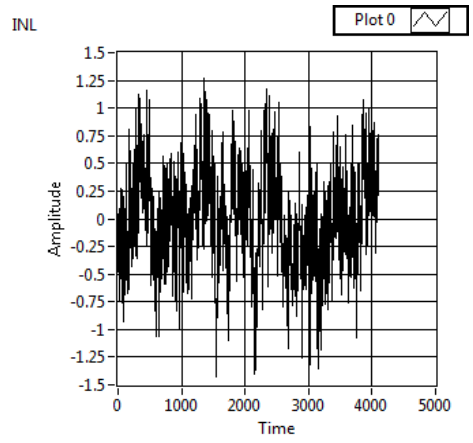


Figure 1. ADC INL

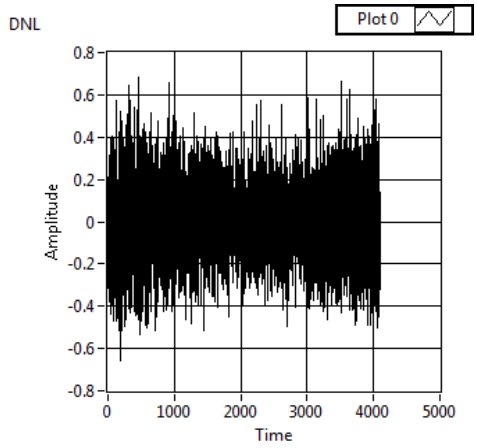


Figure 2. ADC DNL

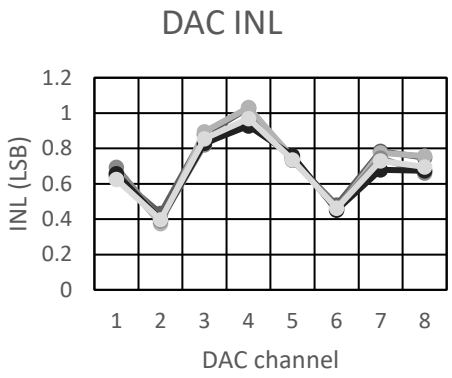


Figure 3 DAC INL

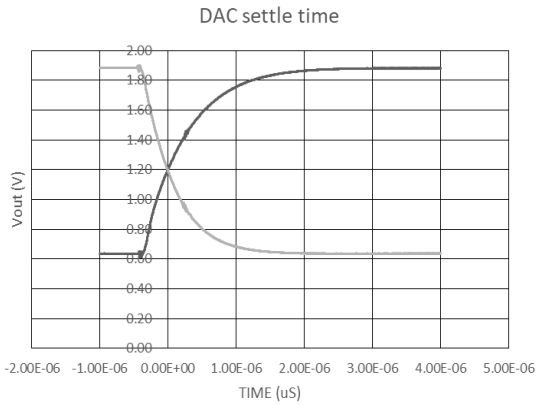


Figure 4 DAC settling time, output range = 0~Vref

Detail Description

Register Map

Table 1 Pointer Byte Configuration

D7	D6	D5	D4	D3	D2	D1	D0
Mode bits				Mode dependent data bits			

Table 2 Mode Bits

D7	D6	D5	D4	Description
0	0	0	0	Configuration mode
0	0	0	1	DAC write
0	1	0	0	ADC readback
0	1	0	1	DAC readback
0	1	1	0	GPIO readback
0	1	1	1	Register readback

Table 3 Configuration register table

Pointer Byte	R/W	Default Value	Register Name	Description
8'h00	R/W	16'h0000	NO	No operation is available
8'h02	R/W	16'h0000	ADC sequence	Selects ADC sequence
8'h03	R/W	16'h0000	ADC DAC general configuration	ADC and DAC configuration
8'h04	R/W	16'h0000	ADC selection	Selects ADC channels
8'h05	R/W	16'h0000	DAC selection	Selects DAC channels
8'h06	R/W	16'h00ff	Pull down selection	Selects which pins have 85 kΩ pull down resistor
8'h07	R/W	16'h0000	LDAC control	Selects load DAC operation
8'h08	R/W	16'h0000	GPIO write selection	Selects general purpose outputs
8'h09	R/W	16'h0000	GPIO write data	Writes data to general purpose outputs
8'h0a	R/W	16'h0000	GPIO read selection	Selects general purpose inputs
8'h0b	R/W	16'h0000	Power down control	Powers down control of the ADC, DAC and reference
8'h0c	R/W	16'h0000	Open drain configuration	open drain or push pull control for general purpose outputs
8'h0d	R/W	16'h0000	Three state selection	Selects three stated output
8'h0f	R/W	16'h0000	Software reset	Resets the chip
8'h7e	R	16'h0808	Chip ID	Chip ID for readback

Register Explanations

Table 4 ADC Sequence

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Reserved						REP	TEMP	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0

Table 5 ADC Sequence Descriptions

Bits	Description
D15 to D10	Reserved, set to 0.
D9	REP: sequence repeat 0 = disable repetition (default) 1 = enable repetition
D8	Temperature selection 0 = disable temperature read back 1 = enable temperature read back
D7 to D0	1 = includes corresponding ADC in conversion sequence 0 (default) = not selected in conversion sequence

Table 6 ADC DAC general configuration

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Reserved						Pre-charge	ADC Buffer	GPIO Lock	DAC write all	ADC range	DAC range	Reserved			

Table 7 ADC DAC general configuration Descriptions

Bits	Description
D15 to D10	Reserved. Set these bits to 0.
D9	Precharge. 0: No ADC precharge function(default). The ADC buffer is always powered up if it is enabled. 1: ADC buffer is used to precharge the sampling cap and then powered down until next conversion.
D8	ADC buffer 0: the ADC buffer is disabled (default). 1: the ADC buffer is enabled.
D7	GPIO Lock 0: the IO selection registers can be changed (default). 1: the IO selection registers cannot be changed.
D6	DAC write all 0: DAC value is written to DAC channels according to DAC address bits. 1: all DACs channels are updated with the same data.
D5	ADC range. 0: 0 to V_{REF} (default). 1: 0 to 2 × V_{REF}.
D4	DAC range. 0: 0 to V_{REF} (default). 1: 0 to 2 × V_{REF}.
D3 to D0	Reserved;

Table 8 LDAC Control

D1	D0	Description
0	0	Data written to input register is copied into DAC register, and the DAC output is also updated (default).
0	1	Data written to an input register is not copied to DAC register, and the DAC output is also not updated.
1	0	Data in the input registers are copied to the DAC registers, and the DAC outputs are updated simultaneously. The LDAC control bits returns to 01 after the operation is done.
1	1	Reserved.

Table 9 DAC Pointer Byte Address

DAC Address	D7	D6	D5	D4	D3	D2	D1	D0
DAC0	0	0	0	1	0	0	0	0
DAC1	0	0	0	1	0	0	0	1
DAC2	0	0	0	1	0	0	1	0
DAC3	0	0	0	1	0	0	1	1
DAC4	0	0	0	1	0	1	0	0
DAC5	0	0	0	1	0	1	0	1
DAC6	0	0	0	1	0	1	1	0
DAC7	0	0	0	1	0	1	1	1

Table 10 DAC Data

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	DAC address			12-bit DAC data											

Table 11 ADC Data

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	ADC address			12-bit ADC data											

Table 12 GPIO Write selection

Bits	Description
D15 to D8	Reserved;
D7 to D0	GPIO output selection 1: set to be output pin 0: determined by pin selection registers (default)

Table 13 Open-Drain Configuration

Bits	Description
D15 to D8	Reserved
D7 to D0	GPIO output Open-drain selection 1: open drain output 0: push/pull output (default)

Table 14 GPIO Write Data

Bits	Description
D15 to D8	Reserved
D7 to D0	1: Set GPIO output to 1. 0: Set GPIO output to 0

Table 15 Three-State selection

Bits	Description
D15 to D8	Reserved
D7 to D0	Set pins as three-state outputs 1: set GPIO to three-state output 0: determined by pin selection registers (default)

Table 16 Pull-Down Selection

Bits	Description
D15 to D8	Reserved
D7 to D0	Set pins as weak pull-down outputs 1: pulled down by 85 kΩ pull-down resistor 0: determined by pin selection registers (default)

Table 17 Power-Down Register

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	PD_ALL	EN_REF	0	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Table 18 LDAC Mode Register Descriptions

Bits	Bit Name	Description
D15 to D11	Reserved	Reserved
D10	PD_ALL	0 = Determined by D0~D9 (default). 1 = all analog blocks are powered down.(REF, ADC, DAC)
D9	EN_REF	0 = Internal Reference is powered down (default). 1 = Internal reference is powered up and available on the V_{REF} pin.
D7 to D0	PD7 to PD0	0 = the channel is in operating mode (default). 1 = the channel is powered down if it is selected as DAC.

Feature Description

The TPAFE0808 has eight input/output pins, which can be configured to be ADC input, or DAC output, or General purpose I/O pins.

DAC SECTION

TPAFE0808 has eight channel 12bit DACs, which can be connected to corresponding input/output pin. Each channel has a resistor-string DAC with output buffer. Following is the DAC diagram:

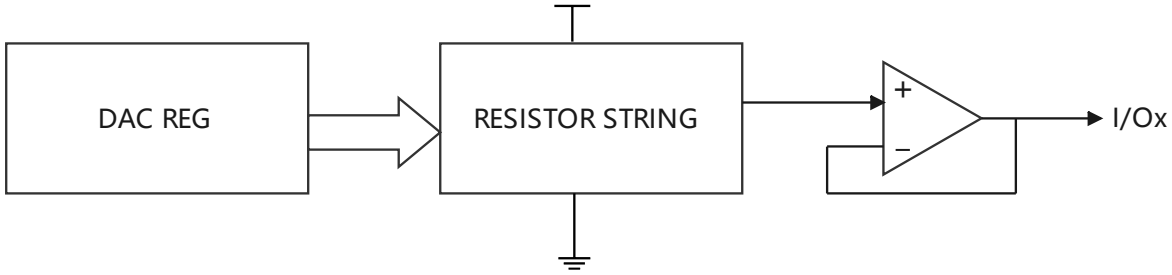


Figure 5 DAC architecture

The DAC range is 0 V to V_{REF} or 0 V to 2 × V_{REF}, controlled by DAC Range bit.

The output voltage is:

$$V_{OUT} = V_{REF} \times \frac{D}{2^{12}} \quad \text{or} \quad V_{OUT} = 2 \times V_{REF} \times \frac{D}{2^{12}}$$

Where V_{REF} is the 2.5V internal reference or external reference voltage,

D is the DAC register value.

ADC SECTION

TPAFE0808 has a 12-bit ADC, which can be connected to each I/O pin by a multiplexer. The conversion time is 2 μs. And the ADC can scan selected channels automatically by setting the selection register.

ADC input range is 0 V to VREF or 0 V to 2 × VREF, controlled by the ADC range bit. All input channels share the same range.

The input/output pin can be set to be both ADC and DAC. In this case, the DAC output voltage can be monitored by ADC.

Following figure shows the ADC input structure:

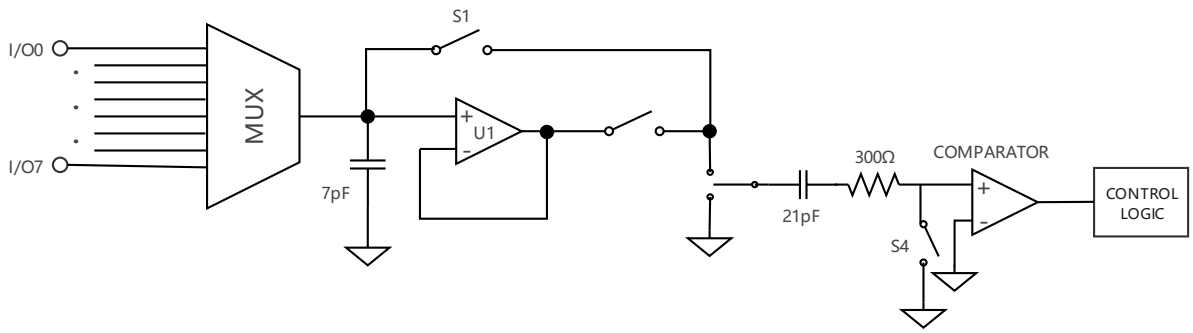


Figure 6 ADC input structure

The current flowing into the ADC input pins varies with sampling rate and differential voltage. It can be calculated as follows:

$f_S \times C \times V_{DIFF}$

where: f_S is the ADC sample rate.

C is the sampling capacitance (7 pf in buffer mode, 7+21=28 pf in un-buffered mode)

V_{DIFF} is the voltage difference between successive channels.

For example:

f_S = 10 kHz, previous ADC input is 0.5 V, and current ADC input is 2 V, the ADC input current in unbuffered mode is as follows:

$(10{,}000 \times 28 \times 10^{-12} \times 1.5) = 420$ nA

GPIO SECTION

By controlling the GPIO selection register, each of the eight input/output pins can be configured as digital input or output pin. general-purpose digital input or output pin by programming the GPIO control register. Logic levels for general-purpose outputs are relative to V_{DD} and GND.

INTERNAL REFERENCE

The TPAFE0808 has an internal 2.5 V reference. The reference is powered down by default. When the reference is powered down, an external reference must be connected to V_{REF}.

When the internal reference is powered up, it appears on the V_{REF} pin， but can not be used as a reference source for other components. When the internal reference is used, it is recommended to not decoupled between V_{REF} to GND, or using a capacitor >=100 nf.

RESET FUNCTION

The TPAFE0808 has two reset functions, hardware reset by RESET pin and software reset by writing to specific register 0x0F.

A falling edge on RESET resets all registers to default values, and input/output pins are set to status with 85 kΩ pull-down resistor to GND. The reset function takes 250 µs maximum; do not write new data to the TPAFE0808 during this time.

The TPAFE0808 has a software reset function, by writing 0x0F to pointer byte and 0x0D and 0xAC to MSB and LSB. Software reset function performs the same as the RESET pin.

TEMPERATURE INDICATOR

The TPAFE0808 contains an integrated temperature to monitor die temperature. The temperature can be calculated as follows:

$$\text{Temp} = \frac{ADC\ Code - 1024}{16}$$

The range of codes returned by the ADC when reading from the temperature indicator is approximately 384 to 3024.

SERIAL INTERFACE

The TPAFE0808 has a 2-wire, I²C-compatible serial interface. It supports standard mode (100 kHz) and fast mode (400 kHz). The six MSBs of the 7-bit slave address is 001000, and the LSB is set by state of A0 pin.

The 2-wire serial bus protocol operates as follows:

I2C Write

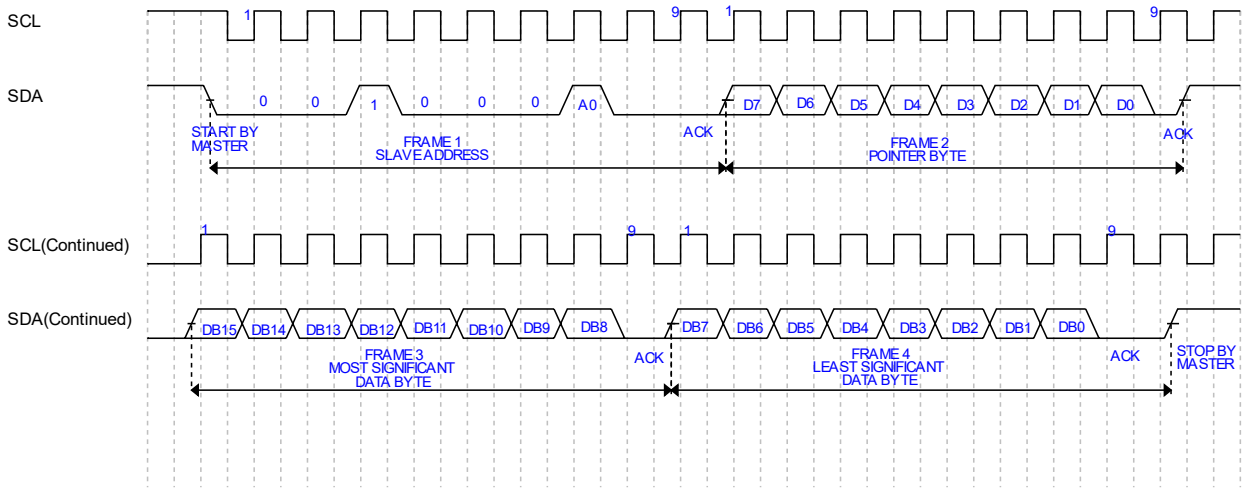


Figure 7 I²C Write

I²C Read

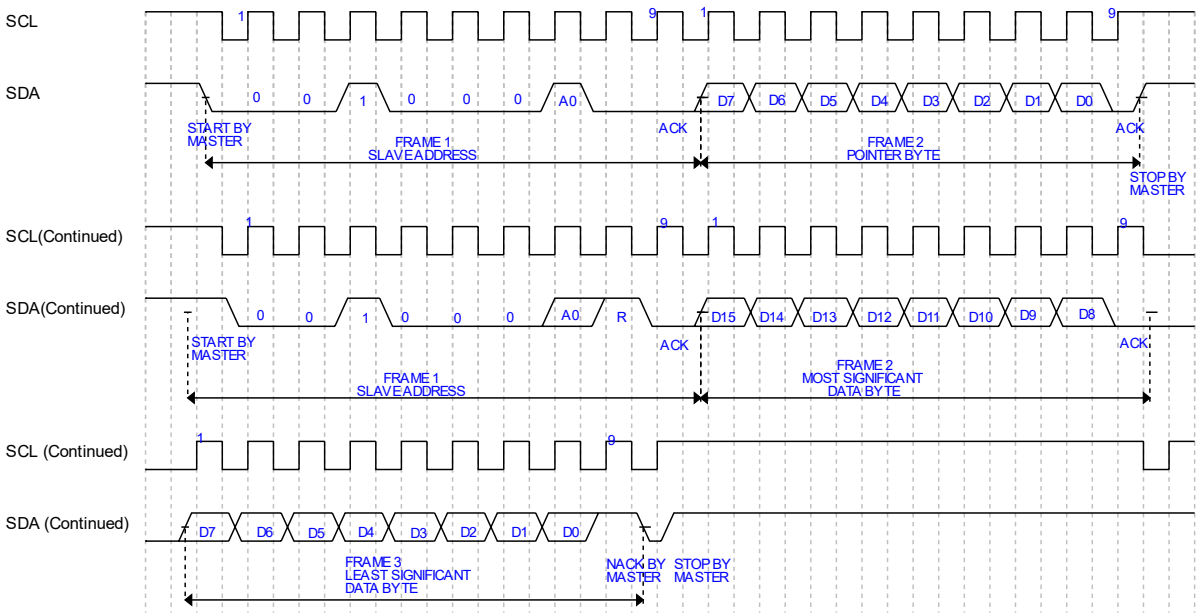


Figure 8 Read one 16-bit word

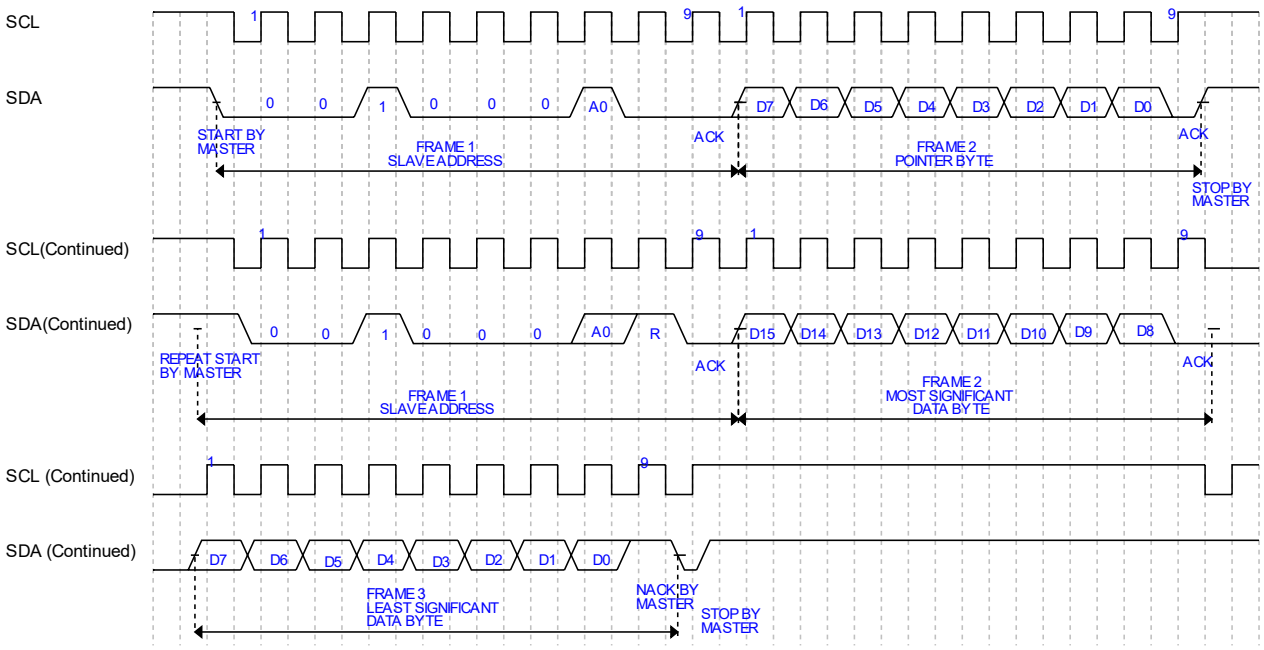


Figure 9 Read one 16-bit word, maintain control of the bus

I²C Block Read

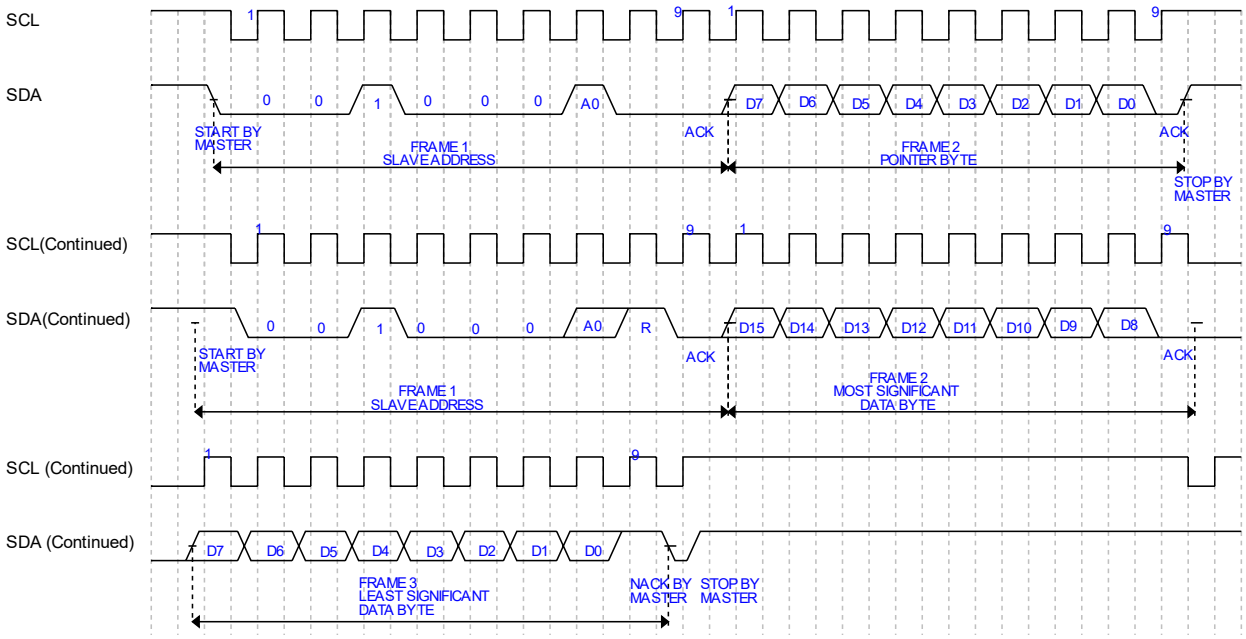


Figure 10 I²C block read

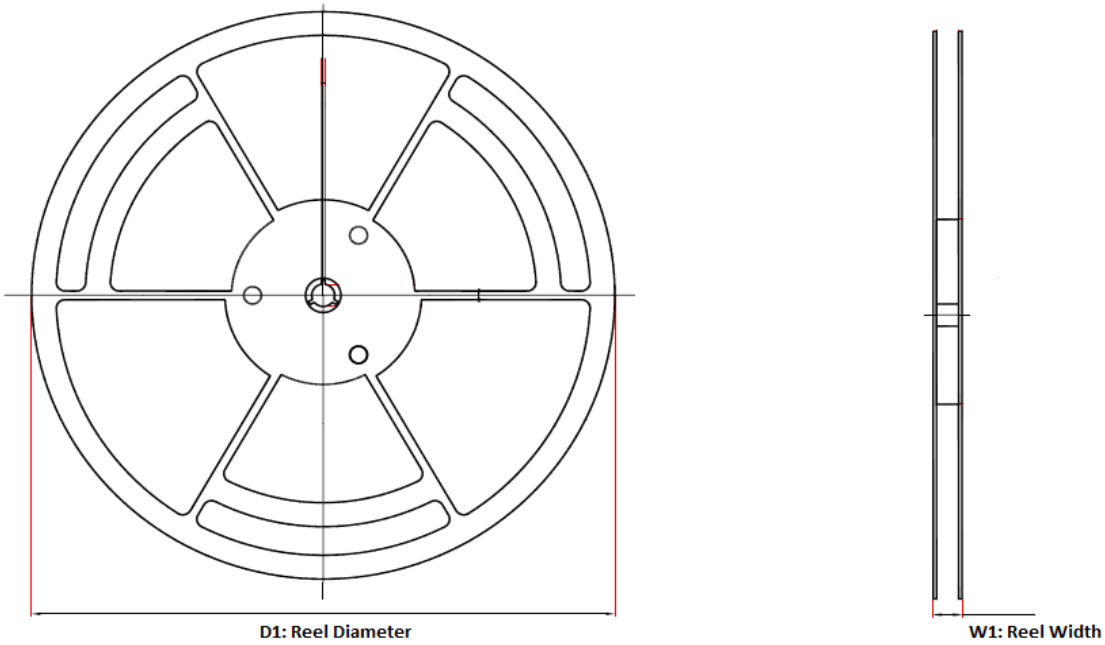
Application Information

NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

1. When internal reference is used, at least 100 nf capacitor should be added as filter cap. And resistive loading should not be connected to reference pin.
2. If one input/output pin is used as DAC function, don't toggle it between DAC mode and GPIO mode.
3. No special power up sequence is required.

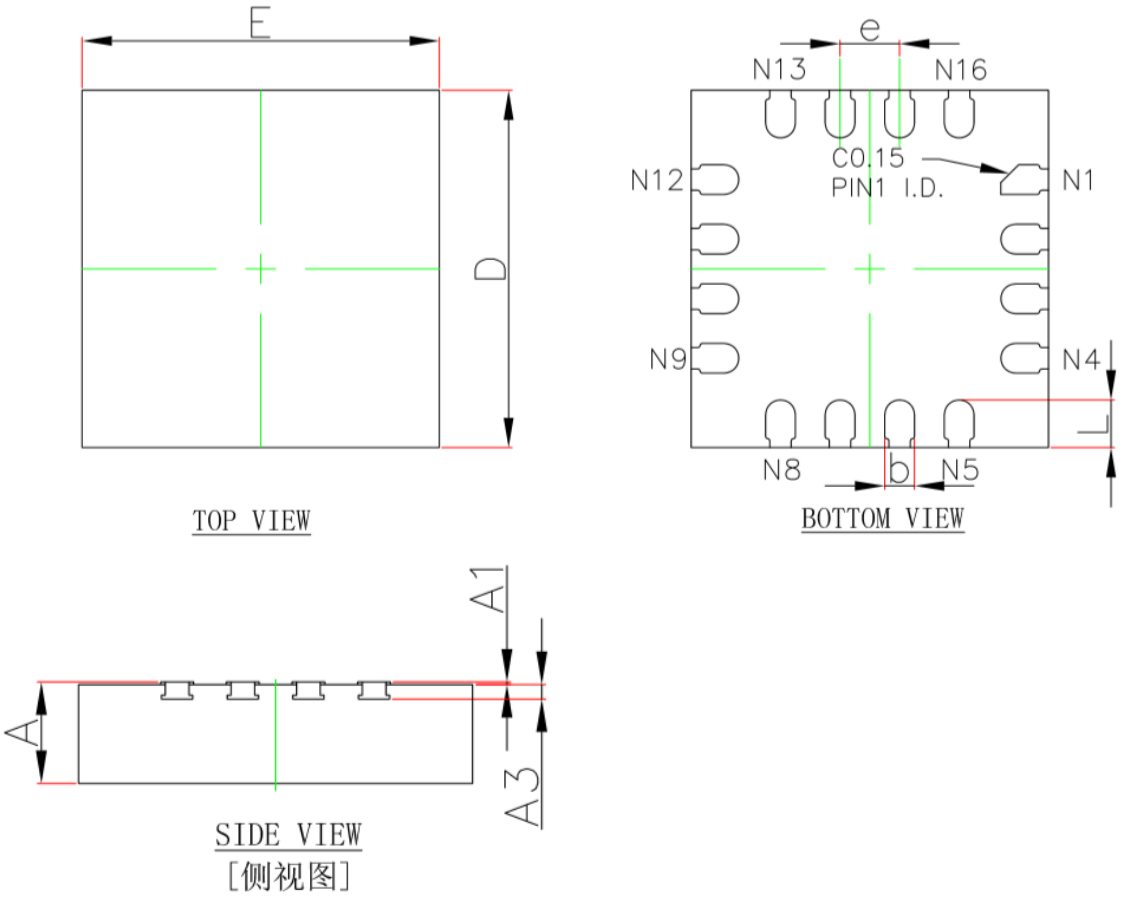
Tape and Reel Information



Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPAFEA008-WLPR	WLCSP	178	12.5	2.24	2.24	0.75	4	8	Q2
TPAFE0808-LFPR-S	MIS3X3-16L	330	17.6	3.3	3.3	1	8	12	Q2

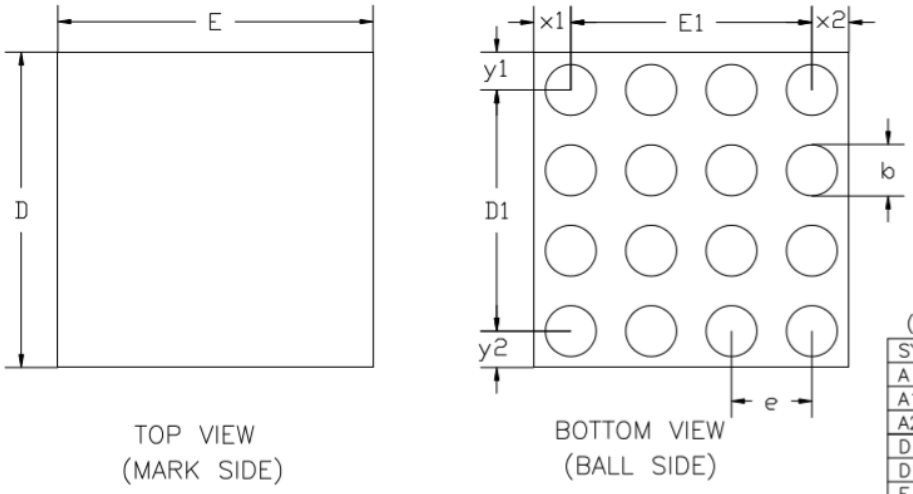
Package Outline Dimensions

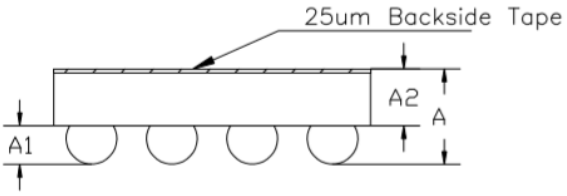
MIS3X3-16L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	-0.004	0.046	0.000	0.002
A3	0.110REF.		0.004REF.	
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
b	0.200	0.300	0.008	0.012
e	0.500BSC.		0.020BSC.	
L	0.300	0.500	0.012	0.020

WLCSP 2x2-16L





COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.550	0.595	0.640
A1	0.220	0.240	0.260
A2	0.330	0.355	0.380
D	1.930	1.960	1.990
D1		1.500BSC	
E	1.930	1.960	1.990
E1		1.500BSC	
b	0.300	0.320	0.340
e		0.500BSC	
x1		0.22875 REF	
x2		0.23125 REF	
y1		0.2325 REF	
y2		0.2275 REF	

NOTES:
ALL WAFER ORIENTATION NOTCH DOWN

Order Information

Order Number	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPAFE0808-LFPR-S	MIS3X3-16L	0808	3	Tape and Reel, 4000	Green
TPAFE0808-WS2R	WLCSP 2x2-16L	0808	1	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances

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