Analog Monitor Control Solution

Features

- 32 Monotonic 12-Bit DACs
  - Selectable Ranges: –10 V to 0 V, –5 V to 0 V, 0 V to 5 V, and 0 V to 10 V
  - High Current Drive Capability: Up to ±20 mA
  - Auto-Range Detector
  - Selectable Clamp Voltage
- 12-Bit SAR ADC
  - 6 High-Precision Inputs with 0-V to 5-V Range
  - Programmable Out-of-Range Alarms
- Five General Purpose I/O Ports (GPIOs)
- Internal 2.5-V Reference
- Internal Temperature Sensor
  - –40°C to 125°C Operation
- Low-Power SPI-Compatible Serial Interface
  - 3-Wire Mode, 1.8-V to 5.5-V Operation
- Operating Temperature: –40°C to 125°C
- Available in TQFP7X7-48L Package

Applications

- Wireless Infrastructure
  - Cellular Base Stations
  - Microwave Backhaul
- Optical Networks
- General Purpose Monitor and Control
- Data Acquisition Systems

Description

The TPAFE0534 is a highly integrated analog monitor and control solution with low power consumption. It includes a 6-channel 12-bit ADC, and 32-channel 12-bit DACs with programmable output ranges, an internal reference, 5 GPIOs, and a local temperature sensor. The high integration significantly reduces component counts and simplifies the system design with a small pace, low power, and high reliability.

The low power, very high integration, and wide operation temperature range of this device make it suitable for an all-in-one, low-cost, and bias-control circuit for power amplifiers found in multi-channel RF communication systems. The flexible DAC output ranges allow the device to be used as a biasing solution for a large variety of transistor technologies, such as LDMOS, GaN, or GaAs.

Table of Contents

Revision History

Date	Revision	Notes
2019-12-10	Rev.A.6	Added the application note. Corrected the register names of the DACBxx in the register description.
2020-05-28	Rev.A.7	Corrected the GPIO number in page 1.
2021-02-18	Rev.A.8	Added Tape and Reel Order Information, and the 2nd package POD.
2022-05-30	Rev.A.9	Updated the example board layout.
2023-05-21	Rev.A.10	Updated Tape and Reel Information.
2024-08-13	Rev.A.11	Updated to a new datasheet format. Added a note for Recommended Operating Conditions.
2024-12-12	Rev.A.12	Updated the POD of TQFP7x7-48. Added the MSL in the Order Information.

Pin Configuration and Functions

TPAFE0534
TQFP7X7-48L
Top View

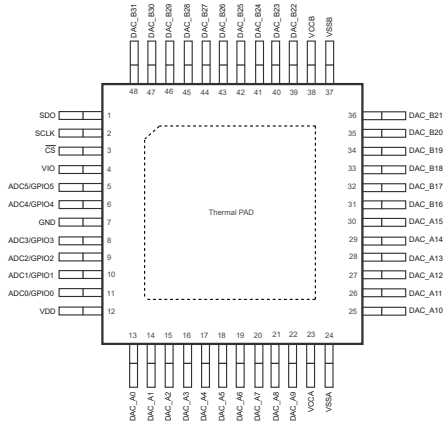


Table 1. Pin Functions

Pin No.	Name	I/O	Description
1	SDIO	I/O	Bi-directional serial data pin.
2	SCLK	I	SPI clock.
3	$\overline{CS}$	I	Active low serial data enable.
4	VIO	PWR	IO supply voltage.
5	ADC5/ GPIO5	I/O	• Analog ADC input. • It can be set to operate as GPIO: — GPIO5: $\overline{ALARMIN}$, active low alarm-control signal.
6 8~11	ADC4/ GPIO4 to ADC0/ GPIO0	I/O	• Analog ADC inputs. • These pins can be set to operate as GPIOs. • The GPIO functions are as follows: — GPIO4: $\overline{DAV}$, active low ADC data available indicator. — GPIO3: $\overline{ADCTRIG}$, active low external ADC conversion trigger. — GPIO2: $\overline{ALARMOUT}$, open drain global alarm output. — GPIO1: $\overline{CLEARB}$, active low DAC group B clear control signal. — GPIO0: $\overline{CLEARA}$, active low DAC group A clear control signal.
7	GND	GND	Ground supply.
12	VDD	PWR	Analog supply voltage.
13~22 25~30	DAC_A0 to DAC_A15	O	• DAC group A. • These 16 DAC outputs share the same range and clamp levels.
23	VCCA	PWR	Positive analog power supply for DAC group A.
24	VSSA	PWR	Negative analog power supply for DAC group A.

Pin No.	Name	I/O	Description
31~36 39~48	DAC_B16 to DAC_B31	O	• DAC group B. • These 16 DAC outputs share the same range and clamp levels.
37	VSSB	PWR	Negative analog power supply for DAC group A.
38	VCCB	PWR	Positive analog power supply for DAC group A.
	Thermal PAD	–	The thermal pad should be connected to PCB ground plane for good thermal performance.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
Supply Voltage	V_{DD} to GND	−0.3	6	V
	V_{IO} to GND	−0.3	6	V
	$V_{CC\ (A,\ B)}$ to GND	−0.3	12	V
	$V_{SS\ (A,\ B)}$ to GND	−12	0.3	V
	V_{CCA} to V_{SSA}	−0.3	12	V
	V_{CCB} to V_{SSB}	−0.3	12	V
Pin Voltage	DAC_A (0-15) Outputs to GND	V_{SSA} − 0.3	V_{CCA} + 0.3	V
	DAC_B (16-31) Outputs to GND	V_{SSB} − 0.3	V_{CCB} + 0.3	V
	FlexIO Pins to GND	−0.3	V_{DD} + 0.3	V
	SPI Pins to GND	−0.3	V_{IO} + 0.3	V
	ADC Analog Input Current	−10	10	mA
T_A	Operating Temperature Range	−40	125	℃
T_J	Maximum Junction Temperature	−40	150	℃
T_{STG}	Storage Temperature Range	−65	150	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output diode current ratings are observed.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2,000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1,000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Nom	Max	Unit
Supply Voltage	V_{DD}	4.5		5.5	V
	V_{IO}	1.65		5.5	V
	$V_{CC\ (A,\ B)}$	4.5		11	V
	$V_{SS\ (A,\ B)}$	−11		−4.5	V

Parameter		Min	Nom	Max	Unit
	V_{CCA} − V_{SSA}	4.5		11	V
	V_{CCB} − V_{SSB}	4.5		11	V
Specified Temperature Range		−40		125	℃
Operating Temperature Range		−40		125	℃

(1) For positive output, $V_{ss[a]}$ or $V_{ss[b]}$ should be connected to 0 V. For negative output, $V_{cc[a]}$ or $V_{cc[b]}$ should be connected to 0 V.

Thermal Information

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
TQFP7X7-48L	22.1	6.6	12.7 (top), 0.7 (bottom)	°C/W

Electrical Characteristics-DAC Specification

All test conditions: V_{DD} = 4.5 V to 5.5 V, V_{IO} = 1.65 V to 3.6 V; V_{CC} = 4.5 V to 11 V, V_{SS} = GND for positive range; V_{CC} = GND, V_{SS} = −11 V to −4.5 V for negative output range; over specified temperature range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
DAC DC Specifications					
Resolution		12			
Full-Scale Output Voltage Range	Power up or reset through auto-range detection	−10		0	V
		−5		0	
		0		5	
		0		10	
INL				±3	LSB
DNL				±1	LSB
Positive Output Range					
TUE	End point fit between codes 16 to 4031. DAC outputs unloaded.		±0.1	±0.5	%FSR
Total Error Temperature Drift	After one point calibration at 25 ℃. V_{OUT}: 2.5 V (10-V or 5-V range)		±0.03		%FSR
Offset Error	Full temp End point fit towards value at code 000h		±2	±15	mV
Offset Error Temperature Drift			±2		ppm/℃
Gain Error	Full temp		±0.01	±0.45	%FSR
Gain Error Temperature Drift			±20		ppm/℃
Zero-Scale Error	Full temp, code = 000h		2	15	mV
Zero-Scale Error Temperature Drift			±2		ppm/℃
Full-Scale Error	Code = FFFh		±0.01	±0.45	%FSR
Full-Scale Error Temperature Drift			±20		ppm/℃
Negative Output Ranges					
TUE			±0.1	±0.5	%FSR
Total Error Temperature Drift			±0.03		%FSR
Offset Error	End point fit towards value at code FFFh		±2	±15	mV
Offset Error Temperature Drift			±2		ppm/℃
Gain Error			±0.01	±0.45	%FSR
Gain Error Temperature Drift			±20		ppm/℃
Zero-Scale Error	Code = FFFh		−2	25	mV
Zero-Scale Error Temperature Drift			±2		ppm/℃
Full-Scale Error	Code = 000h		±0.01	±0.45	%FSR

Parameter	Conditions	Min	Typ	Max	Unit
Full-Scale Error Temperature Drift			±20		ppm/℃
DAC Output Buffer Specifications					
Load Current	Source with 1-V headroom from V_{CC} with 25-mV variation		20		mA
	Sink with 1-V headroom from V_{SS} with 25-mV variation		20		mA
Short-Circuit Current	Low current mode		±10		mA
	Normal mode (default)		±45		mA
Capacitive Load Stability	R_L = ∞		200		pF
DC Output Impedance	DAC code at mid-scale		1		Ω
Output Voltage Settling Time	Zero-scale to quarter full-scale step to within 2.5 mV. R_L = 2 kΩ, C_L = 200 pF		7		µs
	1/4 to 3/4 scale settling to ±0.5 LSB. R_L = 2 kΩ, C_L = 200 pF		11		
Slew Rate	Transition: 1/4 to 3/4 scale, 10% to 90%		0.5		V/µs
Output Noise	0.1 Hz to 10 Hz, DAC code at mid-scale		250		µVpp
Output Noise Density	1 kHz, DAC code at mid-scale		1,000		nV/√Hz
AC PSRR	DAC code at mid-scale. Frequency = 60 Hz, amplitude = 200 mVpp superimposed on V_{DD}		60		dB
	DAC code at mid-scale. Frequency = 60 Hz, amplitude = 200 mVpp superimposed on V_{CC}		85		dB
	DAC code at mid-scale. Frequency = 60 Hz, amplitude = 200 mVpp superimposed on V_{SS}		85		dB
DC PSRR	DAC code at mid-scale. ±5% variation on all supplies.		0.15		mV/V
Code Change Glitch Impulse	1-LSB change around major carrier		6		nV-s
Glitch Impulse Amplitude	1-LSB change around major carrier		4		mV
Power-on Overshoot	V_{SS} = GND, V_{CC} = 0 V to +11 V, 2-ms ramp, R_series = 5 ohm, C =1 µF		50		mV
	V_{SS} = GND, V_{CC} = 0 V to −11 V, 2-ms ramp, R_series = 5 ohm, C = 1 µF		50		mV
Turn-on Overshoot	0~1/2 FS R_series = 5 ohm, C = 1 µF				mV
Channel-to-Channel DC Crosstalk	Measured channel at midscale.		1		mV

Parameter	Conditions	Min	Typ	Max	Unit
	Full scale output change on all other channels.				
Clamp Output Specifications					
Load Current	DAC output buffers inactive. Sink with 2-V headroom from V_{SS}.	8			mA

Electrical Characteristics-ADC & TEMP Sensor Specification

All test conditions: V_{DD} = 4.5 V to 5.5 V, V_{IO} = 1.65 V to 3.6 V; V_{CC} = 4.5 V to 11 V, V_{SS} = GND for positive range; V_{CC} = GND, V_{SS} = −11 V to −4.5 V for negative output range; over operating temperature range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
ADC DC Specifications					
Resolution		12			
Full-Scale Input Range		0		$2 \times V_{REF}$	V
		0		V_{REF}	V
INL				±2	LSB
DNL				±1	LSB
Offset Error	After calibration			±5	LSB
Offset Error Match			±0.4		
Offset Error Temperature Drift			4		ppm/℃
Gain Error			±0.01	±0.5	%FSR
Gain Error Match			±0.4		LSB
Gain Error Temperature Drift			4		ppm/℃
Input Capacitance			20		pF
Input Bias Current	Unselected ADC input			±10	μA
Conversion Time			1.875		μS
Acquisition Time	500-kSPS conversion rate				μS
Conversion Rate			430		kSPS
Throughput Rate	SCLK = 20 MHz SPI update data rate			250	kSPS
Temperature Sensor Range					
Operating Range		−40		150	℃
Accuracy	T_J = −40℃ to 125℃		±2.5		℃
Resolution	LSB size		0.0625		℃
Update Time	T_J = −40℃ to 125℃		31.25		ms

Electrical Characteristics-General Specifications

All test conditions: V_{DD} = 4.5 V to 5.5 V, V_{IO} = 1.65 V to 5.5 V; V_{CC} = 4.5 V to 11 V, V_{SS} = GND for positive range; V_{CC} = GND, V_{SS} = −11 V to −4.5 V for negative output range; over operating temperature range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
GPIO Specifications					
$V_{IH\ LowVIO}$		0.7 × V_{IO}			V
$V_{IL\ LowVIO}$				0.3 × V_{IO}	V
Serial Interface Specifications					
$V_{IH\ LowVIO}$		0.7 × V_{IO}			V
$V_{IL\ LowVIO}$				0.3 × V_{IO}	V
Input Current			2		µA
Input Pin Capacitance			2		pF
V_{OH}	I_{source} = 0.2 mA	V_{IO} − 0.2			V
V_{OL}	I_{sink} = 0.2 mA			0.2	V
Output Pin Capacitance			2		pF
Pull-up Resistor nCS			1 M		Ω
Pull-up Resistor SCLK			1 M		Ω
Auto-Range Threshold Detector					
V_{SSTH}	Negative voltage range		−3.75		
V_{CCTH}	Positive voltage range		3		
Power Requirement					
I_{VDD}	All DAC at midscale code. ADC in fastest auto mode. Temperature sensor enabled.		20		mA
I_{VCC} (A,B)			10		mA
I_{VSS} (A,B)			10		mA
I_{VIO}			5		µA
I_{VDD}	Power-down mode		3		mA
I_{VCC} (A,B)			0.5		mA
I_{VSS} (A,B)			0.5		mA
I_{VIO}			5		µA

Timing Requirements

All test conditions: V_{DD} = 4.5 V to 5.5 V, V_{IO} = 1.8 V to 3.6 V; V_{CC} = 4.5 V to 11 V, V_{SS} = GND for positive range; V_{CC} = GND, V_{SS} = −11 V to −4.5 V for negative output range; over operating temperature range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
Serial Interface					
f(SCLK)				20	MHz
t_{PH} SCLK Pulse Width High		24.5			nS
t_{PL} SCLK Pulse Width Low		24.5			nS
t_{SU} SDI Setup (1)		20			nS
t_H SDI Hold (1)		20			nS
$t_{(ODZ)}$ SDO Driven to Tri-state		0		25	nS
$t_{(OZD)}$ SDO Tri-State to Driven		1.5		30	nS
$t_{(OD)}$ SDO Output Delay		0		25	nS
$t_{SU(CS)}$ $\overline{CS}$ Setup (1)		20			nS
$t_{H(/CS)}$ $\overline{CS}$ Hold (1)		20			nS
$t_{(IAG)}$ $\overline{CS}$ High Time		20			nS

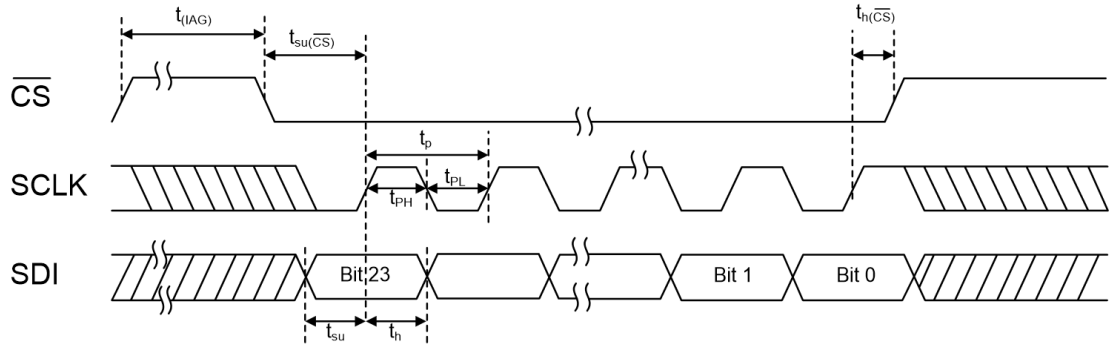


Figure 1. Serial Interface Write Timing Diagram

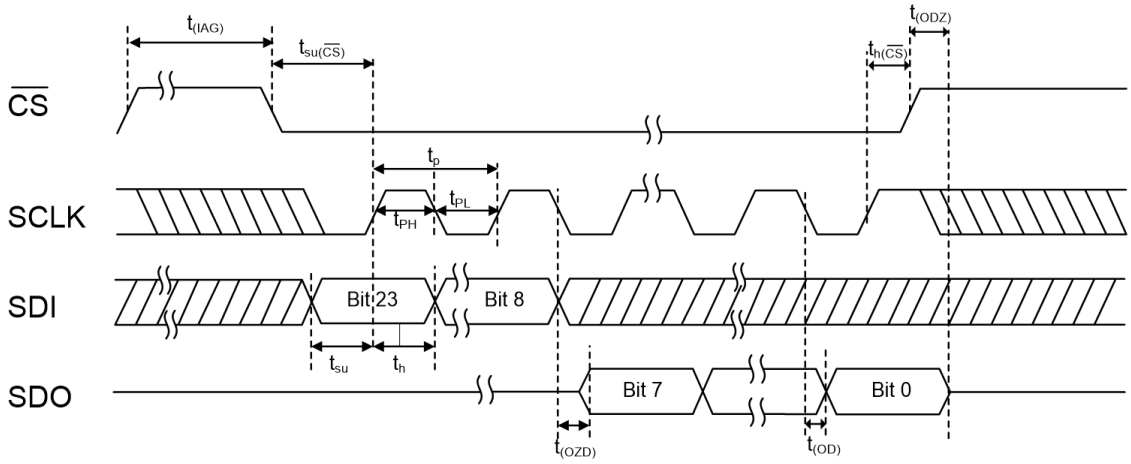


Figure 2. Serial Interface Read Timing Diagram

Detailed Description

Functional Block Diagram

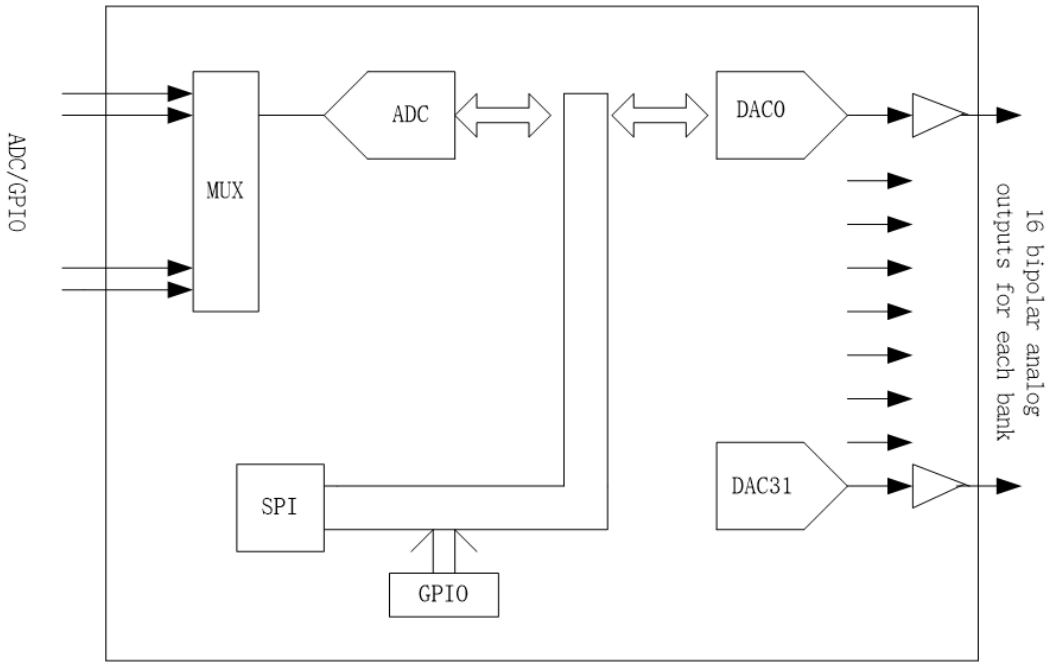


Figure 3. Functional Block Diagram

Feature Description

Register Map

Address1	Type	Default	Register Name
0x00	R/W	30	Interface Configuration 0
0x01	R/W	0	Interface Configuration 1
0x02	R/W	3	Device Configuration
0x03	R	8	Chip Type
0x04	R	32	Chip ID (Low Byte)
0x05	R	5	Chip ID (High Byte)
0x06	R	3	Chip Version
0x07–0x0B	—	—	Reserved
0x0C	R	32	Manufacturer ID (Low Byte)
0x0D	R	1	Manufacturer ID (High Byte)
0x0E	—	—	Reserved
0x0F	R/W	0	Register Update
0x21E	R	0	Temperature Data (Low byte)

Address1	Type	Default	Register Name
0x21F	R	40	Temperature Data (High byte)
0x220	R	0	ADC0-Data (Low Byte)
0x221	R	0	ADC0-Data (High Byte)
0x222	R	0	ADC1-Data (Low Byte)
0x223	R	0	ADC1-Data (High Byte)
0x224	R	0	ADC2-Data (Low Byte)
0x225	R	0	ADC2-Data (High Byte)
0x226	R	0	ADC3-Data (Low Byte)
0x227	R	0	ADC3-Data (High Byte)
0x228	R	0	ADC4-Data (Low Byte)
0x229	R	0	ADC4-Data (High Byte)
0x22A	R	0	ADC5-Data (Low Byte)
0x22B	R	0	ADC5-Data (High Byte)
0x22C–0x22D	—	—	Reserved
0x22E–0x22F	—	—	Reserved
0x230	R/W	0	DACA0-Data (Low Byte)
0x231	R/W	0	DACA0-Data (High Byte)
0x232	R/W	0	DACA1-Data (Low Byte)
0x233	R/W	0	DACA1-Data (High Byte)
0x234	R/W	0	DACA2-Data (Low Byte)
0x235	R/W	0	DACA2-Data (High Byte)
0x236	R/W	0	DACA3-Data (Low Byte)
0x237	R/W	0	DACA3-Data (High Byte)
0x238	R/W	0	DACA4-Data (Low Byte)
0x239	R/W	0	DACA4-Data (High Byte)
0x23A	R/W	0	DACA5-Data (Low Byte)
0x23B	R/W	0	DACA5-Data (High Byte)
0x23C	R/W	0	DACA6-Data (Low Byte)
0x23D	R/W	0	DACA6-Data (High Byte)
0x23E	R/W	0	DACA7-Data (Low Byte)
0x23F	R/W	0	DACA7-Data (High Byte)
0x240	R/W	0	DACA8-Data (Low Byte)
0x241	R/W	0	DACA8-Data (High Byte)
0x242	R/W	0	DACA9-Data (Low Byte)
0x243	R/W	0	DACA9-Data (High Byte)
0x244	R/W	0	DACA10-Data (Low Byte)
0x245	R/W	0	DACA10-Data (High Byte)

Address1	Type	Default	Register Name
0x246	R/W	0	DACA11-Data (Low Byte)
0x247	R/W	0	DACA11-Data (High Byte)
0x248	R/W	0	DACA12-Data (Low Byte)
0x249	R/W	0	DACA12-Data (High Byte)
0x24A	R/W	0	DACA13-Data (Low Byte)
0x24B	R/W	0	DACA13-Data (High Byte)
0x24C	R/W	0	DACA14-Data (Low Byte)
0x24D	R/W	0	DACA14-Data (High Byte)
0x24E	R/W	0	DACA15-Data (Low Byte)
0x24F	R/W	0	DACA15-Data (High Byte)
0x250	R/W	0	DACB16-Data (Low Byte)
0x251	R/W	0	DACB16-Data (High Byte)
0x252	R/W	0	DACB17-Data (Low Byte)
0x253	R/W	0	DACB17-Data (High Byte)
0x254	R/W	0	DACB18-Data (Low Byte)
0x255	R/W	0	DACB18-Data (High Byte)
0x256	R/W	0	DACB19-Data (Low Byte)
0x257	R/W	0	DACB19-Data (High Byte)
0x258	R/W	0	DACB20-Data (Low Byte)
0x259	R/W	0	DACB20-Data (High Byte)
0x25A	R/W	0	DACB21-Data (Low Byte)
0x25B	R/W	0	DACB21-Data (High Byte)
0x25C	R/W	0	DACB22-Data (Low Byte)
0x25D	R/W	0	DACB22-Data (High Byte)
0x25E	R/W	0	DACB23-Data (Low Byte)
0x25F	R/W	0	DACB23-Data (High Byte)
0x260	R/W	0	DACB24-Data (Low Byte)
0x261	R/W	0	DACB24-Data (High Byte)
0x262	R/W	0	DACB25-Data (Low Byte)
0x263	R/W	0	DACB25-Data (High Byte)
0x264	R/W	0	DACB26-Data (Low Byte)
0x265	R/W	0	DACB26-Data (High Byte)
0x266	R/W	0	DACB27-Data (Low Byte)
0x267	R/W	0	DACB27-Data (High Byte)
0x268	R/W	0	DACB28-Data (Low Byte)
0x269	R/W	0	DACB28-Data (High Byte)
0x26A	R/W	0	DACB29-Data (Low Byte)

Address1	Type	Default	Register Name
0x26B	R/W	0	DACB29-Data (High Byte)
0x26C	R/W	0	DACB30-Data (Low Byte)
0x26D	R/W	0	DACB30-Data (High Byte)
0x26E	R/W	0	DACB31-Data (Low Byte)
0x26F	R/W	0	DACB31-Data (High Byte)
0x310	R/W	0	ADC Configuration
0x311	R/W	60	False Alarm Configuration
0x312	R/W	0	GPIO Configuration
0x313	R/W	3F	ADC MUX Configuration
0x314	R/W	0	Hardware Reset
0x315	R/W	0	DAC Range
0x316	R/W	0	DAC Clear Enable 0
0x317	R/W	0	DAC Clear Enable 1
0x318	R/W	0	DAC Clear Enable 2
0x319	R/W	0	DAC Clear Enable 3
0x31A	R/W	0	DAC Clear Source 0
0x31B	R/W	0	DAC Clear Source 1
0x31C	R/W	0	ALARMOUT Source 0
0x31D	R/W	0	ALARMOUT Source 1
0x370	R	0	Alarm Status 0
0x371	R	0	Alarm Status 1
0x372	R	8	General Status
0x373	R	0	DACA7~DACA0 Output Short
0x374	R	0	DACA15~DACA8 Output Short
0x375	R	0	DACB23~DACB16 Output Short
0x376	R	0	DACB31~DACB24 Output Short
0x377–0x379	—	—	Reserved
0x37A	R/W	3F	GPIO
0x37B	R/W	0	Auxillary
0x37C–0x37D	—	0	Reserved
0x37E	W		DAC Broadcast Data (Low byte)
0x37F	W	—	DAC Broadcast Data (High byte)
0x380	R/W	FF	LT-Upper-Thresh (Low Byte)
0x381	R/W	0	LT-Lower-Thresh (Low Byte)
0x382	R/W	FF	LT-Therm-Thres (Thermal Shut Down)
0x383	—	—	Reserved
0x384	R/W	FF	ADC0-Upper-Thresh (Low Byte)

Address1	Type	Default	Register Name
0x385	R/W	0F	ADC0-Upper-Thresh (High Byte)
0x386	R/W	0	ADC0-Lower-Thresh (Low Byte)
0x387	R/W	0	ADC0-Lower-Thresh (High Byte)
0x388	R/W	FF	ADC1-Upper-Thresh (Low Byte)
0x389	R/W	0F	ADC1-Upper-Thresh (High Byte)
0x38A	R/W	0	ADC1-Lower-Thresh (Low Byte)
0x38B	R/W	0	ADC1-Lower-Thresh (High Byte)
0x38C	R/W	FF	ADC2-Upper-Thresh (Low Byte)
0x38D	R/W	0F	ADC2-Upper-Thresh (High Byte)
0x38E	R/W	0	ADC2-Lower-Thresh (Low Byte)
0x38F	R/W	0	ADC2-Lower-Thresh (High Byte)
0x390	R/W	FF	ADC3-Upper-Thresh (Low Byte)
0x391	R/W	0F	ADC3-Upper-Thresh (High Byte)
0x392	R/W	0	ADC3-Lower-Thresh (Low Byte)
0x393	R/W	0	ADC3-Lower-Thresh (High Byte)
0x394	R/W	FF	ADC4-Upper-Thresh (Low Byte)
0x395	R/W	0F	ADC4-Upper-Thresh (High Byte)
0x396	R/W	0	ADC4-Lower-Thresh (Low Byte)
0x397	R/W	0	ADC4-Lower-Thresh (High Byte)
0x398	R/W	FF	ADC5-Upper-Thresh (Low Byte)
0x399	R/W	0F	ADC5-Upper-Thresh (High Byte)
0x39A	R/W	0	ADC5-Lower-Thresh (Low Byte)
0x39B	R/W	0	ADC5-Lower-Thresh (High Byte)
0x39C–0x39F	—	—	Reserved
0x3A0	R/W	A	LT-Hysteresis
0x3A1	R/W	8	ADC0-Hysteresis
0x3A2	R/W	8	ADC1-Hysteresis
0x3A3	R/W	8	ADC2-Hysteresis
0x3A4	R/W	8	ADC3-Hysteresis
0x3A5	R/W	8	ADC4-Hysteresis
0x3A6	R/W	8	ADC5-Hysteresis
0x3A7–0xAD	—	—	Reserved
0x3AE	R/W	0	DAC Clear 0
0x3AF	R/W	0	DAC Clear 1
0x3B0	R/W	0	DAC Clear 2
0x3B1	R/W	0	DAC Clear 3
0x3B2	R/W	0	Power-Down 0

Address1	Type	Default	Register Name
0x3B3	R/W	0	Power-Down 1
0x3B4	R/W	0	Power-Down 2
0x3B5	R/W	0	Power-Down 3
0x3B6	R/W	0	Power-Down 4
0x3B7–0xBF	—	—	Reserved
0x3C0	R/W	77	ADC Trigger

Register identification

Interface configuration: address 0x00–0x02

Register name: interface configuration 0 – address 0x00

Register Name	Address	Bit	Name	Function
Interface Config 0	0x30	7	SOFT_RESET	Soft reset (self clearing).
				0: no action.
				1: reset. Reset everything except address 0x00, 0x01.
		6	Reserved	Reserved for factory use.
		5	ADDR-ASCEND	Address ascend.
				0: descend-decrements address while streaming (address wrap from 0x7fff to 0x0000).
				1: ascend-increments address while streaming (address wrap from 0x0000 to 0x7fff).
		4	Reserved	Reserved for factory use.
		3:00	Reserved	Reserved for factory use.

(1) This register is not reset by SOFT_RESET.
(2) This register does not require update (address 0x0F).

Register name: interface configuration 1 – address 0x01

Register Name	Address	Bit	Name	Function
Interface Config 1	0x01	7	SINGLE-INSTR	Single instruction enable.
				0: streaming mode (default).
				1: single instruction.
		6	Reserved	Reserved for factory use.
		5	READBACK	Read back.
				0: DAC read back from the active register (default).
				1: DAC read back from the buffer register.
		4	Reserved	Reserved for factory use.
		3	Reserved	Reserved for factory use.
		2	Reserved	Reserved for factory use.
		1	Reserved	Reserved for factory use.
		0	Reserved	Reserved for factory use.

(1) This register is not reset by SOFT_RESET.
(2) This register does not require update (address 0x0F).

Register name: device configuration – address 0x02

Register Name	Address	Bit	Name	Function
Device Config	0x02	7:02	Reserved	Reserved for factory use.
		1:00	POWER-MODE	Mode: • 00: normal opertion-full power and full performance. • 11: sleep-lowest power, non-operational except SPI. One time overwrite of the power-enable register (0xB2−0xB6).

Device identification: address 0x03–0x0D

Register name: chip type – address 0x03

Register Name	Address	Bit	Name	Function
Chip Type	0x03	7:04	Reserved	Reserved for factory use.
		3:00	CHIP-TYPE	Identify the device as a precison analog monitor and control.

Register name: chip ID low byte – address 0x04

Register Name	Address	Bit	Name	Function
Chip ID Low Byte	0x04	7:00	CHIPID-LOW	Chip ID. Low byte.

Register name: chip ID high byte – address 0x05

Register Name	Address	Bit	Name	Function
Chip ID High Byte	0x05	7:00	CHIPID-HIGH	Chip ID. High byte.

Register name: version ID – address 0x06

Register Name	Address	Bit	Name	Function
Version ID	0x06	7:00	VERSION ID	Version ID.

Rregister name: manufacture ID low byte – address 0x0C

Register Name	Address	Bit	Name	Function
Manuf. ID Low Byte	0x0C	7:00	VENDORID-LOW	Manufacture ID. Low byte.

Register name: manufacture ID high byte – address 0x0D

Register Name	Address	Bit	Name	Function
Manuf. ID High Byte	0x0D	7:00	VENDORID-HIGH	Manufacture ID. High byte.

Register update (buffered register): address 0x0F

Register name: register update – address 0x0F (self clearing)

Register Name	Address	Bit	Name	Function
Register Update	0x0F	7:06	Reserved	Reserved for factory use.
		5	TEMP-UPDATE	When set, transfer the latest temperature conversion data to the LT Data register.
		4	ADC-UPDATE	When set, transfer the latest ADC conversion data to the ADC Data registers.
				This function is needed when operating the ADC in autocycle mode.
		3:01	Reserved	Reserved for factory use.
		0	DAC-UPDATE	Update (self clearing).
				0: disabled.
				1: enabled. Transfer data from buffers to active registers (DAC register only).

General device configuration: address 0x310–0x317

Register name: ADC configuration – address 0x10 (R/W)

<table>
<tr><th>Register Name</th><th>Address</th><th>Bit</th><th>Name</th><th>Function</th></tr>
<tr><td rowspan="9">ADC Config</td><td rowspan="9">0x310</td><td rowspan="3">7</td><td rowspan="3">CMODE</td><td>ADC conversion mode bit. This bit selects the ADC conversion mode.</td></tr>
<tr><td>0: direct mode. The analog inputs specified in the ADC channel registers are converted sequentially on time. When one set of conversions is complete, the ADC is idle and waits for a new trigger.</td></tr>
<tr><td>1: auto mode. The analog inputs specified in the ADC channel registers are converted sequentially and repeatedly. When one set of conversions is complete, the ADC multiplexer returns to the first channel and repeats the process. The ADC-UPDATE bit in register 0x0F must be used to initiate the transfer of the latest conversion data to the ADC data registers.</td></tr>
<tr><td>6:05</td><td>CONV-RATE (1:0)</td><td>ADC conversion rate.
<table>
<tr><th>CR</th><th>tacq (ns)</th><th>tconv (ns)</th><th>Throughput</th></tr>
<tr><td>00</td><td>125</td><td>1875</td><td>500 kSPS</td></tr>
<tr><td>01</td><td>2125</td><td>1875</td><td>250 kSPS</td></tr>
<tr><td>10</td><td>6125</td><td>1875</td><td>125 kSPS</td></tr>
<tr><td>11</td><td>30125</td><td>1875</td><td>31.25 kSPS</td></tr>
</table></td></tr>
<tr><td>4</td><td>ADC-RANGE</td><td>ADC range selection bit.
0: 0−5 V.
1: 0−2.5 V.</td></tr>
<tr><td>3</td><td>ADC-CAL</td><td>Set to 1 enable offset calibration sequence upon ADC conversion startup (however offset calibration always runs once on the first trigger after power-up).</td></tr>
<tr><td>2</td><td>Reserved</td><td>Reserved for factory use.</td></tr>
<tr><td>1</td><td>SDOZDD</td><td>SDIO/SDO Z-to-driven delay increase. Increase SDIO/SDO tri-state to driven timing by 2 ns to reduce bus contention on applications where it is critical.</td></tr>
<tr><td>0</td><td>Reserved</td><td>Reserved for factory use.</td></tr>
</table>

Register name: flase alarm configuration – address 0x311

<table>
<tr><th>Register Name</th><th>Address</th><th>Bit</th><th>Name</th><th>Function</th></tr>
<tr><td rowspan="4">FALSE Alarm Config</td><td rowspan="4">0x311</td><td>7:05</td><td>CH-FALR-CT</td><td>False alarm protection for ADC channels.
<table><tr><th>CH-FALR-CT</th><th>N CONSECUTIVE SIMPLE</th></tr><tr><td>000</td><td>1</td></tr><tr><td>001</td><td>4</td></tr><tr><td>010</td><td>8</td></tr><tr><td>011</td><td>16 (default)</td></tr><tr><td>100</td><td>32</td></tr><tr><td>101</td><td>64</td></tr><tr><td>110</td><td>128</td></tr><tr><td>111</td><td>256</td></tr></table></td></tr>
<tr><td>4</td><td>Reserved</td><td>Reserved for factory use.</td></tr>
<tr><td>3:01</td><td>TEMP-FLAR-CT</td><td>False alarm protection senso high and low limits.
<table><tr><th>TEMP-FLAR-CT</th><th>N CONSECUTIVE SIMPLE</th></tr><tr><td>000</td><td>1 (default)</td></tr><tr><td>001</td><td>2</td></tr><tr><td>011</td><td>3</td></tr><tr><td>111</td><td>4</td></tr><tr><td>Others</td><td>1</td></tr></table></td></tr>
<tr><td>0</td><td>Reserved</td><td>Reserved for factory use.</td></tr>
</table>

Register name: GPIO configuration – address 0x312

Register Name	Address	Bit	Name	Function
GPIO Config	0x312	7:06	Reserved	Reserved for factory use.
		5	EN-ALARMIN	$\overline{\text{ALARMIN}}$ pin enable.
				0: GPIO5 operation (default).
				1: $\overline{\text{ALARMIN}}$ operation.
		4	EN-DAV	$\overline{\text{DAV}}$ pin enable.
				0: GPIO4 operation enable (default).
				1: $\overline{\text{DAV}}$ opertion.
		3	EN-ADCTRIG	$\overline{\text{ADCTRIG}}$ pin enable.
				0: GPIO3 operation enable (default).
				1: $\overline{\text{ADCTRIG}}$ operation.
		2	EN-ALARMOUT	$\overline{\text{ALARMOUT}}$ pin enable.
				0: GPIO2 operation enable.
				1: $\overline{\text{ALARMOUT}}$ operation (default).

Register Name	Address	Bit	Name	Function
		1	EN-CLR-B	$\overline{\text{CLEAR-B}}$ pin enable.
				0: GPIO1 operation (default).
				1: $\overline{\text{CLEAR}}$ operation for DAC_B group DACs.
		0	EN-CLR-A	$\overline{\text{CLEAR-A}}$ pin enable.
				0: GPIO1 operation (default).
				1: $\overline{\text{CLEAR}}$ operation for DAC_A group DACs.

Register name: ADC MUX configuration – address 0x313

Register Name	Address	Bit	Name	Function
ADC MUX Config	0x313	7:06	Reserved	Reserved for factory use.
		5	CH5	When set to 1, the corresponding analog input channel ADCn is accessed during an ADC conversion cycle. When set to 1, the corresponding bit in the GPIO configuration register is ignored, and the altermate GPIO function is blocked.
		4	CH4	When cleared to 0, the corresponding input channel ADCn is ignored during an ADC conversion cycle. When set to 0, the corresponding bit in the GPIO configuration register is effective.
		3	CH3	
		2	CH2	
		1	CH1	
		0	CH0	

Register name: hardware reset − address 0x314

Register Name	Address	Bit	Name	Function
Hardware Reset	0x314	7:00	HARD-RESET	Execute a full power-on-reset. Reset all registers to their defaults. When set to reserved, code 0xAD resets the device to its default, power-on-reset state.

DAC configuration: address 0x315−0x31D

Register name: DAC range − address 0x315

<table>
<tr><th>Register Name</th><th>Address</th><th>Bit</th><th>Name</th><th>Function</th></tr>
<tr><td rowspan="8">DAC Range 0</td><td rowspan="8">0x315</td><td>7</td><td>DAC-LC-B</td><td>Set to 1 enable low-current mode of the DACs group B.</td></tr>
<tr><td rowspan="5">6:04</td><td rowspan="5">DAC-RANGEB</td><td>DAC group B output voltage selection. Overrides output range set by the auto-range detection circuit.
DAC Range | DAC Group B Output
0xx | Range set by auto-range detection circuit
100 | −10 V to 0 V
101 | −5 V to 0 V
110 | 0 V to 10 V
111 | 0 V to 5 V</td></tr>
<tr><td></td></tr>
<tr><td></td></tr>
<tr><td></td></tr>
<tr><td></td></tr>
<tr><td>3</td><td>DAC-LC-A</td><td>Set to 1 enable low-current mode of the DACs group A.</td></tr>
<tr><td>2:00</td><td>DAC-RANGEA</td><td>AC group A output voltage selection. Overrides output range set by the auto-range detection circuit.
DAC Range | DAC Group A Output
0xx | Range set by auto-range detection circuit
100 | −10 V to 0 V
101 | −5 V to 0 V
110 | 0 V to 10 V
111 | 0 V to 5 V</td></tr>
</table>

Register name: DAC clear enable 0 − address 0x316

Register Name	Address	Bit	Name	Function
DAC Clear Enable 0	0x316	7	CLREN-A7	This register determines which DACs go into a clear state when a clear event is detected as configured in the DA-CLEAR-SOURCE registers.
		6	CLREN-A6	If CLRENn = 1, DAC_n is forced into a clear state with a clear event.
		5	CLREN-A5	If CLRENn = 0, a clear event does not affect the state of DAC_n.
		4	CLREN-A4	
		3	CLREN-A3	
		2	CLREN-A2	

Register Name	Address	Bit	Name	Function
		1	CLREN-A1	
		0	CLREN-A0	

Register name: DAC clear enable 1 − address 0x317

Register Name	Address	Bit	Name	Function
DAC Clear Enable 1	0x317	7	CLREN-A15	This register determines which DACs go into a clear state when a clear event is detected as configured in the DA-CLEAR-SOURCE registers.
		6	CLREN-A14	If CLRENn = 1, DAC_n is forced into a clear state with a clear event.
		5	CLREN-A13	If CLRENn = 0, a clear event does not affect the state of DAC_n.
		4	CLREN-A12	
		3	CLREN-A11	
		2	CLREN-A10	
		1	CLREN-A9	
		0	CLREN-A8	

Register name: DAC clear enable 2 – address 0x318

Register Name	Address	Bit	Name	Function
0x318	0x318	7	CLREN-B23	This register determines which DACs go into clear state when a clear event is detected as configured in the DA-CLEAR-SOURCE registers.
		6	CLREN-B22	If CLRENn=1, DAC_n is forced into a clear state with a clear event.
		5	CLREN-B21	If CLRENn = 0, a clear event does not affect the state of DAC_n.
		4	CLREN-B20	
		3	CLREN-B19	
		2	CLREN-B18	
		1	CLREN-B17	
		0	CLREN-B16	

Register name: DAC clear enable 3 – address 0x319

Register Name	Address	Bit	Name	Function
DAC Clear Enable 3	0x319	7	CLREN-B31	This register determines which DACs go into clear state when a clear event is detected as configured in the DA-CLEAR-SOURCE registers.
		6	CLREN-B30	If CLRENn = 1, DAC_n is forced into a clear state with a clear event.
		5	CLREN-B29	If CLRENn = 0, a clear event does not affect the state of DAC_n.
		4	CLREN-B28	
		3	CLREN-B27	
		2	CLREN-B26	
		1	CLREN-B25	
		0	CLREN-B24	

Register name: DAC clear source 0 – address 0x31A

Register Name	Address	Bit	Name	Function
DAC Clear Source 0	0x31A	7	REF-ALR-CLR	This register selects which alarm forces DACs into a clear state, regardless of which DAC operation mode is active, auto, or manual. In order for DAC_n to go into clear mode, it must be enabled in the DAC clear enable registers.
		6	ALMIN-ALR-CLR	
		5	ADC5-ALR-CLR	
		4	ADC4-ALR-CLR	
		3	ADC3-ALR-CLR	
		2	ADC2-ALR-CLR	
		1	ADC1-ALR-CLR	
		0	ADC0-ALR-CLR	

Register name: DAC clear source 1 – address 0x31B

Register Name	Address	Bit	Name	Function
DAC Clear Source 1	0x31B	7:03	Reserved	Reserved for factory use.
		2	THERM-ALR-CLR	This register selects which alarm forces DACs into a clear state, regardless of which DAC operation mode is active, auto, or manual. In order for DAC_n to go into clear mode, it must be enabled in the DAC clear enable registers.
		1	LT-HIGH-ALR-CLR	
		0	LT-LOW-ALR-CLR	

Register name: ALARMOUT source 0 – address 0x31C

Register Name	Address	Bit	Name	Function
ALARM OUT Source 0	0x31C	7	REF-ALR-OUT	This register selects which alarms can active the $\overline{\text{ALARMOUT}}$ pin. The $\overline{\text{ALARMOUT}}$ must be enabled for this function to take effect.
		6	ALMIN-ALR-OUT	
		5	ADC5-CLR-OUT	
		4	ADC4-CLR-OUT	
		3	ADC3-CLR-OUT	
		2	ADC2-CLR-OUT	
		1	ADC1-CLR-OUT	
		0	ADC0-CLR-OUT	

Register name: ALARMOUT source 1 – address 0x31D

Register Name	Address	Bit	Name	Function
ALARMOUT Source 1	0x31D	7:04	Reserved	Reserved for factory use.
		3	ALARM-LATCH-DIS	Alarm latch disable bit.
				When cleared to 0, the alarm bits are latched. When an alarm occurs, the corresponding alarm bit is set to 1. The alarm bit remains until the error condition subsides and the alarm register is read. Before reading, the alarm bit is not cleared even if the alarm condition disappears.
				When set to 1, the alarm bits are not latched. When the alarm condition subsides, the alarm bits are cleared regardless of whether the alarm bits have been read or not.
		2	THERM-ALR-OUT	This register selects which alarms can active the $\overline{\text{ALARMOUT}}$ pin. The $\overline{\text{ALARMOUT}}$ must be enabled for this function to take effect.
		1	LT-HIGH-ALR-OUT	
		0	LT-LOW-ALR-OUT	

ADC and temperature data: address 0x21E−0x22B

Register name: temperature data (low byte) – address 0x21E

Register Name	Address	Bit	Name	Function
Temp Data (Low)	0x21E	7:04	TEMP-DATA (3:0)	Store the temperature sensor in decimal data.
		3:00	Reserved	Reserved for factory use.

Register name: temperature data (high byte) – address 0x21F

Register Name	Address	Bit	Name	Function
Temp Data (High)	0x21F	3:00	TEMP-DATA	Stores the temperature sensor. Integer data.

Register name: ADCn data (low byte) – address 0x220−0x22B

Register Name	Address	Bit	Name	Function
ADCn Data (Low)	0x220 to 0x22B	7:00	ADCn-DATA (7:0)	Store the 12-bit ADCn conversion results in straight binary format.

Register name: ADCn data (high byte) – address 0x220−0x22B

Register Name	Address	Bit	Name	Function
ADCn Data (High)	0x220 to 0x22B	7:00	ADCn-DATA (7:0)	Store the 12-bit ADCn conversion results in straight binary format.

DAC data: address 0x230−0x26F

Register name: DACn data (low byte) – address 0x230−0x26

Register Name	Address	Bit	Name	Function
DACn Data (Low)	0x230 to 0x26F	7:00	DACn-DATA	Store the 12-bit data to be loaded to the DAC_n latches in straight binary format. The straight binary format is used for all DAC ranges.

Register name: DACn data (high byte) – address 0x230−0x26F

Register Name	Address	Bit	Name	Function
DACn Data (High)	0x230 to 0x26F	7:04	Reserved	Reserved for factory use.
		3:00	ADCn-DATA (11:8)	Store the 12-bit data to be loaded to the DAC_n latches in straight binary format. The straight binary format is used for all DAC ranges.

Status register: address 0x370−0x372

Register name: alarm status 0 – address 0x370

Register Name	Address	Bit	Name	Function
Alarm Status 0	0x370	7	REF-ALR	REF-ALR = 1 when the internal reference voltage is less than 2.2 V.
		6	ALARMIN-ALR	ALARMIN = 1 if the $\overline{\text{ALARMIN}}$ pin is enabled and set high.
		5	ADC5-ALR	ADC5-ALR = 1 when out of the range defined by the corresponding threshold registers.
				ADC5-ALR = 0 when the analog input is within the specified range.
		4	ADC4-ALR	ADC4-ALR = 1 when out of the range defined by the corresponding threshold registers.
				ADC4-ALR = 0 when the analog input is within the specified range.
		3	ADC3-ALR	ADC3-ALR = 1 when out of the range defined by the corresponding threshold registers.
				ADC3-ALR = 0 when the analog input is within the specified range.
		2	ADC2-ALR	ADC2-ALR = 1 when out of the range defined by the corresponding threshold registers.
				ADC2-ALR = 0 when the analog input is within the specified range.
		1	ADC1-ALR	ADC1-ALR = 1 when out of the range defined by the corresponding threshold registers.
				ADC1-ALR = 0 when the analog input is within the specified range.
		0	ADC0-ALR	ADC0-ALR = 1 when out of the range defined by the corresponding threshold registers.
				ADC0-ALR = 0 when the analog input is within the specified range.

Register name: alarm status 1 – address 0x371

Register Name	Address	Bit	Name	Function
Alarm Status 1	0x371	7:03	Reserved	Reserved for factory use.
		2	THERM-ALR	Thermal alarm flag. When the die temperature is equal to or greater than the thermal threshold, the bit is set 1 and the THERM-ALR flag actives. The on-chip temperature senor (LT) monitors the die temperature. If LT is disabled, the THERM-ALR bit is always 0.

Register Name	Address	Bit	Name	Function
		1	LT-HIGH-ALR	LT-LOW-ALR = 1 when the temperature sensor is out of the range defined by the upper threshold.
		0	LT-LOW-ALR	LT-LOW-ALR = 1 when the temperature sensor is out of the range defined by the lower threshold.

Register name: alarm status 1 – address 0x372

Register Name	Address	Bit	Name	Function
General Status	0x372	7	VCCB	This bit is the VCC detection output for DAC group B. Doesn't affect the auto-range detection result. Used for information only.
		6	VCCA	This bit is the VCC detection output for DAC group A. Doesn't affect the auto-range detection result. Used for information only.
		5	VSSB	This bit is the auto-range detection output for DAC group B.
				0: 0 V to 5 V.
				1: −10 V to 0 V.
		4	VSSA	This bit is the auto-range detection output for DAC group A.
				0: 0 V to 5 V.
				1: −10 V to 0 V.
		3	ADC-READY	ADC Ready indicator. ADC-READY must be 1 in order for the ADC to respond to a trigger to begin conversions.
				ADC-READY = 1 means the ADC is ready (waiting) to be triggered. During power-up, it remains unready (0) until the ADC is powered up (PADC set to 1) and at least one ADC channel is enabled. If there is any write that would stop the ADC, ADC-READY becomes 0 until the device completes processing of these changes/updates. Then if PADC = 1 and at least one channel is enabled, ADC-REDAY returns to 1.
				Once a trigger is received and the ADC begins conversions, the ADC-READY bit becomes 0.
		2	LT-BUSY	Temperature sensor busy indicator.
		1	GALR	Global alarm bit.
				This bit is the OR function or all individual alarm bits of the status register. This bit is set to 1 when any alarm condition occurs and

Register Name	Address	Bit	Name	Function
				remains set until the Status Register is read. This bit is cleared after reading the Status Register.
		0	DAVF	ADC data available flag bit. Direct mode only. Always cleared in auto mode.
				0: ADC conversion is in progress or ADC is in auto mode.
				1: ADC conversion is complete and new data is available.

Register name: DAC output short – address 0x373−0x376

DACA7−DACA0 output short address: 0x373

Register Name	Address	Bit	Name	Function
Power Enable 3	0x373	7	DAC-A7 Short	The bit is set to 1 if the corresponding DAC is detected to be shorted.
		6	DAC-A6 Short	The bit is not latched.
		5	DAC-A5 Short	
		4	DAC-A4 Short	
		3	DAC-A3 Short	
		2	DAC-A2 Short	
		1	DAC-A1 Short	
		0	DAC-A0 Short	

DACA15−DACA8 output short address: 0x374

Register Name	Address	Bit	Name	Function
Power Enable 3	0x374	7	DAC-A15 Short	The bit is set to 1 if the corresponding DAC is detected to be shorted.
		6	DAC-A14 Short	The bit is not latched.
		5	DAC-A13 Short	
		4	DAC-A12 Short	
		3	DAC-A11 Short	
		2	DAC-A10 Short	
		1	DAC-A9 Short	
		0	DAC-A8 Short	

DACB7−DACB0 output short address: 0x375

Register Name	Address	Bit	Name	Function
Power Enable 3	0x375	7	DAC-B23 Short	The bit is set to 1 if the corresponding DAC is detected to be shorted.
		6	DAC-B22 Short	The bit is not latched.
		5	DAC-B21 Short	
		4	DAC-B20 Short	
		3	DAC-B19 Short	
		2	DAC-B18 Short	
		1	DAC-B17 Short	
		0	DAC-B16 Short	

DACB31−DACB23 output short address: 0x376

Register Name	Address	Bit	Name	Function
Power Enable 3	0x376	7	DAC-B31 Short	The bit is set to 1 if the corresponding DAC is detected to be shorted.
		6	DAC-B30 Short	The bit is not latched.
		5	DAC-B29 Short	
		4	DAC-B28 Short	
		3	DAC-B27 Short	
		2	DAC-B26 Short	
		1	DAC-B25 Short	
		0	DAC-B24 Short	

GPIO data: address 0x37A

Register name: GPIO – address 0x37A

Register Name	Address	Bit	Name	Function
GPIO	0x37A	7:06	Reserved	For write operation, the GPIO pin operates as an output. Writing a 1 to the GPIO-n bit sets the GPIO-n pin to high impedance. Writing a 0 sets the GPIO-n pin to logic low-alarm.
		5	GPIO-5	For read operations, the GPIO pin operates as an input. Read the GPIO-n bit to receive the status of the GPIO-n pin.
		4	GPIO-4	After power-on reset, or any forced hardware or software reset, the GPIO-n bit pin is in a high-impedance state.
		3	GPIO-3	
		2	GPIO-2	
		1	GPIO-1	
		0	GPIO-0	

DAC broadcast data: address 0x37E−0x37F

Register name: DAC broadcast data (low byte) – address 0x37E

Register Name	Address	Bit	Name	Function
DAC Broadcast Data (Low)	0x37E	7:00	DAC-BROADCAST-DATA (7:0)	Writing to this register sets all DACn data low byte buffers to specified code.

Register name: DAC broadcast data (high byte) – address 0x37F

Register Name	Address	Bit	Name	Function
DAC Broadcast Data (High)	0x37F	7:04	Reserved	Reserved for factory use.
		3:00	DAC-BROADCAST-DATA (11:8)	Writing to this register sets all DACn data high byte buffers to specified code.

Out-of-range ADC threshold: address 0x380−0x39B

Register name: LT upper thresh – address 0x380

Register Name	Address	Bit	Name	Function
LT Upper Thresh	0x380	7:00	THRU-LT (7:0)	Set 8-bit upper threshold value for the local temperature sensor.

Register name: LT lower thresh – address 0x381

Register Name	Address	Bit	Name	Function
LT Lower Thresh	0x381	7:00	THRL-LT (7:0)	Set 8-bit lower threshold value for the local temperature sensor.

Register name: therm thresh – address 0x382

Register Name	Address	Bit	Name	Function
Therm Thresh	0x382	7:00	THRU-THERM (7:0)	Set 8-bit die thermal threshold value for the local temperature sensor.

Register name: ADCn upper thresh (low byte) – address 0x384−0x39B

Register Name	Address	Bit	Name	Function
ADCn Upper Thresh (Low)	0x384 to 0x39B	7:00	THRUn (7:0)	Set 12-bit upper threshold value for the ADCn channel in straight binary format.

Register name: ADCn upper thresh (high byte) – address 0x384−0x39B

Register Name	Address	Bit	Name	Function
ADCn Upper Thresh (High)	0x384 to 0x39B	7:04	Reserved	Reserved for factory use.
		3:00	THRUn (11:8)	Set 12-bit upper threshold value for the ADCn channel in straight binary format.

Register name: ADCn lower thresh (low byte) – address 0x384−0x39B

Register Name	Address	Bit	Name	Function
ADCn Lower Thresh (Low)	0x384 to 0x39B	7:00	THRLn (7:0)	Set 12-bit lower threshold value for the ADCn channel in straight binary format.

Register name: ADCn lower thresh (high byte) – address 0x384−0x39B

Register Name	Address	Bit	Name	Function
ADCn Lower Thresh (High)	0x384 to 0x39B	7:04	Reserved	Reserved for factory use.
		3:00	THRLn (11:8)	Set 12-bit lower threshold value for the ADCn channel in the straight binary format.

Hysteresis: address 0x3A0−0x3A6

Register name: thermal hysteresis − address 0x3A0

Register Name	Address	Bit	Name	Function
Thermal Hysteresis	0x3A0	7:00	THERM-HYST (7:0)	Hysteresis of the die thermal temperature sensor, 1°C per step.

Register name: ADCn hysteresis – address 0x3A1−0x3A6

Register Name	Address	Bit	Name	Function
ADCn Hysteresis	0x3A6	7	Reserved	Reserved for factory use.
		6:00	HYSTn (6:0)	Hysteresis of general purpose ADCn, 1 LSB per step.

Power-down register: address 0x3AE−0x3B6

Register name: DAC clear 0 – address 0x3AE

Register Name	Address	Bit	Name	Function
DAC Clear 0	0x3AE	7	CLR-A7	This register uses software to force the DAC into a clear state.
		6	CLR-A6	
		5	CLR-A5	If CLRn = 1, DAC_n is forced into a clear state.
		4	CLR-A4	
		3	CLR-A3	If CLRn = 0, DAC_n is restored to normal operation.
		2	CLR-A2	
		1	CLR-A1	
		0	CLR-A0	

Register name: DAC clear 1 – address 0x3AF

Register Name	Address	Bit	Name	Function
DAC Clear 1	0x3AF	7	CLR-A15	This register uses software to force the DAC into a clear state.
		6	CLR-A14	
		5	CLR-A13	If CLRn = 1, DAC_n is forced into a clear state.
		4	CLR-A12	
		3	CLR-A11	If CLRn = 0, DAC_n is restored to normal operation.
		2	CLR-A10	
		1	CLR-A9	
		0	CLR-A8	

Register name: DAC clear 2 – address 0x3B0

Register Name	Address	Bit	Name	Function
DAC Clear 2	0x3B0	7	CLR-B23	This register uses software to force the DAC into a clear state.
		6	CLR-B22	
		5	CLR-B21	If CLRn = 1, DAC_n is forced into a clear state.
		4	CLR-B20	
		3	CLR-B19	If CLRn = 0, DAC_n is restored to normal operation.
		2	CLR-B18	
		1	CLR-B17	
		0	CLR-B16	

Register name: DAC clear 3 – address 0x3B1

Register Name	Address	Bit	Name	Function
DAC Clear 3	0x3B1	7	CLR-B31	This register uses software to force the DAC into a clear state.
		6	CLR-B30	
		5	CLR-B29	If CLRn = 1, DAC_n is forced into a clear state.
		4	CLR-B28	
		3	CLR-B27	If CLRn = 0, DAC_n is restored to normal operation.
		2	CLR-B26	
		1	CLR-B25	
		0	CLR-B24	

Register name: power enable 0 – address 0x3B2

Register Name	Address	Bit	Name	Function
Power Enable 0	0x3B2	7	PDAC-A7	After power-on or reset, all bits in the Power-Down Register are cleared to the default value, and all the components controlled by this register are either powered-down or off.
		6	PDAC-A6	The Power-Down Register allows the host to manage the TPAFE0534 power dissipation. When not required, the ADC, temperature sensor, internal reference, and any of the DACs can be put into an inactive low-power mode to reduce current drain from the supply.
		5	PDAC-A5	The bits in the Power-Down Register control this power-down function. Set the respective bit to 1 to active the corresponding function.
		4	PDAC-A4	
		3	PDAC-A3	
		2	PDAC-A2	
		1	PDAC-A1	
		0	PDAC-A0	

Register name: power enable 1 – address 0x3B3

Register Name	Address	Bit	Name	Function
Power Enable 1	0x3B3	7	PDAC-A15	After power-on or reset, all bits in the Power-Down Register are cleared to the default value, and all the components controlled by this register are either powered-down or off.
		6	PDAC-A14	The Power-Down Register allows the host to manage the TPAFE0534 power dissipation. When not required, the ADC, temperature sensor, internal reference, and any of the DACs can be put into an inactive low-power mode to reduce current drain from the supply.
		5	PDAC-A13	The bits in the Power-Down Register control this power-down function. Set the respective bit to 1 to active the corresponding function.
		4	PDAC-A12	
		3	PDAC-A11	
		2	PDAC-A10	
		1	PDAC-A9	
		0	PDAC-A8	

Register name: power enable 2 – address 0x3B4

Register Name	Address	Bit	Name	Function
Power Enable 2	0x3B4	7	PDAC-B23	After power-on or reset, all bits in the Power-Down Register are cleared to the default value, and all the components controlled by this register are either powered-down or off.
		6	PDAC-B22	The Power-Down Register allows the host to manage the TPAFE0534 power dissipation. When not required, the ADC, temperature sensor, internal reference, and any of the DACs can be put into an inactive low-power mode to reduce current drain from the supply.
		5	PDAC-B21	The bits in the Power-Down Register control this power-down function. Set the respective bit to 1 to active the corresponding function.
		4	PDAC-B20	
		3	PDAC-B19	
		2	PDAC-B18	
		1	PDAC-B17	
		0	PDAC-B16	

Register name: power enable 3 – address 0x3B5

Register Name	Address	Bit	Name	Function
Power Enable 3	0x3B5	7	PDAC-B31	After power-on or reset, all bits in the Power-Down Register are cleared to the default value, and all the components controlled by this register are either powered-down or off.
		6	PDAC-B30	The Power-Down Register allows the host to manage the TPAFE0534 power dissipation. When not required, the ADC, temperature sensor, internal reference, and any of the DACs can be put into an inactive low-power mode to reduce current drain from the supply.
		5	PDAC-B29	The bits in the Power-Down Register control this power-down function. Set the respective bit to 1 to active the corresponding function.
		4	PDAC-B28	
		3	PDAC-B27	
		2	PDAC-B26	
		1	PDAC-B25	
		0	PDAC-B24	

Register name: power enable 4 – address 0x3B6

Register Name	Address	Bit	Name	Function
Power Enable 4	0x3B6	7:03	Reserved	Reserved for factory use.
		2	PTEMP	After power-on or reset, all bits in the Power-Down Register are cleared to the default value, and all the components controlled by this register are either powered-down or off.
		1	Reserved	The Power-Down Register allows the host to manage the TPAFE0534 power dissipation. When not required, the ADC, temperature sensor, internal reference, and any of the DACs can be put into an inactive low-power mode to reduce current drain from the supply.
		0	PADC	The bits in the Power-Down Register control this power-down function. Set the respective bit to 1 to active the corresponding function.

ADC trigger: address 0x3C0

Register name: ADC trigger – address 0x3C0

Register Name	Address	Bit	Name	Function
ADC Trigger	0x3C0	7:01	Reserved	Reserved for factory use.
		0	ICONV	Internal ADC conversion bit.
				Set this bit to 1 start the ADC conversion internally. The bit is automatically cleared to 0 after the ADC conversion starts.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

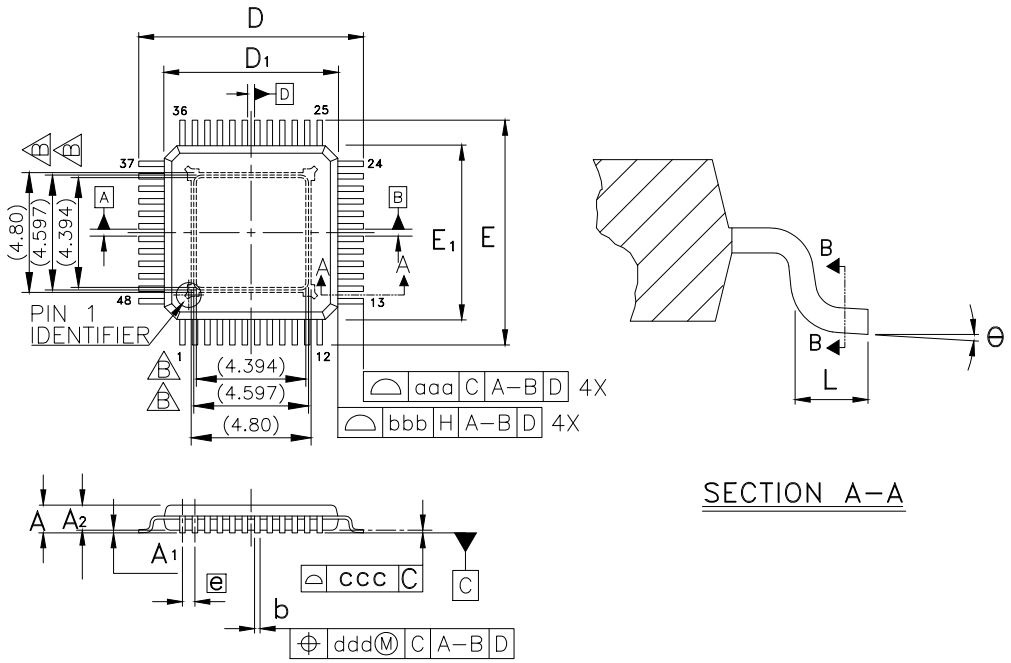
Application Note

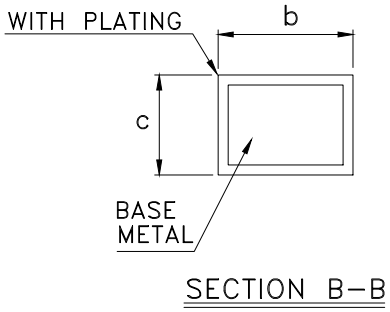
1. The series resistor and filter cap are recommended to be added at the DAC output, and then DAC stability can be assured when driving large loads, such as GaN FET.
   R_series = 5 ohm, C = 1 μF are recommended.
2. The filter cap should be added on each supply voltage to make sure the device works in stable condition.
3. When writing following registers, it is suggested to use single mode, or write single byte in stream mode. If multi bytes are written once in stream mode, SPI speed should be lower than 10 MHz, or wait 800 nS between each two bytes written if SPI speed is larger than 10 MHz.
   - 0x0310 (ADC/SPI Configuration), 0x0311 (False Alarm Configuration);
   - 0x0380 (LT-Upper-Thresh (Low byte)) to 0x0382 (LT-Therm-Thresh (Low byte));
   - 0x0384 (ADC0-Upper-Thresh (Low byte) to 0x39b (ADC5-Lower-Thresh (High byte));
   - 0x03A1 (Therm Hystersis) to 0x03A6 (ADC5-Hystersis);
   - 0x03B2 (Power-Enable 0) to 0x03B6 (Power-Enable 4).
4. When writing 0x026F in stream mode, the descend mode should be used. There is no limit in single mode.

Package Outline Dimensions

TQFP7X7-48

Package Outline Dimensions QPC(TQFP7X7-48-A)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.000	1.200	0.039	0.047
A1	0.050	0.150	0.002	0.006
A2	0.950	1.050	0.037	0.041
b	0.170	0.270	0.007	0.011
c	0.090	0.200	0.004	0.008
D	9.000 BSC		0.354 BSC	
D1	7.000 BSC		0.276 BSC	
E	9.000 BSC		0.354 BSC	
E1	7.000 BSC		0.276 BSC	
e	0.500 BSC		0.020 BSC	
L	0.450	0.750	0.018	0.030
θ	0	7°	0	7°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPAFE0534-QPCR-S	−40 to 125°C	TQFP7X7-48L	0534	3	Tray, 2500	Green
TPAFE0534-QPCR-S	−40 to 125°C	TQFP7X7-48L	0534	3	Tape and Reel, 2000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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