Analog Monitor Control Solution

Features

- 32 Monotonic 12-Bit DACs
  - Selectable Ranges: −10 to 0 V, −5 to 0 V, 0 to 5 V, and 0 to 10 V
  - High Current Drive Capability: up to ±20 mA
  - Auto-Range Detector
  - Selectable Clamp Voltage
- 12-Bit SAR ADC
  - 5 High Precision Inputs with 0-V to 5-V Range
  - Programmable Out-of-Range Alarms
- Five General Purpose I/O Ports (GPIOs)
- Internal 2.5-V Reference
- Internal Temperature Sensor
  - −40°C to 125°C Operation
- Low-Power SPI-Compatible Serial Interface
  - 4-Wire Mode or 3-Wire Mode, 1.8-V to 5.5-V Operation
- Operating Temperature: −40°C to 125°C
- Available in TQFP7X7-48 package

Applications

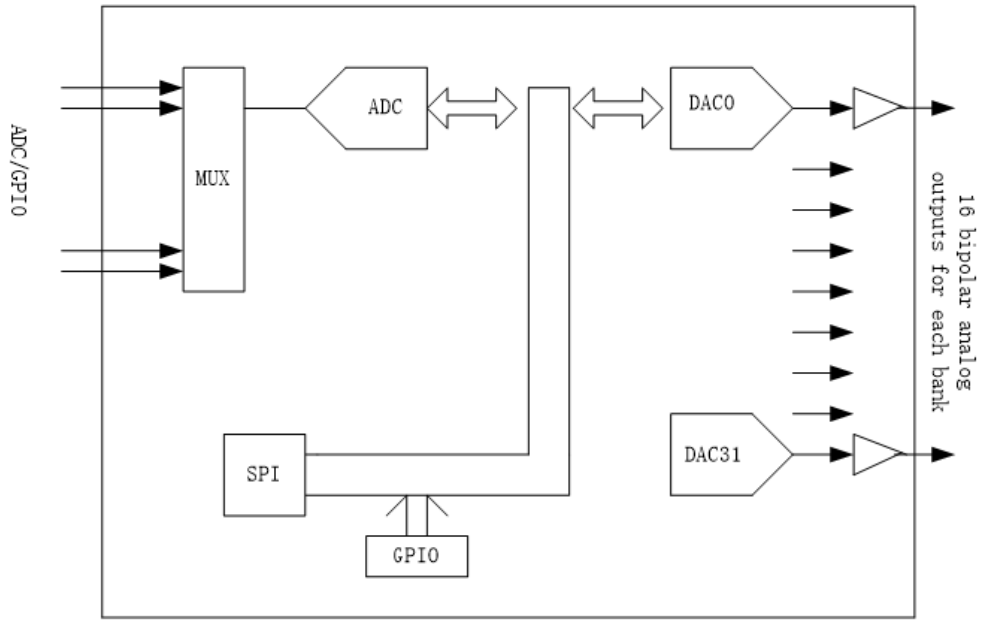
- Wireless Infrastructure
  - Cellular Base Stations
  - Microwave Backhaul
- Optical Networks
- General Purpose Monitor and Control
- Data Acquisition Systems

Description

The TPAFE0532 is a highly integrated, low power consumption, analog monitor and control solution. It includes a 5-channel, 12-bit ADC, 32-channel 12-bit DACs with programmable output ranges, an internal reference, 5 GPIOs, and a local temperature sensor. The high integration significantly reduces component counts and simplifies the system design with small pace, low power, and high reliability.

The low power, very high integration, and wide operation temperature range of this device make it suitable for an all-in-one, low-cost, and bias-control circuit for power amplifiers found in multi-channel RF communication systems. The flexible DAC output ranges allow the device to be used as a biasing solution for a large variety of transistor technologies, such as LDMOS, GaN, or GaAs.

Typical Application Circuit



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Revision History

Date	Revision	Notes
2019-12-10	Rev.A.6	Added the application note. Corrected the register names of the DACBxx in the register description.
2020-05-28	Rev.A.7	Corrected the GPIO number in page 1.
2021-02-18	Rev.A.8	Added Tape and Reel Order Information, and the 2nd package POD.
2022-05-30	Rev.A.9	Updated the example board layout.
2023-05-21	Rev.A.10	Updated Tape and Reel Information.
2024-08-13	Rev.A.11	Updated to a new datasheet format. Added a note for Recommended Operating Conditions.
2024-12-12	Rev.A.12	Updated the POD of TQFP7x7-48. Added the MSL in the Order Information.

Pin Configuration and Functions

TPAFE0532
TQFP7X7-48
Top View

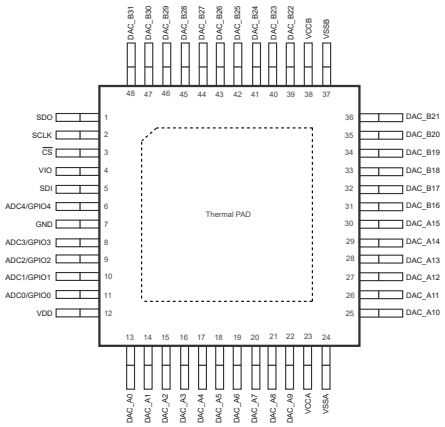


Table 1. Pin Functions

Pin No.	Name	I/O	Description
1	SDO	O	The SPI data output. The data is clocked out of the input shift register on each falling edge of SCLK.
2	SCLK	I	The SPI clock.
3	/CS	I	The active low serial data enable.
4	VIO	PWR	The IO supply voltage.
5	SDI	I	The SPI data input.
6 8~11	ADC4/ GPIO4 to ADC0/ GPIO0	I/O	The analog ADC inputs. These pins can be set to operate as GPIOs. The GPIO functions are as below: GPIO4: /DAV, the active low ADC data available indicator. GPIO3: /ADCTRIG, the active low external ADC conversion trigger. GPIO2: /ALARMOUT, the open drain global alarm output. GPIO1: /CLEARB, the active low DAC group B clear control signal. GPIO0: /CLEARA, the active low DAC group A clear control signal.
7	GND	GND	The ground supply.
12	VDD	PWR	The analog supply voltage.
13~22 25~30	DAC_A0 to DAC_A15	O	The DAC group A. These 16 DAC outputs share the same range and clamp levels.
23	VCCA	PWR	The positive analog power supply for DAC group A.
24	VSSA	PWR	The negative analog power supply for DAC group A.
31~36 39~48	DAC_B16 to DAC_B31	O	The DAC group B. These 16 DAC outputs share the same range and clamp levels.
37	VSSB	PWR	The negative analog power supply for DAC group A.

Pin No.	Name	I/O	Description
38	VCCB	PWR	The positive analog power supply for DAC group A.
	Thermal PAD		The thermal pad should be connected to PCB ground plane for good thermal performance.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
Supply Voltage	V_{DD} to GND	−0.3	6	V
	V_{IO} to GND	−0.3	6	V
	$V_{CC\ (A,\ B)}$ to GND	−0.3	12	V
	$V_{SS\ (A,\ B)}$ to GND	−12	0.3	V
	V_{CCA} to V_{SSA}	−0.3	12	V
	V_{CCB} to V_{SSB}	−0.3	12	V
Pin Voltage	DAC_A [0-15] Outputs to GND	V_{SSA} − 0.3	V_{CCA} + 0.3	V
	DAC_B [16-31] Ouputs to GND	V_{SSB} − 0.3	V_{CCB} + 0.3	V
	FlexIO Pins to GND	−0.3	V_{DD} + 0.3	V
	SPI Pins to GND	−0.3	V_{IO} + 0.3	V
	ADC Analog Input Current	−10	10	mA
T_J	Maximum Junction Temperature	−40	150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output diode current ratings are observed.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
Supply Voltage	V_{DD}	4.5		5.5	V
	V_{IO}	1.65		5.5	V
	$V_{CC\ (A,\ B)}$	4.5		11	V
	$V_{SS\ (A.\ B)}$	−11		−4.5	V

Parameter		Min	Typ	Max	Unit
	V_{CCA} − V_{SSA}	4.5		11	V
	V_{CCB} − V_{SSB}	4.5		11	V
Specifies Temperature Range		−40		125	℃
Operating Temperature Range		−40		125	℃

(1) For positive output, $V_{ss[a]}$ or $V_{ss[b]}$ should be connected to 0 V. For negative output, $V_{cc[a]}$ or $V_{cc[b]}$ should be connected to 0 V.

Thermal Information

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
TQFP7×7-EP48L	22.1	6.6	12.7 (top), 0.7 (bottom)	°C/W

Electrical Characteristics-DAC Specification

All test conditions: V_{DD} = 4.5 to 5.5 V, V_{IO} = 1.65 V to 3.6 V; V_{CC} = 4.5 V to 11 V, V_{SS} = GND for positive range; V_{CC} = GND, V_{SS} = −11 to −4.5 V for negative output range; over specified temperature range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
DAC DC Specifications					
Resolution		12			
Full-Scale Output Voltage Range	Power up or Reset Through Auto-Range Detection	−10		0	V
		−5		0	V
		0		5	V
		0		10	V
INL				±3	LSB
DNL				±1	LSB
Positive Output Range					
TUE	End point fit between codes 16 to 4031. DAC outputs unloaded.		±0.1	±0.5	%FSR
Total Error Temperature Drift	After one point calibration at 25℃. V_{OUT}: 2.5 V (10 V or 5 V range)		±0.03		%FSR
Offset Error	Full temp? End point fit towards value at code 000h		±2	±15	mV
Offset Error Temperature Drift			±2		ppm/℃
Gain Error	Full temp		±0.01	±0.45	%FSR
Gain Error Temperature Drift			±20		ppm/℃
Zero-Scale Error	Code = 000h Full temp		2	15	mV
Zero-Scale Error Temperature Drift			±2		ppm/℃
Full-Scale Error	Code = FFFh		±0.01	±0.45	%FSR
Full-Scale Error Temperature Drift			±20		ppm/℃
Negative Output Ranges					
TUE			±0.1	±0.5	%FSR
Total Error Temperature Drift			±0.03		%FSR
Offset Error	End point fit towards value at code FFFh		±2	±15	mV
Offset Error Temperature Drift			±2		ppm/℃
Gain Error			±0.01	±0.45	%FSR
Gain Error Temperature Drift			±20		ppm/℃
Zero-Scale Error	Code = FFFh		−2	25	mV
Zero-Scale Error Temperature Drift			±2		ppm/℃
Full-Scale Error	Code = 000h		±0.01	±0.45	%FSR

Parameter	Conditions	Min	Typ	Max	Unit
Full-Scale Error Temperature Drift			±20		ppm/℃
DAC Output Buffer Specifications					
Load Current	Source with 1-V headroom from V_{CC} With 25-mV variation		20		mA
	Sink with 1-V headroom from V_{SS} with 25-mV variation		20		mA
Short Circuit Current	Low current mode		±10		mA
	Normal mode (default)		±45		mA
Capacitive Load Stability	R_L = ∞		200		pF
DC Output Impedance	DAC code at mid-scale		1		Ω
Output Voltage Setting Time	Zero-scale to quarter full-scale step to within 2.5 mV R_L = 2 kΩ, C_l = 200 pF		7		µs
	1/4 to 3/4 scale settling to ±0.5 LSB. R_L = 2 kΩ, C_l = 200 pF		11		µs
Slew Rate	Transition: 1/4 to 3/4 scale, 10% to 90%		0.5		V/µs
Output Noise	0.1 Hz to 10 Hz, DAC code at mid-scale		250		µVpp
Output Noise Density	1 kHz, DAC code at mid-scale		1000		nV/√Hz
AC PSRR	DAC code at mid-scale. Frequency = 60 Hz, amplitude = 200 mVpp superimposed on V_{DD}		60		dB
	DAC code at mid-scale. Frequency = 60 Hz, amplitude = 200 mVpp superimposed on V_{CC}		85		dB
	DAC code at mid-scale. Frequency = 60 Hz, amplitude = 200 mVpp superimposed on V_{SS}		85		dB
DC PSRR	DAC code at mid-scale. ±5% variation on all supplies.		0.15		mV/V
Code Change Glitch Impulse	1-LSB change around major carrier		6		nV-s
Glitch Impulse Amplitude	1-LSB change around major carrier		4		mV
Power-on Overshoot	V_{SS} = GND, V_{CC} = 0 to +11 V, 2-ms ramp R_series = 5 ohm, C = 1 µF		50		mV
	V_{SS} = GND, V_{CC} = 0 to −11 V, 2-ms ramp R_series = 5 ohm, C = 1 µF		50		mV
Turn-on Overshoot	0~1/2 FS R_series = 5 ohm, C = 1 µF				mV
Channel to Channel DC Crosstalk	Measured channel at midscale.		1		mV

Parameter	Conditions	Min	Typ	Max	Unit
	Full scale output change on all other channels.				
Clamp Output Specifications					
Load Current	DAC output buffers inactive. Sink with 2-V headroom from V_{SS}	8			mA

Electrical Characteristics-ADC & TEMP Sensor Specification

All test conditions: V_{DD} = 4.5 to 5.5 V, V_{IO} = 1.65 V to 3.6 V; V_{CC} = 4.5 V to 11 V, V_{SS} = GND for positive range; V_{CC} = GND, V_{SS} = −11 to −4.5 V for negative output range; over specified temperature range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
ADC DC Specifications					
Resolution		12			
Full-Scale Input Range		0		$2 \times V_{REF}$	V
		0		V_{REF}	V
INL				±2	LSB
DNL				±1	LSB
Offset Error	After calibration			±5	LSB
Offset Error Match			±0.4		LSB
Offset Error Temperature Drift			4		ppm/℃
Gain Error			±0.01	±0.5	%FSR
Gain Error Match			±0.4		LSB
Gain Error Temperature Drift			4		ppm/℃
Input Capacitance			20		pF
Input Bias Current	Unselected ADC input			±10	μA
Conversion Time			1.875		μS
Acquisition Time	500-kSPS conversion rate				μS
Conversion Rate			430		kSPS
Throughput Rate	SCLK = 20 MHz SPI Update data rate			250	kSPS
Temperature Sensor Range					
Operating Range		−40		150	℃
Accuracy	T_J = −40~125℃		±2.5		℃
Resolution	LSB size		0.0625		℃
Update Time	T_J = −40~125℃		31.25		ms

Electrical Characteristics-General Specifications

All test conditions: V_{DD} = 4.5 to 5.5 V, V_{IO} = 1.65 V to 5.5 V; V_{CC} = 4.5 V to 11 V, V_{SS} = GND for positive range; V_{CC} = GND, V_{SS} = −11 to −4.5 V for negative output range; over specified temperature range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
GPIO Specifications					
$V_{IH\ LowVIO}$		0.7 × V_{IO}			V
$V_{IL\ LowVIO}$				0.3 × V_{IO}	V
Serial Interface Specifications					
$V_{IH\ LowVIO}$		0.7 × V_{IO}			V
$V_{IL\ LowVIO}$				0.3 × V_{IO}	V
Input Current			2		µA
Input Pin Capacitance			2		pF
V_{OH}	I_{source} = 0.2 mA	V_{IO} − 0.2			V
V_{OL}	I_{sink} = 0.2 mA			0.2	V
Output Pin Capacitance			2		pF
Pull up Resistor nCS			1		MΩ
Pull up Resistor SCLK			1		MΩ
Auto-Range Threshold Detector					
V_{SSTH}	Negative voltage range		−3.75		
V_{CCTH}	Positive voltage range		3		
Power Requirement					
I_{VDD}	All DAC at midscale code. ADC in fastest auto mode. Temperature sensor enabled.		20		mA
I_{VCC} [A,B]			10		mA
I_{VSS} [A,B]			10		mA
I_{VIO}			5		µA
I_{VDD}	Power-down mode		3		mA
I_{VCC} [A,B]			0.5		mA
I_{VSS} [A,B]			0.5		mA
I_{VIO}			5		µA

Timing Requirements

All test conditions: V_{DD} = 4.5 to 5.5 V, V_{IO} = 1.8 V to 3.6 V; V_{CC} = 4.5 V to 11 V, V_{SS} = GND for positive range; V_{CC} = GND, V_{SS} = −11 to −4.5 V for negative output range; over specified temperature range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
Serial Interface					
f (SCLK)				20	MHz
t_{PH} SCLK Pulse Width High		24.5			nS
t_{PL} SCLK Pulse Width Low		24.5			nS
t_{su} SDI Setup (1)		20			nS
t_h SDI Hold (1)		20			nS
$t_{(ODZ)}$ SDO Driven to Tri-State		0		25	nS
$t_{(OZD)}$ SDO Tri-State to Driven		1.5		30	nS
$t_{(OD)}$ SDO Output Delay		0		25	nS
$t_{su\ (cs)}$ /CS Setup (1)		20			nS
$t_{h\ (/cs)}$ /CS Hold (1)		20			nS
$t_{(IAG)}$ /CS High Time		20			nS

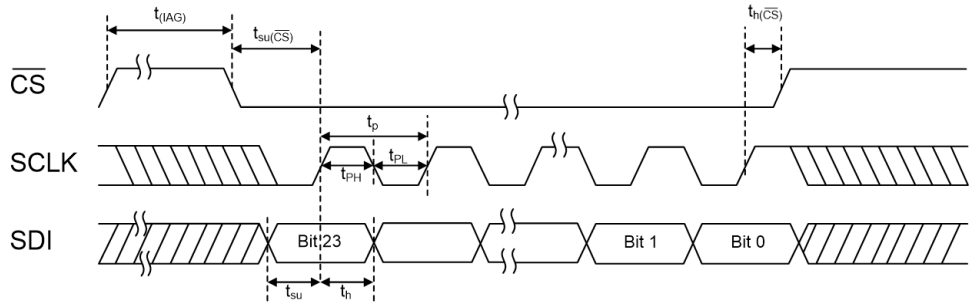


Figure 1. Serial Interface Write Timing Diagram

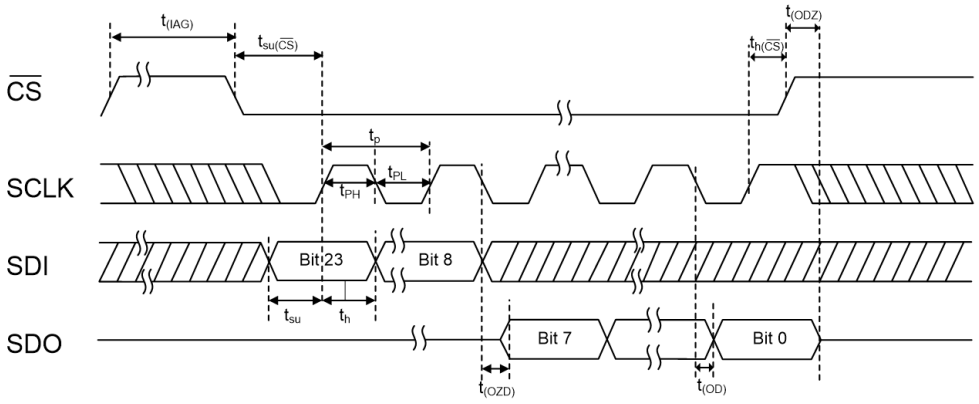


Figure 2. Serial Interface Read Timing Diagram

Detailed Description

Feature Description

Register Map

Address1	Type	Default	Register Name
0×00	R/W	30	Interface Configuration 0
0×01	R/W	0	Interface Configuration 1
0×02	R/W	3	Device Configuration
0×03	R	8	Chip Type
0×04	R	32	Chip ID (Low Byte)
0×05	R	5	Chip ID (High Byte)
0×06	R	3	Chip Version
0×07-0×0B	—	—	Reserved
0×0C	R	32	Manufacturer ID (Low Byte)
0×0D	R	1	Manufacturer ID (High Byte)
0×0E	—	—	Reserved
0×0F	R/W	0	Register Update
0×21E	R	0	Temperature Data (Low Byte)
0×21F	R	40	Temperature Data (High Byte)
0×220	R	0	ADC0-Data (Low Byte)
0×221	R	0	ADC0-Data (High Byte)
0×222	R	0	ADC1-Data (Low Byte)
0×223	R	0	ADC1-Data (High Byte)
0×224	R	0	ADC2-Data (Low Byte)
0×225	R	0	ADC2-Data (High Byte)
0×226	R	0	ADC3-Data (Low Byte)
0×227	R	0	ADC3-Data (High Byte)
0×228	R	0	ADC4-Data (Low Byte)
0×229	R	0	ADC4-Data (High Byte)
0×22A	R	0	ADC5-Data (Low Byte)
0×22B	R	0	ADC5-Data (High Byte)
0×22C-0×22D	—	—	Reserve
0×22E-0×22F	—	—	Reserve
0×230	R/W	0	DACA0-Data (Low Byte)
0×231	R/W	0	DACA0-Data (High Byte)
0×232	R/W	0	DACA1-Data (Low Byte)
0×233	R/W	0	DACA1-Data (High Byte)
0×234	R/W	0	DACA2-Data (Low Byte)

0×235	R/W	0	DACA2-Data (High Byte)
0×236	R/W	0	DACA3-Data (Low Byte)
0×237	R/W	0	DACA3-Data (High Byte)
0×238	R/W	0	DACA4-Data (Low Byte)
0×239	R/W	0	DACA4-Data (High Byte)
0×23A	R/W	0	DACA5-Data (Low Byte)
0×23B	R/W	0	DACA5-Data (High Byte)
0×23C	R/W	0	DACA6-Data (Low Byte)
0×23D	R/W	0	DACA6-Data (High Byte)
0×23E	R/W	0	DACA7-Data (Low Byte)
0×23F	R/W	0	DACA7-Data (High Byte)
0×240	R/W	0	DACA8-Data (Low Byte)
0×241	R/W	0	DACA8-Data (High Byte)
0×242	R/W	0	DACA9-Data (Low Byte)
0×243	R/W	0	DACA9-Data (High Byte)
0×244	R/W	0	DACA10-Data (Low Byte)
0×245	R/W	0	DACA10-Data (High Byte)
0×246	R/W	0	DACA11-Data (Low Byte)
0×247	R/W	0	DACA11-Data (High Byte)
0×248	R/W	0	DACA12-Data (Low Byte)
0×249	R/W	0	DACA12-Data (High Byte)
0×24A	R/W	0	DACA13-Data (Low Byte)
0×24B	R/W	0	DACA13-Data (High Byte)
0×24C	R/W	0	DACA14-Data (Low Byte)
0×24D	R/W	0	DACA14-Data (High Byte)
0×24E	R/W	0	DACA15-Data (Low Byte)
0×24F	R/W	0	DACA15-Data (High Byte)
0×250	R/W	0	DACB16-Data (Low Byte)
0×251	R/W	0	DACB16-Data (High Byte)
0×252	R/W	0	DACB17-Data (Low Byte)
0×253	R/W	0	DACB17-Data (High Byte)
0×254	R/W	0	DACB18-Data (Low Byte)
0×255	R/W	0	DACB18-Data (High Byte)
0×256	R/W	0	DACB19-Data (Low Byte)
0×257	R/W	0	DACB19-Data (High Byte)
0×258	R/W	0	DACB20-Data (Low Byte)
0×259	R/W	0	DACB20-Data (High Byte)
0×25A	R/W	0	DACB21-Data (Low Byte)

0×25B	R/W	0	DACB21-Data (High Byte)
0×25C	R/W	0	DACB22-Data (Low Byte)
0×25D	R/W	0	DACB22-Data (High Byte)
0×25E	R/W	0	DACB23-Data (Low Byte)
0×25F	R/W	0	DACB23-Data (High Byte)
0×260	R/W	0	DACB24-Data (Low Byte)
0×261	R/W	0	DACB24-Data (High Byte)
0×262	R/W	0	DACB25-Data (Low Byte)
0×263	R/W	0	DACB25-Data (High Byte)
0×264	R/W	0	DACB26-Data (Low Byte)
0×265	R/W	0	DACB26-Data (High Byte)
0×266	R/W	0	DACB27-Data (Low Byte)
0×267	R/W	0	DACB27-Data (High Byte)
0×268	R/W	0	DACB28-Data (Low Byte)
0×269	R/W	0	DACB28-Data (High Byte)
0×26A	R/W	0	DACB29-Data (Low Byte)
0×26B	R/W	0	DACB29-Data (High Byte)
0×26C	R/W	0	DACB30-Data (Low Byte)
0×26D	R/W	0	DACB30-Data (High Byte)
0×26E	R/W	0	DACB31-Data (Low Byte)
0×26F	R/W	0	DACB31-Data (High Byte)
0×310	R/W	0	ADC Configuration
0×311	R/W	60	False Alarm Configuration
0×312	R/W	0	GPIO Configuration
0×313	R/W	3F	ADC MUX Configuration
0×314	R/W	0	Hardware Reset
0×315	R/W	0	DAC Range
0×316	R/W	0	DAC Clear Enable 0
0×317	R/W	0	DAC Clear Enable 1
0×318	R/W	0	DAC Clear Enable 2
0×319	R/W	0	DAC Clear Enable 3
0×31A	R/W	0	DAC Clear Source 0
0×31B	R/W	0	DAC Clear Source 1
0×31C	R/W	0	ALARMOUT Source 0
0×31D	R/W	0	ALARMOUT Source1
0×370	R	0	Alarm Status 0
0×371	R	0	Alarm Status 1
0×372	R	8	General Status

0×373	R	0	DACA7~DACA0 Output Short
0×374	R	0	DACA15~DACA8 Output Short
0×375	R	0	DACB23~DACB16 Output Short
0×376	R	0	DACB31~DACB24 Output Short
0×377-0×379	—	—	Reserved
0×37A	R/W	3F	GPIO
0×37B	R/W	0	Auxillary
0×37C-0×37D	—	0	Reserved
0×37E	W		DAC broadcast Data (Low Byte)
0×37F	W	—	DAC broadcast Data (High Byte)
0×380	R/W	FF	LT-Upper-Thresh (Low Byte)
0×381	R/W	0	LT-Lower-Thresh (Low Byte)
0×382	R/W	FF	LT-Therm-Thres (Thermal Thut Down)
0×383	—	—	Reserved
0×384	R/W	FF	ADC0-Upper-Thresh (Low Byte)
0×385	R/W	0F	ADC0-Upper-Thresh (High Byte)
0×386	R/W	0	ADC0-Lower-Thresh (Low Byte)
0×387	R/W	0	ADC0-Lower-Thresh (High Byte)
0×388	R/W	FF	ADC1-Upper-Thresh (Low Byte)
0×389	R/W	0F	ADC1-Upper-Thresh (High Byte)
0×38A	R/W	0	ADC1-Lower-Thresh (Low Byte)
0×38B	R/W	0	ADC1-Lower-Thresh (High Byte)
0×38C	R/W	FF	ADC2-Upper-Thresh (Low Byte)
0×38D	R/W	0F	ADC2-Upper-Thresh (High Byte)
0×38E	R/W	0	ADC2-Lower-Thresh (Low Byte)
0×38F	R/W	0	ADC2-Lower-Thresh (High Byte)
0×390	R/W	FF	ADC3-Upper-Thresh (Low Byte)
0×391	R/W	0F	ADC3-Upper-Thresh (High Byte)
0×392	R/W	0	ADC3-Lower-Thresh (Low Byte)
0×393	R/W	0	ADC3-Lower-Thresh (High Byte)
0×394	R/W	FF	ADC4-Upper-Thresh (Low Byte)
0×395	R/W	0F	ADC4-Upper-Thresh (High Byte)
0×396	R/W	0	ADC4-Lower-Thresh (Low Byte)
0×397	R/W	0	ADC4-Lower-Thresh (High Byte)
0×398	R/W	FF	ADC5-Upper-Thresh (Low Byte)
0×399	R/W	0F	ADC5-Upper-Thresh (High Byte)
0×39A	R/W	0	ADC5-Lower-Thresh (Low Byte)
0×39B	R/W	0	ADC5-Lower-Thresh (High Byte)

0×39C-0×39F	—	—	Reserved
0×3A0	R/W	A	LT-Hysteresis
0×3A1	R/W	8	ADC0-Hysteresis
0×3A2	R/W	8	ADC1-Hysteresis
0×3A3	R/W	8	ADC2-Hysteresis
0×3A4	R/W	8	ADC3-Hysteresis
0×3A5	R/W	8	ADC4-Hysteresis
0×3A6	R/W	8	ADC5-Hysteresis
0×3A7 - 0×AD	—	—	Reserved
0×3AE	R/W	0	DAC Clear 0
0×3AF	R/W	0	DAC Clear 1
0×3B0	R/W	0	DAC Clear 2
0×3B1	R/W	0	DAC Clear 3
0×3B2	R/W	0	Power-Down 0
0×3B3	R/W	0	Power-Down 1
0×3B4	R/W	0	Power-Down 2
0×3B5	R/W	0	Power-Down3
0×3B6	R/W	0	Power-Down4
0×3B7 - 0×xBF	—	—	Reserved
0×3C0	R/W	77	ADC Trigger

Register Identification

Interface configuration: Address 0×00-0×02

Register name: interface configuration 0-address 0×00

Register Name	Address	Bit	Name	Function
Interface Config 0	0×30	7	SOFT_RESET	Soft reset (self clear)
				0: no action
				1: reset-resets everything except address 0×00, 0×01
		6	Reserved	Reserved for factory use
		5	ADDR-ASCEND	Address ascend
				0: descend-decrements address while streaming (address wrap from 0×7fff to 0×0000)
				1: ascend-increments address while streaming (address wrap from 0×0000 to 0×7fff)
		4	Reserved	Reserved for factory use
		3:00	Reserved	Reserved for factory use

(1) This register is not reset by SOFT_RESET.
(2) This register does not require update (address 0×0F).

Register name: interface configuration 1-address 0×01

Register Name	Address	Bit	Name	Function
Interface Config 1	0×01	7	SINGLE-INSTR	Single instruction enable
				0: streaming mode (default)
				1: single instruction
		6	Reserved	Reserved for factory use
		5	READBACK	Read Back
				0: DAC read back from active register (default)
				1: DAC read back from buffer register
		4	Reserved	Reserved for factory use
		3	Reserved	Reserved for factory use
		2	Reserved	Reserved for factory use
		1	Reserved	Reserved for factory use
		0	Reserved	Reserved for factory use

(1) This register is not reset by SOFT_RESET.
(2) This register does not require update (address 0×0F).

Register name: device configuration-address 0×02

Register Name	Address	Bit	Name	Function
Device Config	0×02	7:02	Reserved	Reserved for factory use
		1:00	POWER-MODE	Mode: 00: normal opertion-full power and full performance 11: sleep-lowest power, non-operational except SPI One time overwrite of the power-enable register (0×B2-0×B6)

Device identification: Address 0×03-0×0D

Register name: chip type-address 0×03

Register Name	Address	Bit	Name	Function
Chip Type	0×03	7:04	Reserved	Reserved for factory use
		3:00	CHIP-TYPE	Identifies the device as a precison analog monitor and control

Register name: chip ID low byte-address 0×04

Register Name	Address	Bit	Name	Function
Chip ID Low Byte	0×04	7:00	CHIPID-LOW	Chip ID. Low byte

Register name: chip ID high byte-address 0×05

Register Name	Address	Bit	Name	Function
Chip ID High Byte	0×05	7:00	CHIPID-HIGH	Chip ID. High byte

Register name: version ID-address 0×06

Register Name	Address	Bit	Name	Function
Version ID	0×06	7:00	VERSIONID	Version ID

Register name: manufacture ID low byte-address 0×0C

Register Name	Address	Bit	Name	Function
Manufacture ID Low Byte	0×0C	7:00	VENDORID-LOW	Manufacture ID. Low byte

Register name: manufacture ID high byte-address 0×0D

Register Name	Address	Bit	Name	Function
Manufacture ID High Byte	0×0D	7:00	VENDORID-HIGH	Manufacture ID. High byte

Register update (buffered register): Address 0×0F

Register name: register update-address 0×0F (self clearing)

Register Name	Address	Bit	Name	Function
Register Update	0×0F	7:06	Reserved	Reserved for factory use
		5	TEMP-UPDATE	When set transfers the latest temperature conversion data to the LT data register.
		4	ADC-UPDATE	When set transfers the latest ADC conversion data to the ADC data registers.
				This function is needed when operating the ADC in autocycle mode.
		3:01	Reserved	Reserved for factory use
		0	DAC-UPDATE	Update (self clearing)
				0: disabled
				1: enabled-transfers data from buffers to active registers (DAC register only)
				Reserved for factory use

General device configuration: Address 0×310-0×317

Register name: ADC configuration-address 0×10 (R/W)

<table>
<tr><th>Register Name</th><th>Address</th><th>Bit</th><th>Name</th><th colspan="4">Function</th></tr>
<tr><td rowspan="15">ADC Config</td><td rowspan="15">0×310</td><td rowspan="3">7</td><td rowspan="3">CMODE</td><td colspan="4">ADC conversion mode Bit. This bit selects the ADC conversion mode.</td></tr>
<tr><td colspan="4">0: direct mode. The analog inputs specified in the ADC channel registers are converted sequentially on time. When one set of conversions is complete, the ADC is idle and waits for a new trigger.</td></tr>
<tr><td colspan="4">1: auto mode. The analog inputs specified in the ADC channels registers are converted sequentially and repeatedly. When one set of conversions is complete, the ADC multiplexer returns to the first channel and repeats the process. The ADC-UPDATE bit in register 0×0F must be used to initiate the transfer of the latest conversion data to the ADC Data registers.</td></tr>
<tr><td rowspan="5">6:05</td><td rowspan="5">CONV-RATE [1:0]</td><td colspan="4">ADC Conversion rate</td></tr>
<tr><td>CR</td><td>tacq [ns]</td><td>tconv [ns]</td><td>throughput</td></tr>
<tr><td>00</td><td>125</td><td>1875</td><td>500 kSPS</td></tr>
<tr><td>01</td><td>2125</td><td>1875</td><td>250 kSPS</td></tr>
<tr><td>10</td><td>6125</td><td>1875</td><td>125 kSPS</td></tr>
<tr><td>11</td><td>30125</td><td>1875</td><td>31.25 kSPS</td></tr>
<tr><td rowspan="3">4</td><td rowspan="3">ADC-RANGE</td><td colspan="4">ADC Range selection bit</td></tr>
<tr><td colspan="4">0: 0-5 V</td></tr>
<tr><td colspan="4">1: 0-2.5 V</td></tr>
<tr><td>3</td><td>ADC-CAL</td><td colspan="4">Set to 1 enable offset calibration sequence upon ADC conversion startup (however offset calibration always runs once on the first trigger after power-up).</td></tr>
<tr><td>2</td><td>Reserved</td><td colspan="4">Reserved for factory use</td></tr>
<tr><td>1</td><td>SDOZDD</td><td colspan="4">SDIO/SDO Z-to-driven delay Increase. Increases SDIO/SDO tri-state to driven timing by 2 ns to reduce bus contention on applications where it is critical.</td></tr>
<tr><td>0</td><td>Reserved</td><td colspan="4">Reserved for factory use</td></tr>
</table>

Register name: false alarm configuration-address 0×311

Register Name	Address	Bit	Name	Function
ADC Config	0×311	7:05	CH-FALR-CT	False alram protection for ADC channels
				CH-FALR-CT N CONSECUTIVE SIMPLE
				000: 1
				001: 4
				010: 8
				011: 16 (default)
				100: 32
				101: 64
				110: 128
				111: 256
		4	Reserved	Reserved for factory use
		3:01	TEMP-FLAR-CT	False alarm protection senso high and low limits
				TEMP-FLAR-CT N CONSECUTIVE SIMPLE
				000: 1 (default)
				001: 2
				011: 3
				111: 4
				others :1
		0	Reserved	Reserved for factory use

Register name: GPIO configuration-address 0×312

Register Name	Address	Bit	Name	Function
GPIO Config	0×312	7:06	Reserved	Reserved for factory use
		5	EN-ALARMIN	/ALARMIN pin enable
				0: GPIO5 operation (default)
				1: /ALARMIN operation
		4	EN-DAV	/DAV pin enable
				0: GPIO4 operation enable (default)
				1: /DAV opertion
		3	EN-ADCTRIG	/ADCTRIG pin enable
				0: GPIO3 operation enable (default)
				1: /ADCTRIG operation
GPIO Config	0×312	2	EN-ALARMOUT	/ALARMOUT pin enable
				0: GPIO2 operation enable
				1: /ALARMOUT operation (default)

		1	EN-CLR-B	/CLEAR-B pin enable
				0: GPIO1 operation (default)
				1: /CLEAR operation for DAC_B group DACs
		0	EN-CLR-A	/CLEAR-A pin enable
				0: GPIO1 operation (default)
				1: /CLEAR operation for DAC_A group DACs

Register name: ADC MUX configuration-address 0×313

Register Name	Address	Bit	Name	Function
ADC MUX Config	0×313	7:06	Reserved	Reserved for factory use
		5	CH5	When set to 1, the corresponding analog input channel ADCn is accessed during an ADC conversion cycle. When set to 1, the corresponding bit in GPIO configuration register is ignored, and the altermate GPIO function is blocked.
		4	CH4	When cleared to 0, the corresponding input channel ADCn is ignored during an ADC conversion cycle. When set to 0, the corresponding bit in the GPIO configuration register is effective.
		3	CH3	
		2	CH2	
		1	Ch1	
		0	CH0	

Register name: hardware reset-address 0×314

Register Name	Address	Bit	Name	Function
Hardware Reset	0×314	7:00	HARD-RESET	Executes a full power-on-reset, reset all registers to their defaults. When set to reserved code 0×AD resets the device to its default,power-on-reset state.

DAC configuration: Address 0×315-0×31D

Register name: DAC range-address 0×315

Register Name	Address	Bit	Name	Function	
DAC Range 0	0×315	7	DAC-LC-B	Set to 1 enable low-current mode of the DACs group B	
		6:04	DAC-RANGEB	DAC group B output voltage seletion. Overrides output range set by the auto-range detection circuit	
				DAC-RANGE	DAC Group B Output
				0xx	range set by auto-range detection circuit
				100	−10 V to 0 V
				101	−5 V to 0 V
				110	0 V to 10 V
				111	0 V to 5 V
		3	DAC-LC-A	Set to 1 enable low-current mode of the DACs group A	
		2:00	DAC-RANGEA	AC group A output voltage seletion. Overrides output range set by the auto-range detection circuit	
				DAC-RANGE	DAC Group A Output
				0xx	range set by auto-range detection circuit
				100	−10 V to 0 V
				101	−5 V to 0 V
				110	0 V to 10 V
				111	0 V to 5 V

Register name: DAC clear enable 0-address 0×316

Register Name	Address	Bit	Name	Function
DAC Clear Enable 0	0×316	7	CLREN-A7	This register determines which DACs go into clear state when a clear event is detected as configured in the DA-CLEAR-SOURCE registers.
		6	CLREN-A6	If CLRENn = 1, DAC_n is forced into a clear state with a clear event.
		5	CLREN-A5	If CLRENn = 0, a clear event does not affect the state of DAC_n.
		4	CLREN-A4	
		3	CLREN-A3	
		2	CLREN-A2	
		1	CLREN-A1	
		0	CLREN-A0	

Register name: DAC clear enable 1-address 0×317

Register Name	Address	Bit	Name	Function
DAC Clear Enable 1	0×317	7	CLREN-A15	This register determines which DACs go into clear state when a clear event is detected as configured in the DA-CLEAR-SOURCE registers.
		6	CLREN-A14	If CLRENn = 1, DAC_n is forced into a clear state with a clear event.
		5	CLREN-A13	If CLRENn = 0, a clear event does not affect the state of DAC_n.
		4	CLREN-A12	
		3	CLREN-A11	
		2	CLREN-A10	
		1	CLREN-A9	
		0	CLREN-A8	

Register name: DAC clear enable 2-address 0×318

Register Name	Address	Bit	Name	Function
DAC Clear Enable 2	0×318	7	CLREN-B23	This register determines which DACs go into clear state when a clear event is detected as configured in the DA-CLEAR-SOURCE registers.
		6	CLREN-B22	If CLRENn = 1, DAC_n is forced into a clear state with a clear event.
		5	CLREN-B21	If CLRENn = 0, a clear event does not affect the state of DAC_n.
		4	CLREN-B20	
		3	CLREN-B19	
		2	CLREN-B18	
		1	CLREN-B17	
		0	CLREN-B16	

Register name: DAC clear enable 3-address 0×319

Register Name	Address	Bit	Name	Function
DAC Clear Enable 3	0×319	7	CLREN-B31	This register determines which DACs go into clear state when a clear event is detected as configured in the DA-CLEAR-SOURCE registers.
		6	CLREN-B30	If CLRENn = 1, DAC_n is forced into a clear state with a clear event.
		5	CLREN-B29	If CLRENn = 0, a clear event does not affect the state of DAC_n.
		4	CLREN-B28	
		3	CLREN-B27	
		2	CLREN-B26	
		1	CLREN-B25	
		0	CLREN-B24	

Register name: DAC clear source 0-address 0×31A

Register Name	Address	Bit	Name	Function
DAC Clear Source 0	0×31A	7	REF-ALR-CLR	This register selects which alarm forces DACs into a clear state, regardless of which DAC operation mode is active, auto or manual. In order for DAC_n to go into clear mode, it must be enabled in the DAC clear enable registers.
		6	ALMIN-ALR-CLR	
		5	ADC5-ALR-CLR	
		4	ADC4-ALR-CLR	
		3	ADC3-ALR-CLR	
		2	ADC2-ALR-CLR	
		1	ADC1-ALR-CLR	
		0	ADC0-ALR-CLR	

Register name: DAC clear source 1-address 0×31B

Register Name	Address	Bit	Name	Function
DAC Clear Source 1	0×31B	7:03	Reserved	Reserved for factory use
		2	THERM-ALR-CLR	This register selects which alarm forces DACs into a clear state, regardless of which DAC operation mode is active, auto or manual. In order for DAC_n to go into clear mode, it must be enabled in the DAC clear enable registers.
		1	LT-HIGH-ALR-CLR	
		0	LT-LOW-ALR-CLR	

Register name: ALARMOUT source 0-address 0×31C

Register Name	Address	Bit	Name	Function
ALARMOUT Source 0	0×31C	7	REF-ALR-OUT	This register selects which alarms can active the /ALARMOUT pin. The /ALARMOUT must be enabled for this function to take effect.
		6	ALMIN-ALR-OUT	
		5	ADC5-CLR-OUT	
		4	ADC4-CLR-OUT	
		3	ADC3-CLR-OUT	
		2	ADC2-CLR-OUT	
		1	ADC1-CLR-OUT	
		0	ADC0-CLR-OUT	

Register name: ALARMOUT source 1-address 0×31D

Register Name	Address	Bit	Name	Function
ALARMOUT Source 1	0×31D	7:04	Reserved	Reserved for factory use
		3	ALARM-LATCH-DIS	Alarm latch disable bit.
				When cleared to 0, the alarm bits are latched. When an alarm occurs, the corresponding alarm bit is set to 1 . The alarm bit remains until the error condition subsides and the alarm register is read. Before reading, the alarm bit is not cleared even if the alarm condition disappears.
				When set to 1, the alarm bits are not latched. When the alarm condition subsides, the alarm bits are cleared regardless of whether the alarm bits have been read or not.
		2	THERM-ALR-OUT	This register selects which alarms can active the /ALARMOUT pin. The / ALARMOUT must be enabled for this function to take effect.
		1	LT-HIGH-ALR-OUT	
		0	LT-LOW-ALR-OUT	

ADC and temperature data: Address 0×21E-0×22B

Register name: temperature data (low byte) -address 0×21E

Register Name	Address	Bit	Name	Function
Temp Data (Low)	0×21E	7:04	TEMP-DATA [3:0]	Stores the temperature sensor in decimal data.
		3:00	Reserved	Reserved for factory use

Register name: temperature data (high byte) -address 0×21F

Register Name	Address	Bit	Name	Function
Temp Data (High)	0×21F	3:00	TEMP-DATA	Stores the temperature sensor
				Integer data

Register name: ADCn data (low byte) -address 0×220-0×22B

Register Name	Address	Bit	Name	Function
ADCn Data (Low)	0×220-0×22B	7:00	ADCn-DATA (7:0)	Stores the 12-bit ADCn conversion results in straight binary format.

Register name: ADCn data (high byte) -address 0×220-0×22B

Register Name	Address	Bit	Name	Function
ADCn Data (High)	0×220-0×22B	7:00	ADCn-DATA (7:0)	Stores the 12-bit ADCn conversion results in straight binary format.

DAC data: Address 0×230-0×26F

Register name: DACn data (low byte) -address 0×230-0×26F

Register Name	Address	Bit	Name	Function
DACn Data (Low)	0×230-0×26F	7:00	DACn-DATA	Stores the 12-bit data to be loaded to the DAC_n latches in straight binary format.
				The straight binary format is used for all DAC ranges.

Register name: DACn data (high byte) -address 0×230-0×26F

Register Name	Address	Bit	Name	Function
DACn Data (High)	0×230-0×26F	7:04	Reserved	Reserved for factory use
		3:00	ADCn-DATA (11:8)	Stores the 12-bit data to be loaded to the DAC_n latches in straight binary format.
				The straight binary format is used for all DAC ranges.

Status register: Address 0×370-0×372

Register name: alarm status 0-address 0×370

Register Name	Address	Bit	Name	Function
Alarm Status 0	0×370	7	REF-ALR	REF-ALR = 1 when the internal reference voltage is less than 2.2 V.
		6	ALMIN-ALR	ALARMIN = 1 if the /ALARMIN pin is enabled and set high.
		5	ADC5-ALR	ADC5-ALR = 1 when out of the range defined by the corresponding threshold registers.
				ADC5-ALR = 0 when the analog input is not out of the specified range.
		4	ADC4-ALR	ADC4-ALR = 1 when out of the range defined by the corresponding threshold registers.
				ADC4-ALR = 0 when the analog input is not out of the specified range.
		3	ADC3-ALR	ADC3-ALR = 1 when out of the range defined by the corresponding threshold registers.
				ADC3-ALR = 0 when the analog input is not out of the specified range.
		2	ADC2-ALR	ADC2-ALR = 1 when out of the range defined by the corresponding threshold registers.
				ADC2-ALR = 0 when the analog input is not out of the specified range.
		1	ADC1-ALR	ADC1-ALR = 1 when out of the range defined by the corresponding threshold registers.
				ADC1-ALR = 0 when the analog input is not out of the specified range.
		0	ADC0-ALR	ADC0-ALR = 1 when out of the range defined by the corresponding threshold registers.
				ADC0-ALR = 0 when the analog input is not out of the specified range.

Register name: alarm status 1-address 0×371

Register Name	Address	Bit	Name	Function
Alarm Status 1	0×371	7:03	Reserved	Reserved for factory use
		2	THERM-ALR	Thermal alarm flag. When the die temperature is equal to or greater than the thermal threshold, the bit is set 1, and the THERM-ALR flag actives. The on-chip temperature senor (LT) monitors the die temperature. If LT is disabled, the THERM-ALR bit is always 0.
		1	LT-HIGH-ALR	LT-LOW-ALR = 1 when the temperature sensor is out of the range defined by the upper threshold.
		0	LT-LOW-ALR	LT-LOW-ALR = 1 when the temperature sensor is out of the range defined by the lower threshold.

Register name: alarm status 1-address 0×372

Register Name	Address	Bit	Name	Function
General Status	0×372	7	VCCB	This bit is the VCC detection output for DAC group B. It doesn't affect the auto-range detection result, and is used for information only.
		6	VCCA	This bit is the VCC detection output for DAC group A. It doesn't affect the auto-range detection result, and is used for information only.
		5	VSSB	This bit is the auto-range detection output for DAC group B.
				0: 0 V to 5 V
				1: −10 V to 0 V
		4	VSSA	This bit is the auto-range detection output for DAC group A.
				0: 0 V to 5 V
				1: −10 V to 0 V
		3	ADC_READY	ADC Ready indicator, ADC-READY must be 1 in order for the ADC to respond to a trigger to begin conversions.
				ADC-READY = 1 means the ADC is ready (waiting) to be triggered. At power-up, it remains not ready (0) until the ADC is powered up (PADC set to 1) and at least one ADC channel is enabled. If there is any write that would stop the ADC, ADC-READY becomes 0 until the device completes processing of these changes/updates. Then if PADC = 1 and at least one channel is enabled, ADC-REDAY returns to 1.
				Once a trigger is received and the ADC begins conversions, the ADC-READY bit become 0.
		2	LT-BUSY	Temperature sensor busy indicator
		1	GALR	Global alarm bit
				This bit is the OR function or all individual alarm bits of the status register. This bit is set to 1 when any alarm condition occurs and remains set until the status register is read. This bit is cleared after reading the Status Register
		0	DAVF	ADC Data available flag bit, direct mode only. It is always cleared in auto mode
				0: ADC conversion is in progress or ADC is in auto mode.
				1: ADC conversion are complete and new data is available.

Register name: DAC output short-address 0×373-0×376

DACA7-DACA0 output short address: 0×373

Register Name	Address	Bit	Name	Function
Power Enable 3	0×373	7	DAC-A7 short	The bit is set to 1 if corresponding DAC is detected to be shorted.
		6	DAC-A6 short	The bit is not latched.
		5	DAC-A5 short	
		4	DAC-A4 short	
		3	DAC-A3 short	
		2	DAC-A2 short	
		1	DAC-A1 short	
		0	DAC-A0 short	

DACA15-DACA8 output short address: 0×374

Register Name	Address	Bit	Name	Function
Power Enable 3	0×374	7	DAC-A15 short	The bit is set to 1 if corresponding DAC is detected to be shorted.
		6	DAC-A14 short	The bit is not latched.
		5	DAC-A13 short	
		4	DAC-A12 short	
		3	DAC-A11 short	
		2	DAC-A10 short	
		1	DAC-A9 short	
		0	DAC-A8 short	

DACB7-DACB0 output short address: 0×375

Register Name	Address	Bit	Name	Function
Power Enable 3	0×375	7	DAC-B23 short	The bit is set to 1 if corresponding DAC is detected to be shorted.
		6	DAC-B22 short	The bit is not latched.
		5	DAC-B21 short	
		4	DAC-B20 short	
		3	DAC-B19 short	
		2	DAC-B18 short	
		1	DAC-B17 short	
		0	DAC-B16 short	

DACB31-DACB23 output short address: 0×376

Register Name	Address	Bit	Name	Function
Power Enable 3	0×376	7	DAC-B31 short	The bit is set to 1 if corresponding DAC is detected to be shorted.
		6	DAC-B30 short	The bit is not latched.
		5	DAC-B29 short	
		4	DAC-B28 short	
		3	DAC-B27 short	
		2	DAC-B26 short	
		1	DAC-B25 short	
		0	DAC-B24 short	

GPIO data: Address 0×37A

Register name: GPIO-address 0×37A

Register Name	Address	Bit	Name	Function
GPIO	0×37A	7:06	Reserved	For write operation, the GPIO pin operates as an output. Writing a 1 to the GPIO-n bit sets the GPIO-n pin to high impedance. Writing a 0 sets the GPIO-n pin to logic low-alarm.
		5	GPIO-5	For read operations, the GPIO pin operates as an input. Read the GPIO-n bit to receive the status of the GPIO-n pin.
		4	GPIO-4	After power-on reset, or any forced hardware or software reset, the GPIO-n bit pin is in a high impedance state.
		3	GPIO-3	
		2	GPIO-2	
		1	GPIO-1	
		0	GPIO-0	

DAC broadcast data: Address 0×37E-0×37F

Register name: DAC broadcast data (low byte)-address 0×37E

Register Name	Address	Bit	Name	Function
DAC Broadcast Data (Low)	0×37E	7:00	DAC-BROADCAST-DATA (7:0)	Write to this register sets all DACn-Data low byte buffers to specified code.

Register name: DAC broadcast data (high byte)-address 0×37F

Register Name	Address	Bit	Name	Function
DAC Broadcast Data (High)	0×37F	7:04	Reserved	Reserved for factory use
		3:00	DAC-BROADCAST-DATA (11:8)	Write to this register sets all DACn-Data high byte buffers to specified code.

Out-of-range ADC threshold: Address 0×380-0×39B

Register name: LT upper thresh-address 0×380

Register Name	Address	Bit	Name	Function
LT Upper Thresh	0×380	7:00	THRU-LT (7:0)	Set 8-bit upper threshold value for the local temperature sensor.

Register name: LT lower thresh-address 0×381

Register Name	Address	Bit	Name	Function
LT Lower Thresh	0×381	7:00	THRL-LT (7:0)	Set 8-bit lower threshold value for the local temperature sensor.

Register name: therm thresh-address 0×382

Register Name	Address	Bit	Name	Function
Therm Thresh	0×382	7:00	THRU-THERM (7:0)	Set 8-bit die thermal threshold value for the local temperature sensor.

Register name: ADCn Upper Thresh (low byte) -address 0×384-0×39B

Register Name	Address	Bit	Name	Function
ADCn Upper Thresh (Low)	0×384-0×39B	7:00	THRUn (7:0)	Sets 12-bit upper threshold value for the ADCn channel in straight binary format.

Register name: ADCn upper thresh (high byte) -address 0×384-0×39B

Register Name	Address	Bit	Name	Function
ADCn Upper Thresh (High)	0×384-0×39B	7:04	Reserved	Reserved for factory use
		3:00	THRUn (11:8)	Sets 12-bit upper threshold value for the ADCn channel in straight binary format.

Register name: ADCn Lower Thresh (low byte) -address 0×384-0×39B

Register Name	Address	Bit	Name	Function
ADCn Lower Thresh (Low)	0×384-0×39B	7:00	THRUn (7:0)	Sets 12-bit lower threshold value for the ADCn channel in straight binary format.

Register name: ADCn Lower Thresh (high byte) -address 0×384-0×39B

Register Name	Address	Bit	Name	Function
ADCn Lower Thresh (High)	0×384-0×39B	7:04	Reserved	Reserved for factory use
		3:00	THRUn (11:8)	Sets 12-bit lower threshold value for the ADCn channel in straight binary format.

Hysteresis: Address 0×3A0-0×3A6

Register name: Therm Hysteresis-address 0×3A0

Register Name	Address	Bit	Name	Function
Thermal Hysteresis	0×3A0	7:00	THERM-HYST (7:0)	Hysteresis of die thermal temperature sensor, 1°C per step.

Register name: Therm Hysteresis-address 0×3A1-0×3A6

Register Name	Address	Bit	Name	Function
ADCn Hysteresis	0×3A6	7	Reserved	Reserved for factory use
		6:00	HYSTn (6:0)	Hysteresis of general purpose ADCn, 1 LSB per step

Power-down register: Address 0×3AE-0×3B6

Register name: DAC clear 0-address 0×3AE

Register Name	Address	Bit	Name	Function
DAC Clear 0	0×3AE	7	CLR-A7	This register uses software to force the DAC into a clear state.
		6	CLR-A6	
		5	CLR-A5	If CLRn = 1, DAC_n is forced into a clear state.
		4	CLR-A4	
		3	CLR-A3	If CLRn = 0, DAC_n is restored to normal operation.
		2	CLR-A2	
		1	CLR-A1	
		0	CLR-A0	

Register name: DAC clear 1-address 0×3AF

Register Name	Address	Bit	Name	Function
DAC Clear 1	0×3AF	7	CLR-A15	This register uses software to force the DAC into a clear state.
		6	CLR-A14	
		5	CLR-A13	If CLRn = 1, DAC_n is forced into a clear state.
		4	CLR-A12	
		3	CLR-A11	If CLRn = 0, DAC_n is restored to normal operation
		2	CLR-A10	
		1	CLR-A9	
		0	CLR-A8	

Register name: DAC clear 2-address 0×3B0

Register Name	Address	Bit	Name	Function
DAC Clear 2	0×3B0	7	CLR-B23	This register uses software to force the DAC into a clear state.
		6	CLR-B22	
		5	CLR-B21	If CLRn = 1, DAC_n is forced into a clear state.
		4	CLR-B20	
		3	CLR-B19	If CLRn = 0, DAC_n is restored to normal operation
		2	CLR-B18	
		1	CLR-B17	
		0	CLR-B16	

Register name: DAC clear 3-address 0×3B1

Register Name	Address	Bit	Name	Function
DAC Clear 3	0×3B1	7	CLR-B31	This register uses software to force the DAC into a clear state.
		6	CLR-B30	
		5	CLR-B29	If CLRn = 1, DAC_n is forced into a clear state.
		4	CLR-B28	
		3	CLR-B27	If CLRn = 0, DAC_n is restored to normal operation
		2	CLR-B26	
		1	CLR-B25	
		0	CLR-B24	

Register name: power enable 0-address 0×3B2

Register Name	Address	Bit	Name	Function
Power Enable 0	0×3B2	7	PDAC-A7	After power-on or reset, all bits in the power-down register are cleared to the default value, and all the components controlled by this register are either powered-down or off. The power-down register allows the host to manage the TPAFE0532 power dissipation. When not required, the ADC, temperature sensor, internal reference,and any of the DACs can be put into an inactive low-power mode to reduce current drain from the supply. The bits in the power-down register control this power-down function. Set the respective bit to 1 to active the corresponding function.
		6	PDAC-A6	
		5	PDAC-A5	
		4	PDAC-A4	
		3	PDAC-A3	
		2	PDAC-A2	
		1	PDAC-A1	
		0	PDAC-A0	

Register name: power enable 1-address 0×3B3

Register Name	Address	Bit	Name	Function
Power Enable 1	0×3B3	7	PDAC-A15	After power-on or reset, all bits in the power-down register are cleared to the default value, and all the components controlled by this register are either powered-down or off. The power-down register allows the host to manage the TPAFE0532 power dissipation. When not required, the ADC, temperature sensor, internal reference,and any of the DACs can be put into an inactive low-power mode to reduce current drain from the supply. The bits in the power-down register control this power-down function. Set the respective bit to 1 to active the corresponding function.
		6	PDAC-A14	
		5	PDAC-A13	
		4	PDAC-A12	
		3	PDAC-A11	
		2	PDAC-A10	
		1	PDAC-A9	
		0	PDAC-A8	

Register name: power enable 2-address 0×3B4

Register Name	Address	Bit	Name	Function
Power Enable 2	0×3B4	7	PDAC-B23	After power-on or reset, all bits in the power-down register are cleared to the default value, and all the components controlled by this register are either powered-down or off. The power-down register allows the host to manage the TPAFE0532 power dissipation. When not required, the ADC, temperature sensor, internal reference,and any of the DACs can be put into an inactive low-power mode to reduce current drain from the supply. The bits in the power-down register control this power-down function. Set the respective bit to 1 to active the corresponding function.
		6	PDAC-B22	
		5	PDAC-B21	
		4	PDAC-B20	
		3	PDAC-B19	
		2	PDAC-B18	
		1	PDAC-B17	
		0	PDAC-B16	

Register name: power enable 3-address 0×3B5

Register Name	Address	Bit	Name	Function
Power Enable 3	0×3B5	7	PDAC-B31	After power-on or reset, all bits in the power-down register are cleared to the default value, and all the components controlled by this register are either powered-down or off. The power-down register allows the host to manage the TPAFE0532 power dissipation. When not required, the ADC, temperature sensor, internal reference,and any of the DACs can be put into an inactive low-power mode to reduce current drain from the supply. The bits in the power-down register control this power-down function. Set the respective bit to 1 to active the corresponding function.
		6	PDAC-B30	
		5	PDAC-B29	
		4	PDAC-B28	
		3	PDAC-B27	
		2	PDAC-B26	
		1	PDAC-B25	
		0	PDAC-B24	

Register name: power enable 4-address 0×3B6

Register Name	Address	Bit	Name	Function
Power Enable 4	0×3B6	7:03	Reserved	Reserved for factory use
		2	PTEMP	After power-on or reset, all bits in the power-down register are cleared to the default value, and all the components controlled by this register are either powered-down or off. The power-down register allows the host to manage the TPAFE0532 power dissipation. When not required, the ADC, temperature sensor, internal reference,and any of the DACs can be put into an inactive low-power mode to reduce current drain from the supply. The bits in the power-down register control this power-down function. Set the respective bit to 1 to active the corresponding function.
		1	Reserved	
		0	PADC	

ADC trigger: Address 0×3C0

Register name: ADC trigger-address 0×3C0

Register Name	Address	Bit	Name	Function
ADC Trigger	0×3C0	7:01	Reserved	Reserved for factory use
		0	ICONV	Internal ADC conversion bit. Set this bit to 1to start the ADC conversion internally. The bit is automatically cleared to 0 after the ADC conversion starts.

Application and Implementation

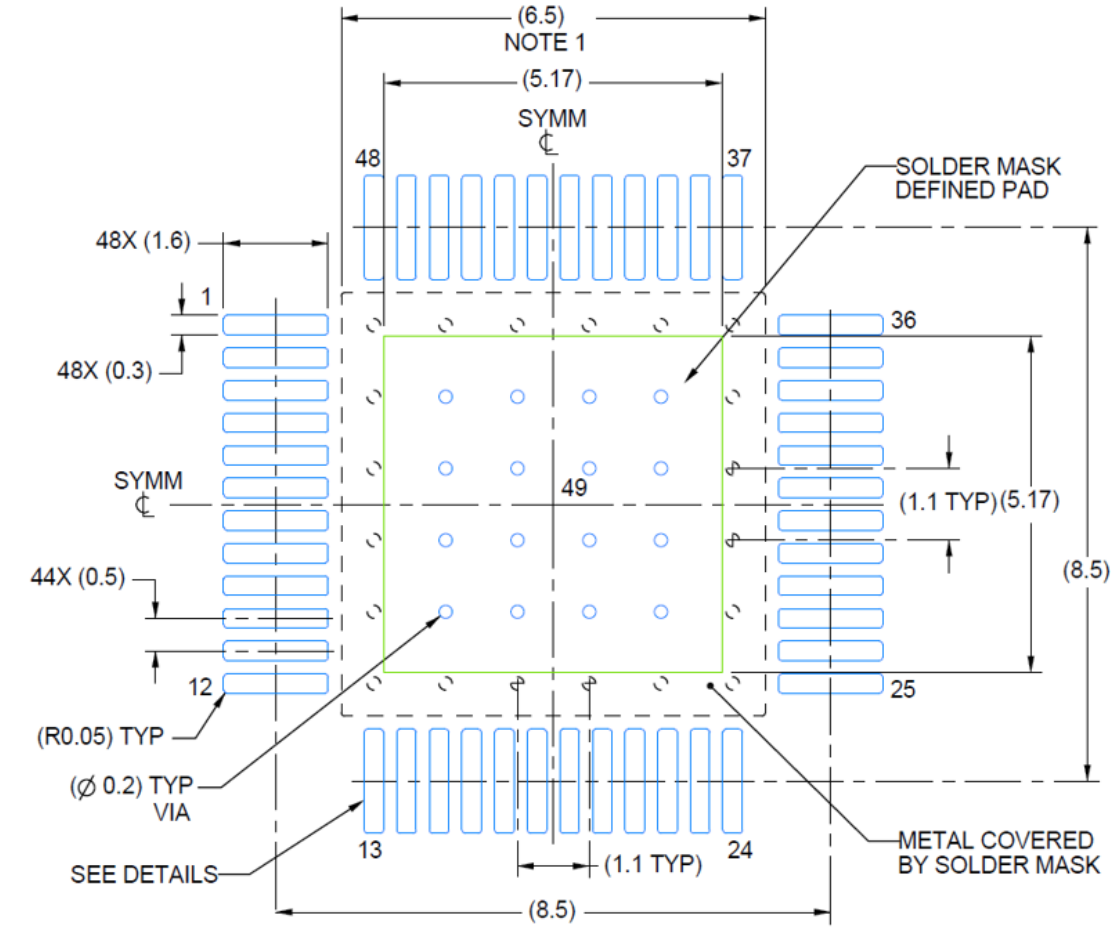
> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Note

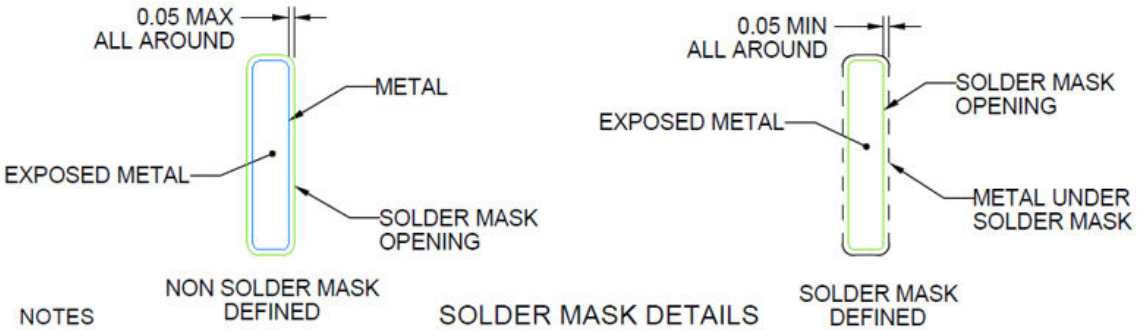
1. The series resistor and the filter cap are recommended to be added at DAC output, and then DAC stability could be assured when driving large load such as GaN FET.
   R_series = 5 ohm, C = 1 μF are recommended.
2. The filter cap should be added on each supply voltage to make sure the device works in stable condition.
3. When writing following registers, it is suggested to use single mode, or write single byte in the stream mode. If multi bytes are written once in stream mode, the SPI speed should be lower than 10 MHz, or wait 800 nS between each two bytes written if SPI speed is larger than 10 MHz.
   - 0×0310 (ADC/SPI Configuration), 0×0311 (False Alarm Configuration),
   - 0×0380 (LT-Upper-Thresh (Low byte)) ~ 0×0382 (LT-Therm-Thresh (Low byte)),
   - 0×0384 (ADC0-Upper-Thresh (Low byte) ~ 0×39b (ADC5-Lower-Thresh (High byte)),
   - 0×03A1 (Therm Hystersis) ~ 0×03A6 (ADC5-Hystersis),
   - 0×03B2 (Power-Enable 0) ~ 0×03B6 (Power-Enable 4).
4. When writing 0×026F in stream mode, the descend mode should be used. There is no limit in single mode.

Layout

Layout Example



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN

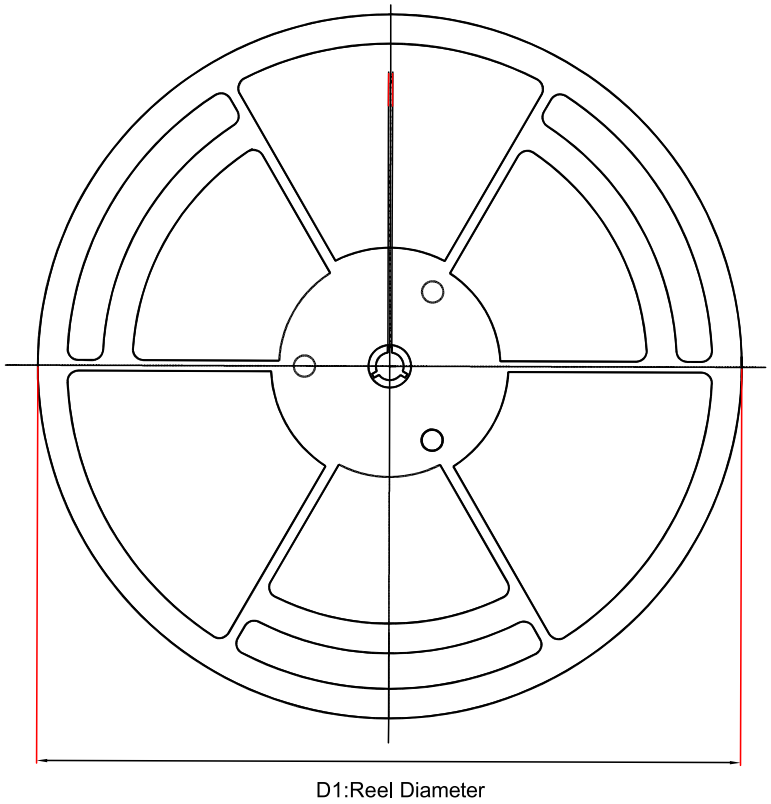


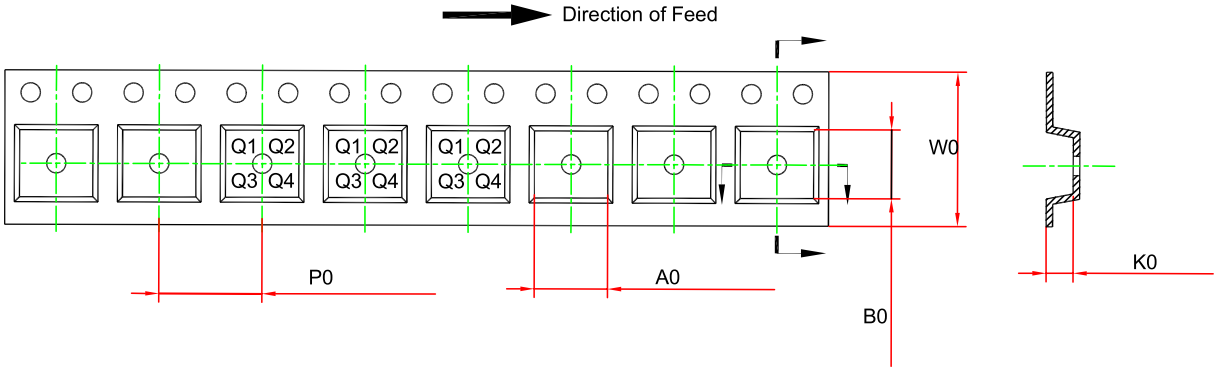
SOLDER MASK DETAILS

NOTES

1. Size of metal pad may vary due to creepage requirement.
2. Vias are optional depending on application. It is recommended that vias under paste be filled, plugged or tented.
3. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

Tape and Reel Information



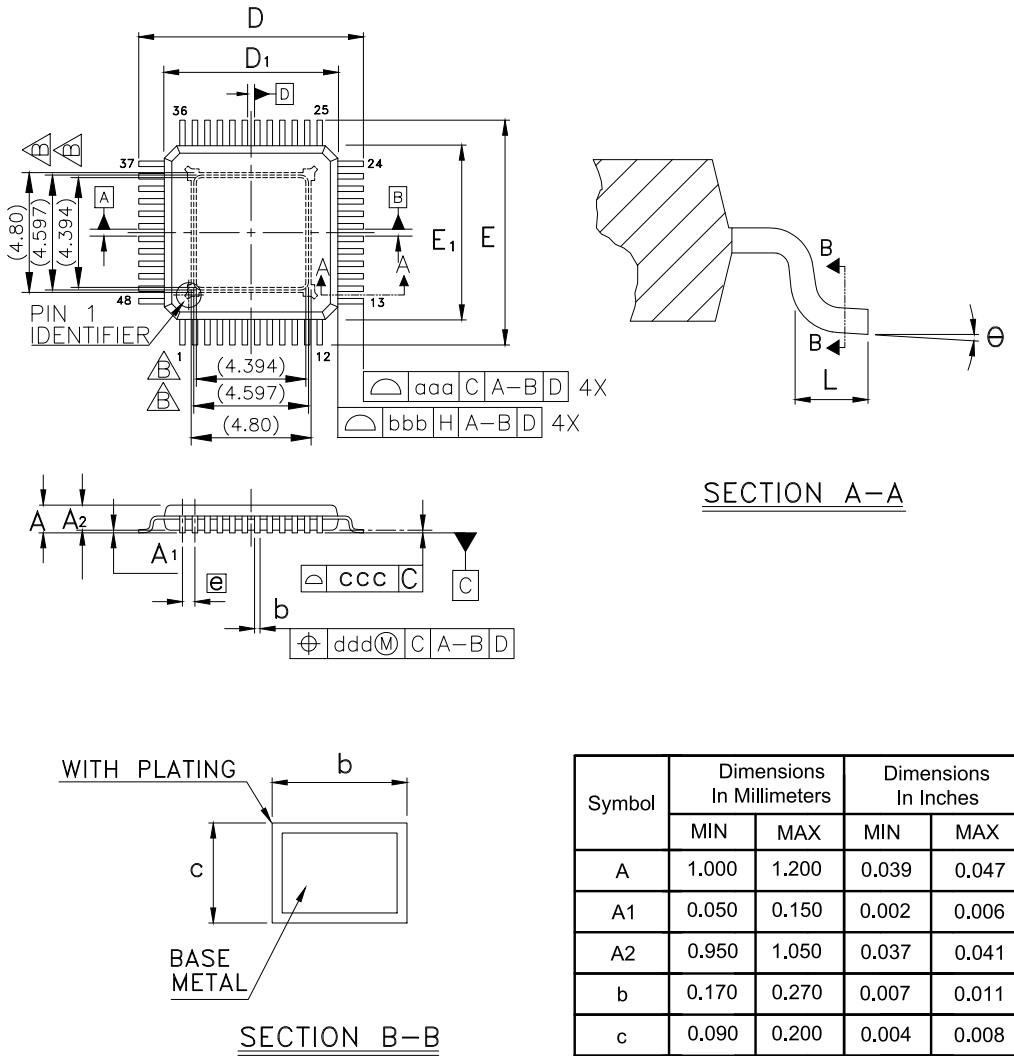


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPAFE0532-QPCR-S	TQFP7×7-EP48L	330	22	9.4	9.4	1.6	12	16	Q2

Package Outline Dimensions

TQFP7X7-48

Package Outline Dimensions QPC(TQFP7X7-48-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.000	1.200	0.039	0.047
A1	0.050	0.150	0.002	0.006
A2	0.950	1.050	0.037	0.041
b	0.170	0.270	0.007	0.011
c	0.090	0.200	0.004	0.008
D	9.000 BSC		0.354 BSC	
D1	7.000 BSC		0.276 BSC	
E	9.000 BSC		0.354 BSC	
E1	7.000 BSC		0.276 BSC	
e	0.500 BSC		0.020 BSC	
L	0.450	0.750	0.018	0.030
θ	0	7°	0	7°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPAFE0532-QPCR-S	−40 to 125°C	TQFP7X7-EP48L	0532	3	Tray, 2500	Green
TPAFE0532-QPCR-S	−40 to 125°C	TQFP7X7-EP48L	0532	3	Tape and Reel, 2000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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