Features

- ±200 kV/μs static CMTI, ±150 kV/μs dynamic CMTI
- 2 V input voltage range
- Fixed gain: 1
- Low offset error: 3mV maximum at 25°C
- Very low gain error: 0.5% maximum at 25°C
- Wide Temperature Range: −40°C to +125°C
- SOP8 package
- Safety-Related Certifications:
  - VDE Certification according to DIN VDE V 0884-17(IEC60747-17)
  - 3750V_{RMS} Isolation Rating per UL 1577
  - CQC Certification per GB 4943.1
  - CSA, TUV and CB certifications

Description

The TPA8023 is a precision, isolated amplifier with an output separated from the input circuitry by capacitive silicon dioxide insulation barrier. This barrier is certified to provide isolation of up to 3750V_{RMS} according to UL1577.

The common mode transient immunity (CMTI) of the TPA8023 has been significantly enhanced through innovative circuit design and optimized structure.

The input of the TPA8023 is high-impedance which can be connected to high-impedance resistive dividers or any other high-impedance voltage signal source. The excellent performance of the device supports bus voltage in motor control or other applications. The common-mode overvoltage and missing high-side supply voltage detection features of the TPA8023 simplify system-level diagnostics.

The device is available in SOP8 packages, and is characterized from −40°C to +125°C.

Applications

- Solar Inverter
- Motor Control
- Power Supplies

Typical Application Circuit

Table of Contents

Revision History

Date	Revision	Notes
2022-11-05	Rev.Pre.0	Pre releasing version
2022-12-16	Rev.Pre.1	Updated isolated rating.
2023-07-03	Rev.Pre.2	Updated Specification.
2023-08-18	Rev.Pre.3	Updated Specification. Updated quantity: 1000 to 4000.
2023-09-16	Rev.Pre.4	Updated V_{IORM}, V_{IOWM} and V_{IOTM}

Pin Configuration and Functions

TPA8023
8-Pin SOP Package
Top View

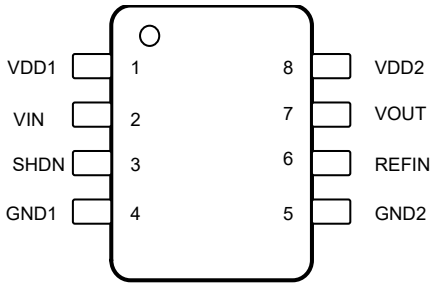


Table 6-1. Pin Functions: TPA8023

Pin		Name	I/O	Description
1		VDD1		High-side power supply
2		VIN	Input	Analog input
3		SHDN	Input	Shutdown input, active high, with internal pullup resistor. Connect to GND1 to enable the device.
4		GND1		High-side analog ground
5		GND2		Low-side analog ground
6		REF	Input	Reference voltage
7		VOUT	Output	Analog output, refer to the voltage at REF pin
8		VDD2		Low-side power supply

Specifications

Absolute Maximum Ratings(1)

Parameter		Min	Max	Unit
VDD	Supply voltage, VDD1 to GND1 or VDD2 to GND2	−0.3	7	V
	Analog input voltage at VIN	GND1 – 6	VDD1 + 0.5	V
	Analog input voltage at SHDN	GND1 – 0.5	VDD1 + 0.5	V
	Analog output voltage at VOUT, REFIN	GND1 – 0.5	VDD2 + 0.5	V
I_{IN}	Input current to any pin except supply pins	−10	10	mA
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Parameter	Condition	Value	Unit
HBM, per ANSI/ESDA/JEDEC JS-001/ANSI/ESD STM5.5.1(1)	All Pin	2	kV
CDM, per ANSI/ESDA/JEDEC JS-002(2)	All Pin	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
VDD1	High-side supply voltage (VDD1 to GND1)	4.5	5.0	5.5	V
VDD2	Low-side supply voltage (VDD2 to GND2)	3.0	3.3	5.5	V
T_A	Operating ambient temperature	−40	25	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOP8	158	43	°C/W

Insulation Specifications

Symbol	Parameter	Conditions	Value			Unit
				SOP8		
CLR	External clearance	Shortest terminal-to-terminal distance through air		> 4.0		mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface		> 4.0		mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)		> 22		μm
DTC	Distance through the Molding compound	Minimum internal distance across the conductors inside the package		0.45		mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A		> 600		V
	Material group	According to IEC 60664-1		I		
	Over-voltage category	For Rated Mains Voltage ≤ 150 V_{RMS}		I-IV		
		For Rated Mains Voltage ≤ 300 V_{RMS}		I-III		
		For Rated Mains Voltage ≤ 600 V_{RMS}		I-II		
		For Rated Mains Voltage ≤ 1000 V_{RMS}		I		
	Climatic category			40/125/21		
	Pollution degree			2		
DIN V VDE V 0884-17 (1)(2)						
V_{IORM}	Maximum repetitive isolation voltage	AC voltage		990		V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; TDDB Test		700		V_{RMS}
		DC voltage		990		V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)		5300		V_{PK}
V_{IOSM}	Maximum surge isolation voltage (3)	Test method per IEC 62368-1, 1.2/50 μs waveform, V_{TEST} = 1.3 × V_{IOSM} (qualification)		5980		V_{PK}
q_{pd}	Apparent charge	Method a, After Input/Output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s		≤ 5		pC
		Method a, After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s		≤ 5		
		Method b1; At routine test (100% production) and preconditioning (type test), V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1 s		≤ 5		

C_{IO}	Isolation capacitance	V_{IO} = 0.4 × sin (2πft), f = 1 MHz		~0.5		pF
R_{IO}	Isolation resistance	V_{IO} = 500 V, T A= 25°C		> 10^{12}		Ω
		V_{IO} = 500 V, 100°C ≤ T A≤ 125°C		> 10^{11}		Ω
		V_{IO} = 500 V at T S= 150°C		> 10^{9}		Ω
UL 1577						
V_{ISO}	Withstanding isolation voltage	V_{TEST} = V_{ISO} , t = 60 s(qualification); V_{TEST} = 1.2 × V_{ISO} , t = 1 s (100% production)		3750		V_{RMS}

(1) All pins on each side of the barrier tied together creating a two-terminal device.
(2) This coupler is suitable for safe electrical insulation only within the safety operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3)Testing must be carried out in oil.

Safety-Related Certifications

VDE	UL	TUV	CQC	CSA	CB
Certified according to DIN VDE V 0884-17	Certified according to UL 1577 and CSA Component Acceptance Notice 5A	Certified according to EN IEC 62368-1 and EN IEC 61010-1	Certified according to GB 4943.1	Certified CSA C22.2 No. 62368-1 and CAN/CSA-C22.2 No. 60601-1	Certified according to EN IEC 62368-1
Certificate No.	Report Reference	Registration No.	Certificate No.	Master contract:	Ref. Certif. No.

Safety Limiting Values (1)

Parameter	Conditions(1)	Min	Typ	Max	Unit
Safety input, output or supply current	$R_{\theta JA}$ = 158°C/W, VDD1 = VDD2 = 5.5 V, T_J = 150°C, T_A = 25°C, SOP8 Package			143	mA
Safety total power	$R_{\theta JA}$ = 158°C/W, T_J = 150°C, T_A = 25°C, SOP8 Package			791	mW
Maximum safety temperature				150	°C

(1) The assumed junction-to-air thermal resistance in the Thermal Information is that of a device installed on a high-K test board for leaded surface-mount packages.

Electrical Characteristics

Minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD1 = 4.5 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, VIN = 0.1 V to 2 V(unless otherwise noted); typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ANALOG INPUT						
VClipping	Input voltage before clipping output	IN to GND1		2.516		V
VFSR	Specified linear full-scale voltage	IN to GND1	0.1		2	V
VOS	Input offset voltage	In VFSR, T_A = 25°C	–3	0.4	3	mV
		In 0V to 0.1V, T_A = 25°C		10		mV
TCV_{OS}	Input offset drift	In VFSR		±2		μV/°C
CIND	Differential input capacitance			7		pF
RIN	Single-ended input resistance	VINN = GND1		1		GΩ
IIB	Input bias current	IN = GND1, T_A = 25℃	–15		15	nA
ANALOG OUTPUT						
	Nominal gain	VIN at VFSR		1		
E_G	Gain error	VDD1 = 5 V, VIN at VFSR, T_A = 25°C	–0.5	±0.05	0.5	%
TCE_G	Gain error drift	VDD1 = 5 V, VIN at VFSR	–50	±15	50	ppm/°C
	Nonlinearity	VDD1 = 5 V, VIN at VFSR	–0.02	±0.01	0.02	%
	Input voltage range of REFIN		0		VDD2 – 2.5	V
	Input Resistance of REFIN			145		kΩ
	Nonlinearity drift			1		ppm/°C
THD	Total harmonic distortion	f_{IN} = 10 kHz		–80		dB
	Output noise	VIN = GND1, BW = 100 kHz		300		μV_{RMS}
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz, BW = 10 kHz		80		dB
		f_{IN} = 10 kHz, BW = 100 kHz		70		dB
PSRR	Power-supply rejection ratio	vs VDD1, at dc		–65		dB
		vs VDD1, 100-mV and 10-kHz ripple		–65		dB
		vs VDD2, at dc		–85		dB
		vs VDD2, 100-mV and 10-kHz ripple		–70		dB
CMTI	Common-mode transient immunity	|GND1 – GND2| = 1 kV		150		kV/μs
VCMout	Common-mode output voltage			1.4		V
	Output short-circuit current			±15		mA
ROUT	Output resistance	on VOUTP or VOUTN		< 0.2		Ω
BW	Output bandwidth			310		kHz

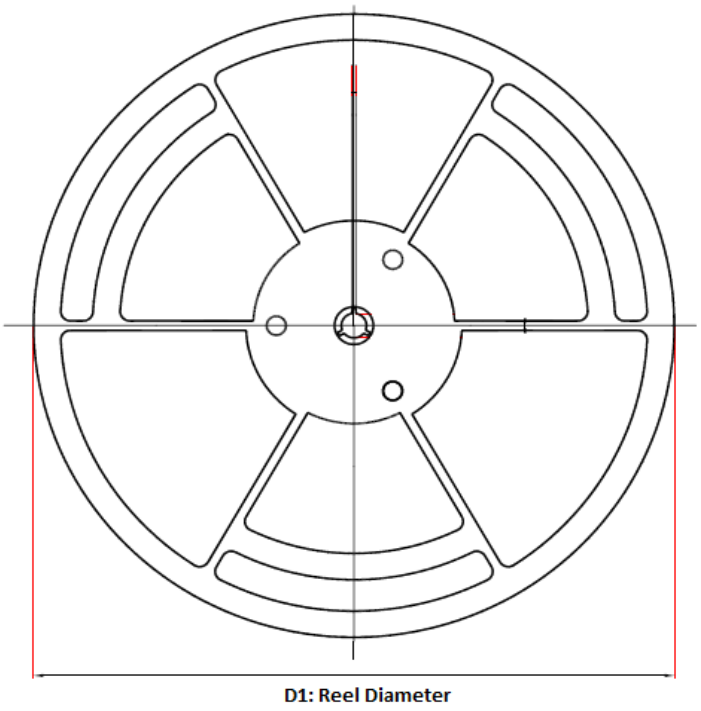
(1) Provided by bench test and design simulation

Electrical Characteristics

Minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD1 = 4.5 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, VIN = 0.1 V to 2 V(unless otherwise noted); typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DIGITAL INPUT						
	Input voltage	SHTDN to GND1	0		VDD1	V
I_{IN}	Input current	SHTDN pin, GND1 ≤ SHTDN ≤ VDD1	–70		1	μA
C_{IN}	Input capacitance	SHTDN pin		5		pF
V_{IH}	High-level input voltage	Shutdown	0.7 × VDD1			V
V_{IL}	Low-level input voltage	Enable			0.3 × VDD1	V
POWER SUPPLY						
	VDD1 undervoltage detection threshold	VDD1 falling		2		V
	VDD2 undervoltage detection threshold	VDD2 falling		2		V
I_{DD1}	High-side supply current	4.5 V ≤ VDD1 ≤ 5.5 V		15		mA
I_{DD2}	Low-side supply current	3.0 V ≤ VDD2 ≤ 3.6 V		8		mA
		4.5 V ≤ VDD2 ≤ 5.5 V		10		mA
SWITCHING CHARACTERISTICS						
t_r	Rise time	See Figure		1		μs
t_f	Fall time	See Figure		1		μs
	V_{IN} to V_{OUT} signal delay (50% – 10%)	See Figure, unfiltered output		0.7		μs
	V_{IN} to V_{OUT} signal delay (50% – 50%)	See Figure, unfiltered output		1.2		μs
	V_{IN} to V_{OUT} signal delay (50% – 90%)	See Figure, unfiltered output		1.8		μs
	Analog settling time	VDD1 step to 5.0 V with VDD2 ⩾ 3.0 V, to VOUTP, VOUTN valid, 0.1% settling				μs
	Enable time	Set SHDN high to low				μs
	Shutdown time	Set SHDN low to high				μs

Tape and Reel Information

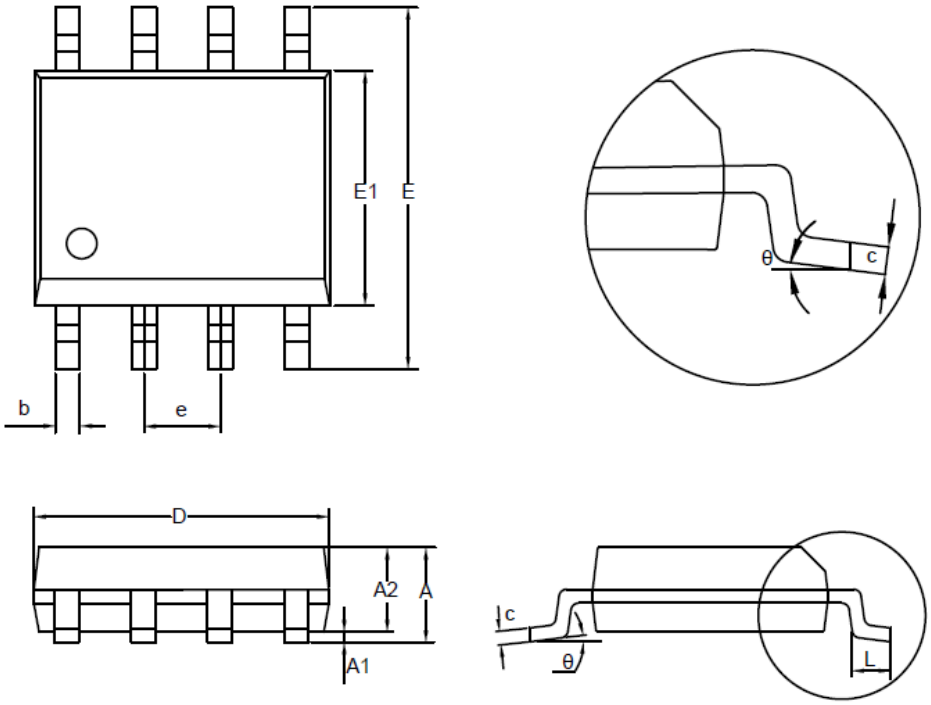


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPA8023-SO1R	SOP8	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1

Package Outline Dimensions

SOP8

Package Outline Dimensions SO1(SOP-8-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPA8023-SO1R	−40 to 125°C	SOP8	A8023	MSL3	Tape and Reel, 4000	Green

(1) Can provide sample in 2 months.

(2) Future product, contact 3PEAK factory for more information and sample.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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