1 Features

- 16 Monotonic 12-Bit DACs
  - Selectable Ranges: –10 to 0 V, –5 to 0 V, 0 to5 V, and 0 to 10 V
  - High Current Drive Capability: up to ±10 mA
  - Auto-Range Detector
  - Selectable Clamp Voltage
- 12-Bit SAR ADC
  - 21 External Analog Inputs(16 bi-polar inputs with -12.5 to 12.5V range; 5 high precision inputs with 0 to 5V range)
  - Programmable Out-of-Range Alarms
- Eight General Purpose I/O Ports (GPIOs)
- Internal 2.5 V Reference
- Internal Temperature Sensor
  - –40°C to 125°C Operation
  - ±7.5°C Accuracy
- Low-Power SPI-Compatible Serial Interface
  - 4-Wire Mode, 1.8 to 5.5 V Operation
- Operating Temperature: –40°C to 125°C
- Available in 64-Pin TQFP package

2 Applications

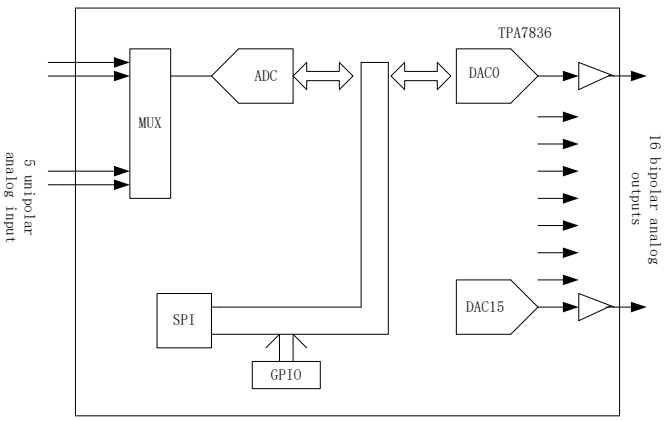
- Wireless infrastructure
  - Cellular Base Stations
  - Microwave Backhaul
- Optical networks
- General Purpose Monitor and Control
- Data Acquisition Systems

3 Description

The TPA7836B is a highly integrated, low power consumption, analog monitor and control solution, it includes a 21-channel, 12bits ADC, sixteen 12-bits DACs with programmable output ranges, an internal reference, eight GPIOs and a local temperature sensor, the high integration significantly reduces component counts and simplifies the system design with small pace, low power, high reliability.

The low power, very high integration and wide operation temperature range of this device make it suitable for an all-in-one, low cost, bias-control circuit for the power amplifiers found in multi-channel RF communication systems, the flexible DAC output ranges allow the device to be used as a biasing solution for the large variety of transistor technologies, such as LDMOS, GaN, GaAs.

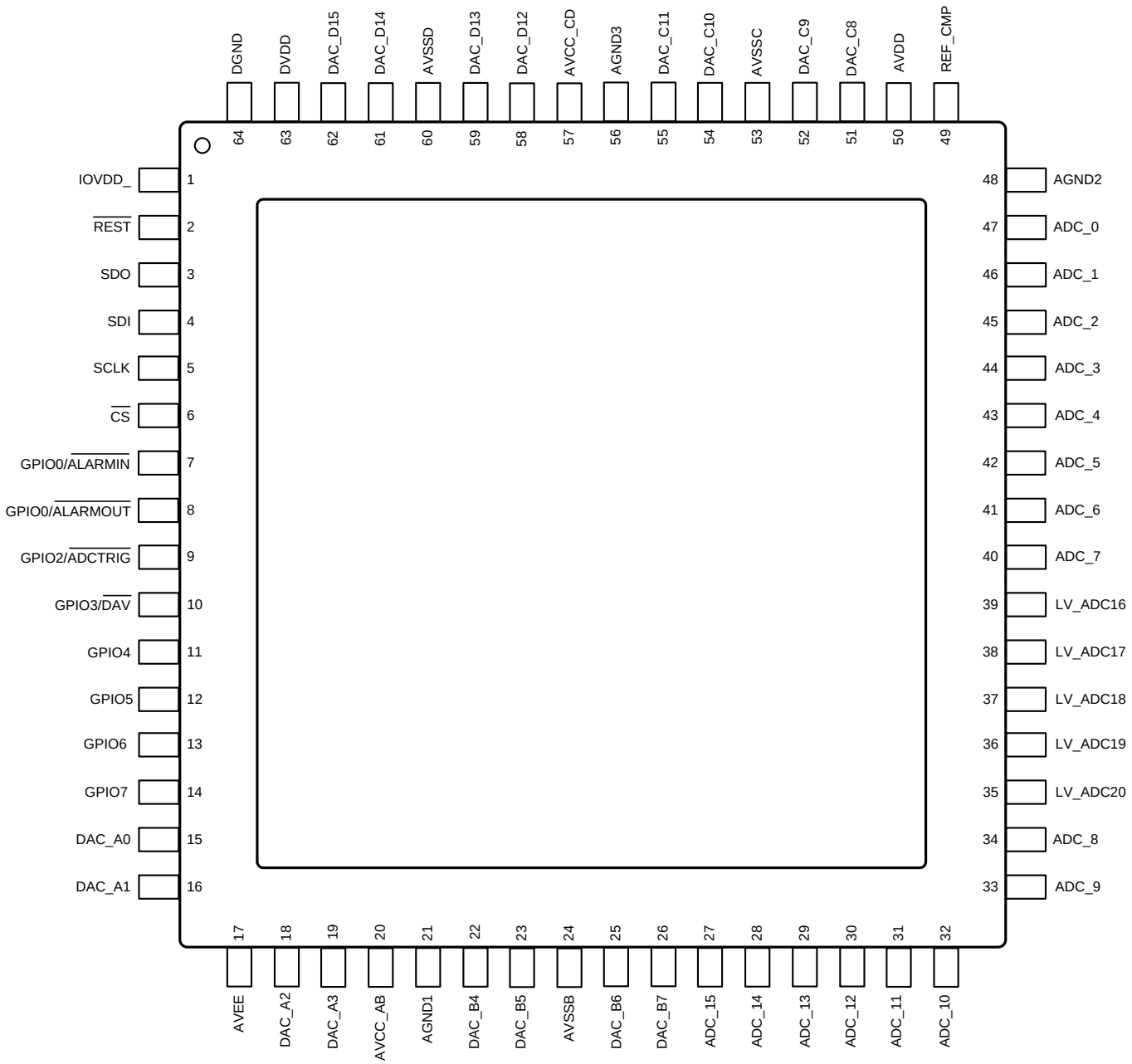
4 Function block diagram



Order Information

Order Number	Operating Temperature Range	Package	Marking Information	Transport Media, Quantity
TPA7836B-QP	-40 to 125°C	TQFP EP 64	TPA7836	Tape reel, MPQ 1000

5 Pin Configuration and Functions



Pin functions

Pin			Description
Pin Name	No	1/o	
ADC_0	47	I	Bipolar analog inputs. These pins are typically used to monitor the DAC group-C outputs. input range of these channels is –12.5 to 12.5 V.
ADC_1	46		
ADC_2	45		
ADC_3	44		
ADC_4	43		Bipolar analog inputs. These pins are typically used to monitor the DAC group-D outputs. input range of these channels is –12.5 to 12.5 V.
ADC_5	42		
ADC_6	41		
ADC_7	40		
ADC_8	34		Bipolar analog inputs. These pins are typically used to monitor the DAC group-B outputs. input range of these channels is –12.5 to 12.5 V.
ADC_9	33		
ADC_10	32		
ADC_11	31		
ADC_12	30		Bipolar analog inputs. These pins are typically used to monitor the DAC group-A outputs. input range of these channels is –12.5 to 12.5 V.
ADC_13	29		
ADC_14	28		
ADC_15	27		
AGND1	21	I	Analog ground, these pins are the ground reference point for all analog circuit on the device, connect the AGND1,AGND2 and AGND3 pins to the same potential(AGND), ideally, the analog and digital grounds should be at the same potential ground and must not differ by more than +/-0.3V
AGND2	48		
AGND3	56		
AVCC_AB	20	I	Positive analog power for DAC groups A and B, the AVCC_AB and must be connected to the same potential (AVCC)
AVCC_CD	57	I	Positive analog power for DAC groups C and D, the AVCC_AB and must be connected to the same potential (AVCC)
AVDD	50	I	Analog supply voltage (4.5 V to 5.5 V). This pin must have the same value as the DVDD pin.
AVEE	17	I	Lowest potential in the system. This Pin is typically tied to the negative supply voltage but if all DACs are set in the positive output range, this pin can be connected to the same analog ground. This pin also acts as the negative analog supply for DAC group A. This pins sets the power-on-reset and clamp voltage values for the DAC group A
AVSSB	24	I	Negative analog supply for DAC group B, This pin sets the power-on-reset and clamp voltage values for the DAC group B, this pin is typically tied to the AVEE pin for the negative output range or AGND for the positive output range
AVSSC	53	I	Negative analog supply for DAC group C, This pin sets the power-on-reset and clamp voltage values for the DAC group B, this pin is typically tied to the AVEE pin for the negative output range or AGND for the positive output range
AVSSD	60	I	Negative analog supply for DAC group D, This pin sets the power-on-reset and clamp voltage values for the DAC group B, this pin is typically tied to the AVEE pin for the negative output range or AGND for the positive output range
$\overline{CS}$	6	I	Active-low serial-data enable. This input is the frame-synchronization signal for the serial data, When this signal goes low, it enables the serial interface input shift register

DAC_A0	15	O	DAC group A, These DAC channels share the same range and clamp voltage. If any of the other DAC groups is in the negative voltage range, DAC group A should be in the negative voltage range as well
DAC_A1	16		
DAC_A2	18		
DAC_A3	19		
DAC_B4	22	O	DAC group B, These DAC channels share the same range and clamp voltage. If any of the other DAC groups is in the negative voltage range, DAC group B should be in the negative voltage range as well
DAC_B5	23		
DAC_B6	25		
DAC_B7	26		
DAC_C8	51	O	DAC group C, These DAC channels share the same range and clamp voltage. If any of the other DAC groups is in the negative voltage range, DAC group C should be in the negative voltage range as well
DAC_C9	52		
DAC_C10	54		
DAC_C11	55		
DAC_D12	58	O	DAC group D, These DAC channels share the same range and clamp voltage. If any of the other DAC groups is in the negative voltage range, DAC group D should be in the negative voltage range as well
DAC_D13	59		
DAC_D14	61		
DAC_D15	62		
DGND	64	I	Digital ground. This pin is the ground reference point for all digital circuitry on the device. Ideally, the analog and digital grounds should be at the same potential (GND) and must not differ by more than +/-0.3V.
DVDD	63	I	Digital supply voltage (4.5 V to 5.5 V). This pin must have the same value as the AVDD pin.
GPIO0/ $\overline{\text{ALARMIN}}$	7	I/O	General-purpose digital I/O 0(default), this pin is a bidirectional digital input/output with an internal 48-KΩ pullup resistor to the IOVDD pin. Alternatively the pin can be set to operate as the digital input ALARMIN which is an active-low alarm-control signal. If unused this pin can be left floating
GPIO1/ $\overline{\text{ALARMOUT}}$	8	I/O	General purpose digital I/O 1(default),this pin is bidirectional digital I/O with an internal 48-KΩ pullup resistor to the IOVDD pin, alternatively the pin can be set to operate as ALARMOUT which is an open drain global alarm output, this pin goes low(active) when an alarm event is detected. If unused this pin can be left floating.
GPIO2/ $\overline{\text{ADCTRIG}}$	9	I/O	General purpose digital I/O 2(default),this pin is bidirectional digital I/O with an internal 48-KΩ pullup resistor to the IOVDD pin, alternatively the pin can be set to operate as ADCTRIG which is an active-low external conversion trigger. The falling edge of this pin begins the sampling and conversion of the ADC, if unused this pin can be left floating
GPIO3/ $\overline{\text{DAV}}$	10	I/O	General purpose digital I/O 3(default), this pin is bidirectional digital I/O with an internal 48-KΩ pullup resistor to the IOVDD pin, alternatively the pin can be set to operate as DAV pin goes low (active) when the conversion ends, in the auto mode, a 1-uS pulse (active low) appears on this pin when a conversion cycle finishes, the DAV pin remains high when deactivated. If unused this pin can be left floating.
GIPO4	11	I/O	General purpose digital I/O. These pins are bidirectional digital I/Os with an internal 48-KΩ, pullup resistor to the IOVDD pin. If unused these pins can be left floating
GPIO5	12		
GPIO6	13		
GPIO7	14		
IOVDD	1	I	I/O supply voltage (1.8 V to 5.5 V). This pin sets the I/O operating voltage and threshold levels The voltage on this pin must not be greater than the value of the DVDD pin

LV_ADC16	39	I	General purpose analog inputs. These channels are used for general monitoring. The input range of these pins is 0 to 2 × Vref.
LV_ADC17	38		
LV_ADC18	37		
LV_ADC19	36		
LV_ADC20	35		
REF_CMP	49	O	Internal-reference compensation-capacitor connection. Connect a 4.7-μF capacitor between this pin and the AGND2 pin.
$\overline{\text{RESET}}$	2	I	Active-low reset input.
SCLK	5	I	Serial interface clock.
SDI	4	I	Serial-interface data input. Data is clocked into the input shift register on each rising edge other SCLK pin.
SDO	3	O	Serial-interface data output. The SDO pin is in high impedance when the CS pin is high. Data is clocked out of the input shift register on each falling edge of the SCLK pin.
Thermal Pad	---	I	The thermal pad is located on the bottom-side of the device package. The thermal pad should be tied to the same potential as the AVEE pin or left disconnected.

6 Specifications

6.1 Absolute Maximum Ratings

Items	Description	Value	Unit
Supply voltage	AV_{DD} to GND	−0.3 to 6	V
	DV_{DD} to GND	−0.3 to 6	
	IOV_{DD} to GND	−0.3 to 6	
	AV_{CC} to GND	−0.3 to 18	
	AV_{EE} to GND	−13 to 0.3	
	AV_{SSB},AV_{SSC},AV_{SSD} to AV_{EE}	−0.3 to 13	
	AV_{CC} to AV_{SSB}, AV_{SSC}, or AV_{SSD}	−0.3 to 26	
	AV_{CC} to AV_{EE}	-0.3 to 26	
	DGND to AGND	-0.3 to 0.3	
Pin Voltage	ADC_(0-15)analog voltage to GND	AV_{EE}-0.3 to 13	V
	LV_ADC(16-20) analog input voltage to GND	-0.3 to AV_{DD}+0.3	
	DAC_A[0-3] outputs to GND	AV_{EE}-0.3 to AV_{CC}+0.3	
	DAC_B[4-7] outputs to GND	AVSSB–0.3 to AVCC+0.3	
	DAC_C[8-11] outputs to GND	AVSSC–0.3 to AVCC+0.3	
	DAC_D[12-15] outputs to GND	AVSSD–0.3 to AVCC+0.3	
	REF_CMP to GND	–0.3 to AVDD+0.3	
	$\overline{\text{CS}}$, SCLK, SDI and $\overline{\text{RESET}}$ to GND	–0.3 to IOVDD+0.3	
	SDO to GND	–0.3 to IOVDD+0.3	
	GPIO[0-7] to GND	–0.3 to IOVDD+0.3	
	ADC_[0:15] analog input current	-10 to 10	

Pin current	LV_ADC[16:20] analog input current	-10 to 10	mA
	GPIO[0:7] sinking current	5	
Operating temperature		-40 to 125	^{0}C
Junction temperature($T_J$max)		–40 to 150	^{0}C
Storage temperature(Tstg)		-40 to 150	^{0}C

*** Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(1) The input and output voltage ratings may be exceeded if the input and output diode current ratings are observed.

6.2 ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	±2500	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	±1000	V

6.3 RECOMMENDED OPERATING CONDITIONS

Items	Parameter	Minimum	Normal	Maximum	Unit
Power supply	AV_{DD}	4.5	5	5.5	V
	DVDD(1)	4.5	5	5.5	
	IOVDD(2)	1.8	3.3	5.5	
	AVCC	4.5	12	12.5	
	AVEE	-12.5	-12	0	
	AVSSB, AVSSC, AVSSD	AVEE		0	
Specified operating temperature		-40	25	105	^{0}C
Operating temperature		-40	25	125	^{0}C

*(1): The value of the DV_{DD} pin must be equal to that of the AV_{DD} pin.

*(2): The value of the IOV_{DD} pin must be less than or equal to that of the DV_{DD} pin.

6.4 Thermal information

Symbol	Parameter	PAP (HTQFP) 64Pins	Unit
RθJA	Junction-to-ambient thermal resistance	26.2	°C/W
RθJC(top)	Junction-to-case (top) thermal resistance	7.2	

RθJB	Junction-to-board thermal resistance	9.1	
Ψ_{JT}	Junction-to-top characterization parameter	0.2	
Ψ_{JB}	Junction-to-board characterization parameter	9	
RθJC(bot)	Junction-to-case (bottom) thermal resistance	0.2	

6.5 Electrical Characteristics-DAC specification

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These Specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of The product containing it. AV_{DD} = DV_{DD} = 4.5 to 5.5 V, AV_{CC} = 12 V, IOV_{DD} = 1.8 to 5.5 V, AGND = DGND = 0 V, AV_{EE} = AV_{SSB} = AV_{SSC} = AV_{SSD} = –12 V (for DAC groups in negative range) or 0 V (for DAC groups in positive ranges), DAC output Range = 0 to 10 V for all groups, no load on the DACs, TA = –40°C to 105°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution		12			bits
INL (Relative accuracy)	Measured by line passing through codes 020h and FFFh. 0 to 10 V and –10 to 0 V ranges		±0.3	±2	LSB
	Measured by line passing through codes 040h and FFFh. 0 to 5 V and –5 to 0 V ranges		±0.5	±2	
DNL (Differential nonlinearity)	Specified monotonic. Measured by line passing through codes 020h and FFFh. 0 to 10 V and –10 to 0V range		±0.03	±1	LSB
	Specified monotonic. Measured by line passing through codes 020h and FFFh. 0 to 5 V and –5 to 0V range		±0.06	±1	
TUE (Total unadjusted error(1))	TA = 25°C, 0 to 10 V range		±2.5	±30	mV
	TA = 25°C, –10 to 0 V range		±2.5	±30	
	TA = 25°C, 0 to 5 V range		±1.5	±15	
	TA = 25°C, –5 to 0 V range		±1.5	±15	
Offset error	TA = 25°C, Measured by line passing through codes 020h and FFFh. 0 to 10 V range		±0.25	±5	mV
	TA = 25°C, Measured by line passing through codes 040h and FFFh. 0 to 5 V range		±0.25	±5	
Zero-code error*	TA = 25°C, Code 000h, –10 to 0 V range		±1	±25	mV
	TA = 25°C, Code 000h, –5 to 0 V range		±1	±25	
Gain error*	TA = 25°C, Measured by line passing through codes 020h and FFFh, 0 to 10 V range		±0.01	±0.2	%FSR
	TA = 25°C, Measured by line passing through codes 020h and FFFh, -10V to 0 V range		±0.01	±0.2	
	TA = 25°C, Measured by line passing through codes 040h and FFFh, 0 to 5V range		±0.01	±0.2	
	TA = 25°C, Measured by line passing through codes 040h and FFFh, -5 to 0V range		±0.01	±0.2	
Offset temperature coefficient	0 to 10 V range		±2		ppm/°C
	0 to 5 V range		±2		
Zero-code temperature coefficient	–10 to 0 V range		±2		ppm/°C
	–5 to 0 V range		±2		
Gain temperature coefficient(1)	0 to 10 V range		±2		ppm/°C
	–10 to 0 V range		±2		
	0 to 5 V range		±2		
	–5 to 0 V range		±2		

*: the internal reference contribution is not included

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC OUTPUT CHARACTERISTICS					
Full-scale output voltage range	Set at power-up or reset through auto-range detection. The output range can be modified after power-up or reset through the DAC range registers (Address 0x1E through 0x1F). DAC-RANGE = 100b	-10		0	V
	The output range can be modified after power-up or reset through the DAC range registers (address 0x1E Through 0x1F). DAC-RANGE = 101b	-5		0	
	Set at power-up or reset through auto-range detection. The output range can be modified after power-up or reset through the DAC range registers (Address 0x1E through 0x1F). DAC-RANGE = 111b	0		5	
	The output range can be modified after power-up or reset through the DAC range registers (address 0x1E through 0x1F). DAC-RANGE = 110b	0		10	
Output voltage settling time	Transition: Code 400h to C00h to within ½ LSB, RL =2 kΩ, CL = 200 pF. 0 to 10 V and –10 to 0 V ranges		10		μs
	Transition: Code 400h to C00h to within ½ LSB, RL =2 kΩ, CL = 200 pF. 0 to 5 V and –5 to 0 V ranges		10		
Output noise	TA = 25°C, 1 kHz, code 800h, includes internal reference noise		1.2		μV/√Hz
	TA = 25°C, integrated noise from 0.1 Hz to 10 Hz code 800h, includes internal reference noise		64		μVrms
Slew rate	Transition: Code 400h to C00h, 10% to 90%, RL = 2kΩ, CL = 200 pF. 0 to 10 V and –10 to 0 V ranges		1.25		V/μs
	Transition: Code 400h to C00h, 10% to 90%, RL = 2kΩ, CL = 200 pF. 0 to 5 V and –5 to 0 V ranges		1.25		
Glitch energy	Transition: Code 7FFh to 800h; 800h to 7FFh		1		nV-s
Power-on overshoot	AVEE = AVSSB = AVSSC = AVSSD = AGND, AVCC = 0t o 12 V, 2-ms ramp		10		mV
DC output impedance	Code set to 800h, ±15mA		1		Ω
Maximum capacitive load	RL = ∞	0		10	nF
Load current	Source or sink with 1-V headroom from the DAC group AVCC or AVSS voltage, voltage drop < 25 mV	±15			mA
	Source or sink with 300-mV headroom from the DAC group AVCC or AVSS voltage, voltage drop < 25 mV	±10			
Short circuit current	Full-scale current shorted to the DAC group AVSS or AVCC voltage		±45		mA
CLAMP OUTPUTS					
Clamp output voltage	DAC output range: 0 to 10 V, AVSS = AGND		0		V
	DAC output range: 0 to 5 V, AVSS = AGND		0		
	DAC output range: –10 to 0 V, AVSS = –12 V		AVSS + 2		

	DAC output range: –5 to 0 V, AVSS = –6 V		AVSS + 1		
Clamp output impedance			8		kΩ

6.6 Electrical Characteristics-ADC&TEMP sensor specification

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These Specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of The product containing it. AV_{DD} = DV_{DD} = 4.5 to 5.5 V, AV_{CC} = 12 V, IOV_{DD} = 1.8 to 5.5 V, AGND = DGND = 0 V, AV_{EE} = AV_{SSB} = AV_{SSC} = AV_{SSD} = –12 V (for DAC groups in negative range) or 0 V (for DAC groups in positive ranges), DAC output Range = 0 to 10 V for all groups, no load on the DACs, TA = –40°C to 105°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution		12			bits
INL	Unipolar input channels		±0.5	±2	LSB
	Bipolar input channels		±0.5	±2	
DNL	Specified monotonic. All input channels	-1	±0.5	1.5	LSB
UNIPOLAR ANALOG INPUTS: LV_ADC16 to LV_ADC20					
Absolute input voltage range		AGND – 0.2		AVDD + 0.2	V
Full scale input range	Vref measured at REF_CMP pin	0		2 × Vref	V
Update time	Single unipolar input, temperature sensor disabled		9.2		µs
Gain error*			±0.5	±10	LSB
Gain error match			±1		LSB
Offset error			±1	±5	LSB
Offset error match			±0.5		LSB
DC input leakage current	Unselected ADC input			±10	µA
Input capacitance			20		pF
BIPOLAR ANALOG INPUTS: ADC_0 to ADC_15					
Absolute input voltage range		-13		+13	V
Full scale input range		-12.5		+12.5	V
Update time	Single bipolar input, temperature sensor disabled		28.4		µs
Gain error*			±0.5	±20	LSB
Offset error			±0.25	±15	LSB
Input resistance			170		kΩ
ADC UPDATE TIME					
ADC update time	All 21 ADC inputs enabled, temperature sensor disabled		500.4		µs
	All 21 ADC inputs enabled, temperature sensor enabled		528.8		µs
Internal oscillator frequency			5		MHz
INTERNAL REFERENCE (INTERNAL REFERENCE NOT ACCESSIBLE)					
Initial accuracy	TA = 25°C	2.4925	2.5	2.5075	
Reference temperature coefficient			20		ppm/°C

TEMPERATURE SENSOR					
Resolution	LSB size		0.25		°C
Accuracy	TA = –40°C to 125°C, AVDD = 5 V		±2.5		°C
Update time	All ADC input channels are disabled		32		ms
Operating range		-40		+125	°C

*: the internal reference contribution is not included

6.7 Timing Requirements

AVDD = DVDD = 4.5 to 5.5 V, AVCC = 12 V, AVEE = –12 V, AGND = DGND = AVSSB = AVSSC = AVSSD = 0 V, DAC output range= 0 to 10 V for all groups, no load on the DACs, TA = –40°C to 105°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL LOGIC					
Reset delay; delay-to-normal operation from reset		100		500	µs
Reset pulse width		20			ns
Convert pulse width		20			ns
Clamp shutdown delay			100		µs
Power-down recovery time				70	µs
ADC WAIT state(5); the wait time from when the ADC enters the IDLE state, to when the ADC is ready for trigger		2			µs
SERIAL INTERFACE					
f(SCLK) SCLK frequency	IOVDD = 1.8 to 2.7 V			15	MHz
	IOVDD = 2.7 to 5.5 V			20	
t_p SCLK period	IOVDD = 1.8 to 2.7 V	66.7			Ns
	IOVDD = 2.7 to 5.5 V	50			
tPL SCLK pulse width low	IOVDD = 1.8 to 2.7 V	30			Ns
	IOVDD = 2.7 to 5.5 V	23			
tPH SCLK pulse width high	IOVDD = 1.8 to 2.7 V	30			Ns
	IOVDD = 2.7 to 5.5 V	23			
th SDI hold	IOVDD = 1.8 to 2.7 V	10			Ns
	IOVDD = 2.7 to 5.5 V	10			
tsu SDI setup	IOVDD = 1.8 to 2.7 V	10			Ns
	IOVDD = 2.7 to 5.5 V	10			
th($\overline{CS}$) $\overline{CS}$ hold	IOVDD = 1.8 to 2.7 V	20			Ns
	IOVDD = 2.7 to 5.5 V	20			
tsu($\overline{CS}$) $\overline{CS}$ setup	IOVDD = 1.8 to 2.7 V	5			Ns
	IOVDD = 2.7 to 5.5 V	5			

t(ODZ)	IOVDD = 1.8 to 2.7 V	0		15	Ns
SDO driven to tri-state	IOVDD = 2.7 to 5.5 V	0		9	
t(OZD)	IOVDD = 1.8 to 2.7 V	0		23	Ns
SDO tri-state to driven	IOVDD = 2.7 to 5.5 V	0		15	
t(OD)	IOVDD = 1.8 to 2.7 V	0		23	Ns
SDO output delay	IOVDD = 2.7 to 5.5 V	0		15	
t(IAG)	IOVDD = 1.8 to 2.7 V	17			ns
Inter-access gap	IOVDD = 2.7 to 5.5 V	17			

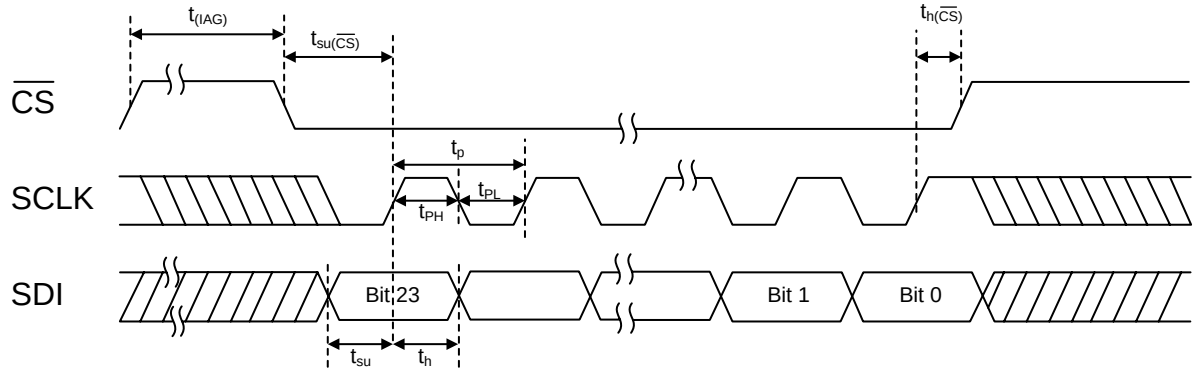


Figure 1. Serial Inerface Write Timing Diagram

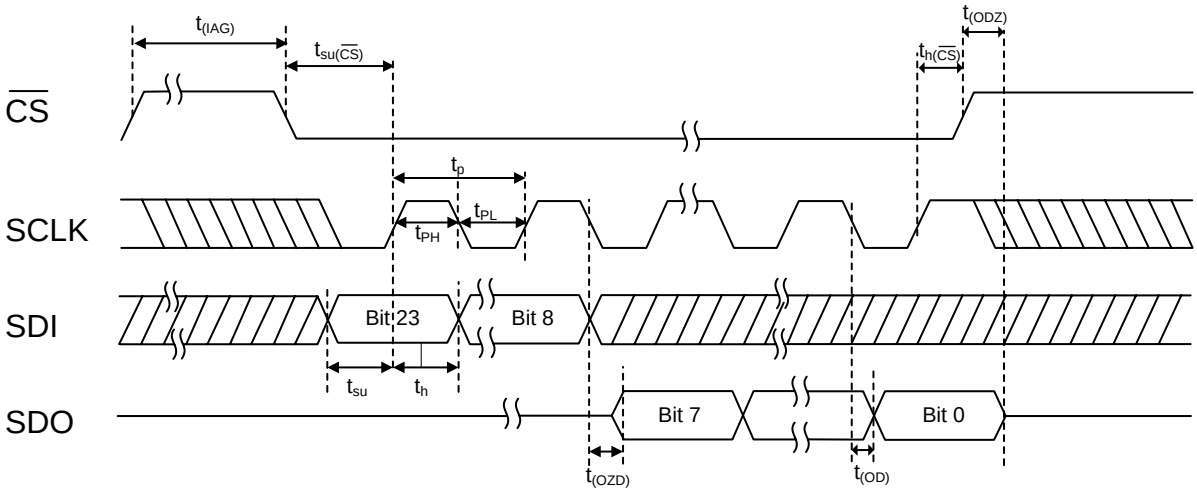


Figure 2. Serial Inerface Read Timing Diagram

6.8 Electrical Characteristics — General Specifications

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These Specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of The product containing it. AV_{DD} = DV_{DD} = 4.5 to 5.5 V, AV_{CC} = 12 V, IOV_{VDD} = 1.8 to 5.5 V, AGND = DGND = 0 V, AV_{EE} = AV_{SSB} = AV_{SSC} = AV_{SSD} = –12 V (for DAC groups in negative range) or 0 V (for DAC groups in positive ranges), DAC output Range = 0 to 10 V for all groups, no load on the DACs, TA = –40°C to 105°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER REQUIREMENTS					
I_{AVDD} AV_{DD} supply current	No DAC load, all DACs at 800h code and ADC at the fastest auto conversion rate		12.8	16.2	mA
I_{AVCC} AV_{CC} supply current			4	8	
I_{AVSS} AV_{SS} supply current		-7.4	-6.7		
I_{AVEE} AV_{EE} supply current		-2.5	-2.3		
I_{DVDD} DV_{DD} supply current			0.2	1	
I_{IOVDD} IOV_{DD} supply current			1.5	15	μA
Power consumption			287		mW
I_{AVDD} AV_{DD} supply current	Power down mode		2.9	3.7	mA
I_{AVCC} AV_{CC} supply current			1.2	1.5	
I_{AVSS} AV_{SS} supply current		-4.3	-3.6		
I_{AVEE} AV_{EE} supply current		-2	-1.2		
I_{DVDD} DV_{DD} supply current			0.1	1	
I_{IOVDD} IOV_{DD} supply current			1	5	uA
Power consumption			87		mW
AV_{SS} DETECTOR					
AVSS threshold detector (AVSSTH)		-3.5		-1.5	V
DIGITAL LOGIC: ALL EXCEPT GPIO					
High-level input voltage	IOV_{DD} = 1.8 to 5.5 V	0.7 × IOV_{DD}			V
Low-level input voltage	IOV_{DD} = 1.8 V			0.45	V
	IOV_{DD} = 2.7 to 5.5 V			0.3 × IOV_{DD}	V
High-level output voltage	IOV_{DD} = 2.7 to 5.5 V	IOV_{DD} – 0.4			V
Low-level output voltage	$I_{(LOAD)}$ = –1 mA			0.4	V
High impedance leakage				±5	μA
High impedance output capacitance			10		pF
DIGITAL LOGIC: GPIO					
High-level input voltage	IOV_{DD} = 1.8 to 5.5 V	0.7 × IOV_{DD}			V
Low-level input voltage	IOV_{DD} = 1.8 V			0.45	V
	IOV_{DD} = 2.7 to 5.5 V			0.3 × IOV_{DD}	
Low-level output voltage	IOV_{DD} = 1.8 V, $I_{(LOAD)}$ = –1 mA			0.4	V
	IOV_{DD} = 5.5 V, $I_{(LOAD)}$ = –2 mA			0.4	
Input impedance	To IOV_{DD}		48		kΩ

6.9 Typical Characteristics

At TA = 25°C (unless otherwise noted)

Blue >>AVCC, Yellow >>VDD, Red >>AVSS, Green >>DAC OUTPUT

AV_{SS} = AV_{EE} = –12 V, AV_{CC} = 0 to 12 V

Figure 13. DAC Power On Overshoot, Dual Supply

Blue>>AVCC, Green>>DAC OUTPUT

AV_{SS} = AV_{EE} = AGND, AV_{CC} = 0 to 12 V

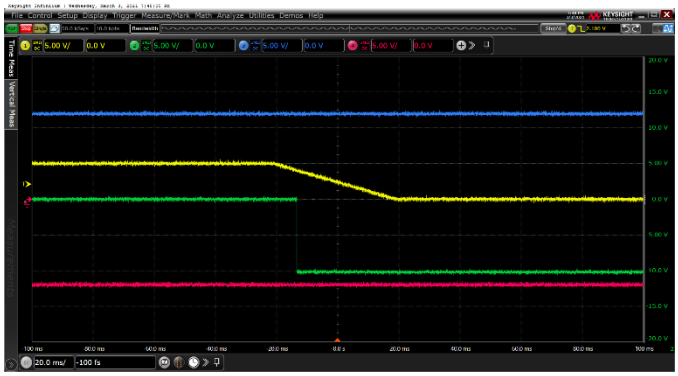
Figure 12. DAC Power On Overshoot, Single Supply

Code 0xFFF, DAC range: –10 to 0 V, no load

Figure 15. DAC Clamp Recovery Large Signal

Code 0xFFF, DAC range: –10 to 0 V, no load

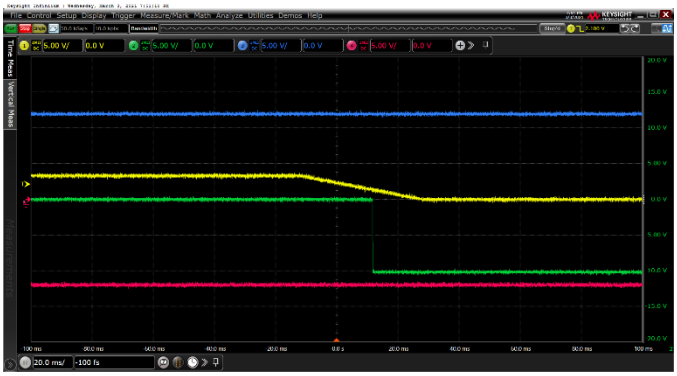
Figure 16. DAC Clamp Recovery Small signal



Blue >>AVCC, Yellow >>AVDD&DVDD, Red >>AVSS, Green >>DAC OUTPUT

Code 0xFFF, DAC range: –10 to 0 V, no load

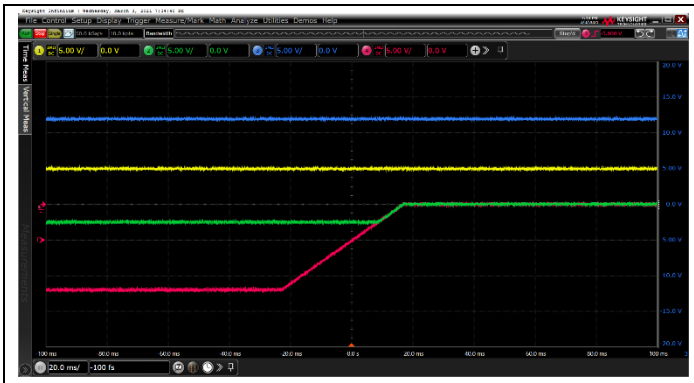
Figure 17. DAC Output With AV_{DD} and DV_{DD} Supply Collapse



Blue >>AVCC, Yellow >>IOVDD, Red >>AVSS, Green >>DAC OUTPUT

Code 0xFFF, DAC range: –10 to 0 V, no load

Figure 18. DAC Output With IOV_{DD} Supply Collapse



Blue >>AVCC, Yellow >>VDD, Red >>AVSS, Green >>DAC OUTPUT

Code 0xC00, DAC range: –10 to 0 V, no load

Figure 19. DAC Output With AVss Supply Collapse

Blue >>AVCC, Yellow >>VDD, Red >>AVSS, Green >>DAC OUTPUT

Code 0xFFF, DAC range: –10 to 0 V, no load

Figure 20. DAC Output With AVcc Supply Collapse

7 Detail description

7.1 Overview

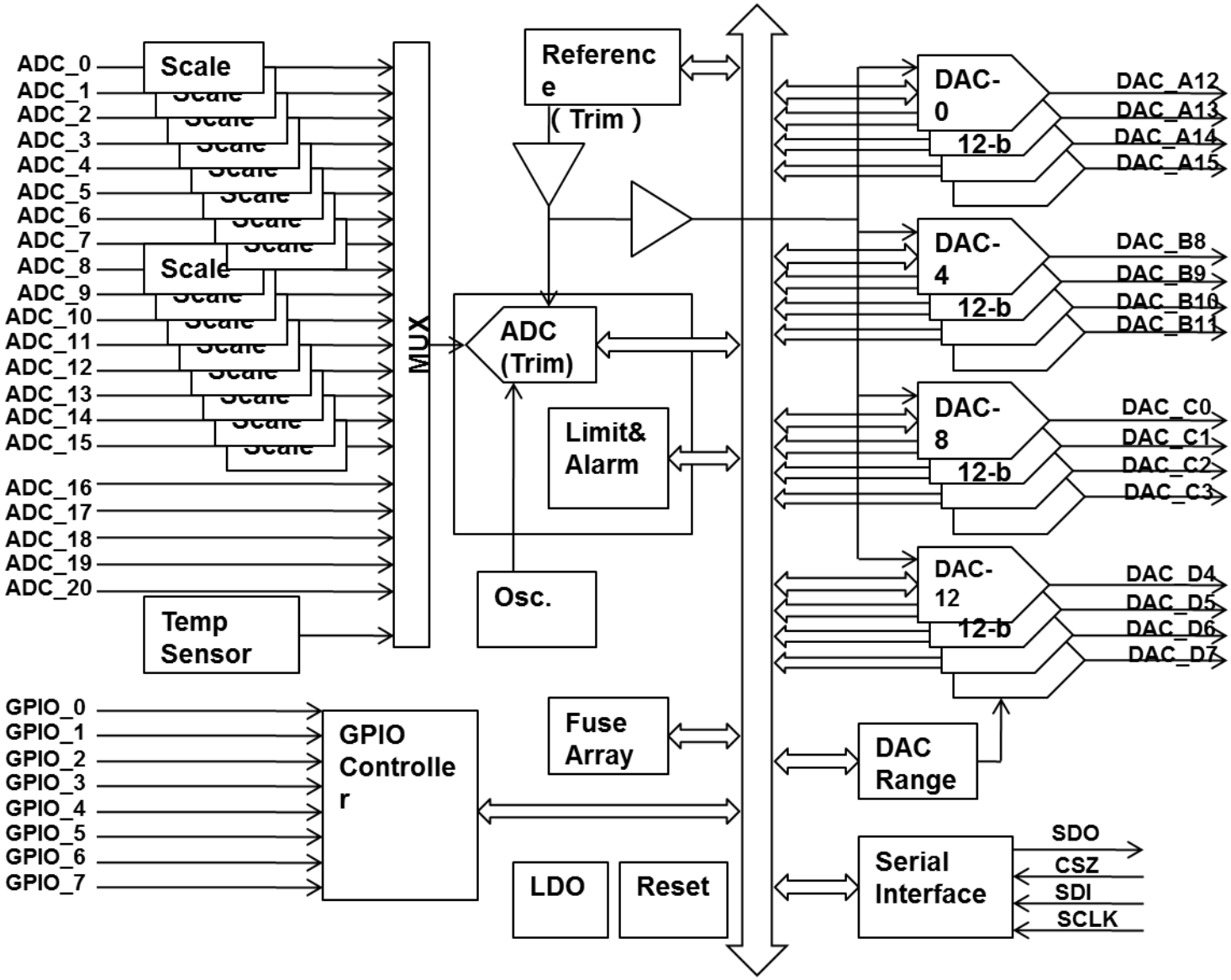
The TPA7836B device is a highly-integrated analog-monitoring and control solution capable of voltage and temperature supervision. The TPA7836B device includes the following features:

- Sixteen 12-bit digital-to-analog converters (DACs) with adjustable output ranges
  - Output ranges: –10 to 0 V, –5 to 0 V, 0 to 5 V, and 0 to 10 V
  - Auto-range detector on device power-up and reset events
  - The DACs power-on and clamp voltages can be pin-selected between AGND and a negative voltage
  - The DACs can be configured to clamp automatically upon detection of an alarm event
- A multi-channel, 12-bit analog-to-digital converter (ADC) for voltage and temperature sensing
  - Sixteen bipolar inputs: –12.5 to 12.5 V input range
  - Five precision inputs with programmable threshold detectors: 0 to 5 V input range
  - Internal temperature sensor
- Internal 2.5 V precision reference
- Eight general purpose I/O (GPIO) ports
- Communication with the device occurs through a 4-wire SPI-compatible interface supporting 1.8 to 5.5 V Operation

The TPA7836B device is characterized for operation over the temperature range of –40ºC to 125ºC which makes the device suitable for harsh-condition applications. The device is available in a 10-mm × 10-mm 64-pin HTQFP PowerPAD IC package.

The very high-integration of the TPA7836B device makes it an ideal all-in-one, low-cost, bias-control circuit for the power amplifiers (PAs) found in multi-channel RF-communication systems. The flexible DAC output ranges allow the device to be used as a biasing solution for a large variety of transistor technologies such as LDMOS, GaAs, and GaN. The TPA836 feature set is similarly beneficial in general-purpose monitor and control systems

7.2 Functional block diagram

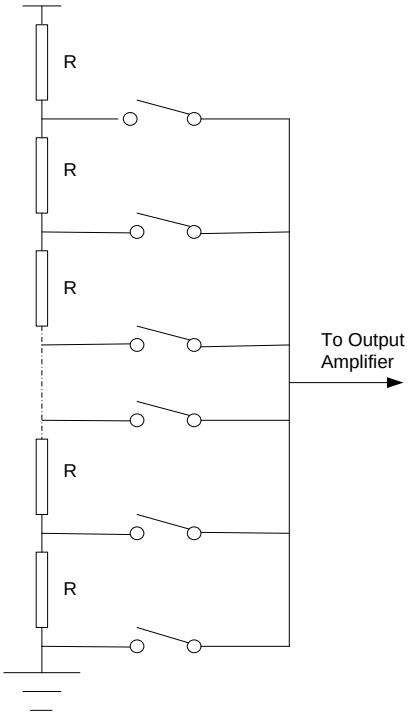


7.3 Feature description

7.3.1 Digital-to-Analog Converters (DACs)

The TPA7836B device features an analog-control system centered on sixteen 12-bits DACs that operate from the Internal reference of the device. Each DAC core consists of a string DAC and output-voltage buffer.
The resistor-string structure consists of a series of resistors, each with a value of R. The code loaded to the DAC Determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is Tapped off by closing one of the switches connecting the string to the amplifier, this architecture has inherent monotonicity, voltage output, and low glitch. This architecture is also linear because all the resistors are of equal value.
The 16 DACs are split into four groups, each with four DACs. All of the DACs in a given group share the same

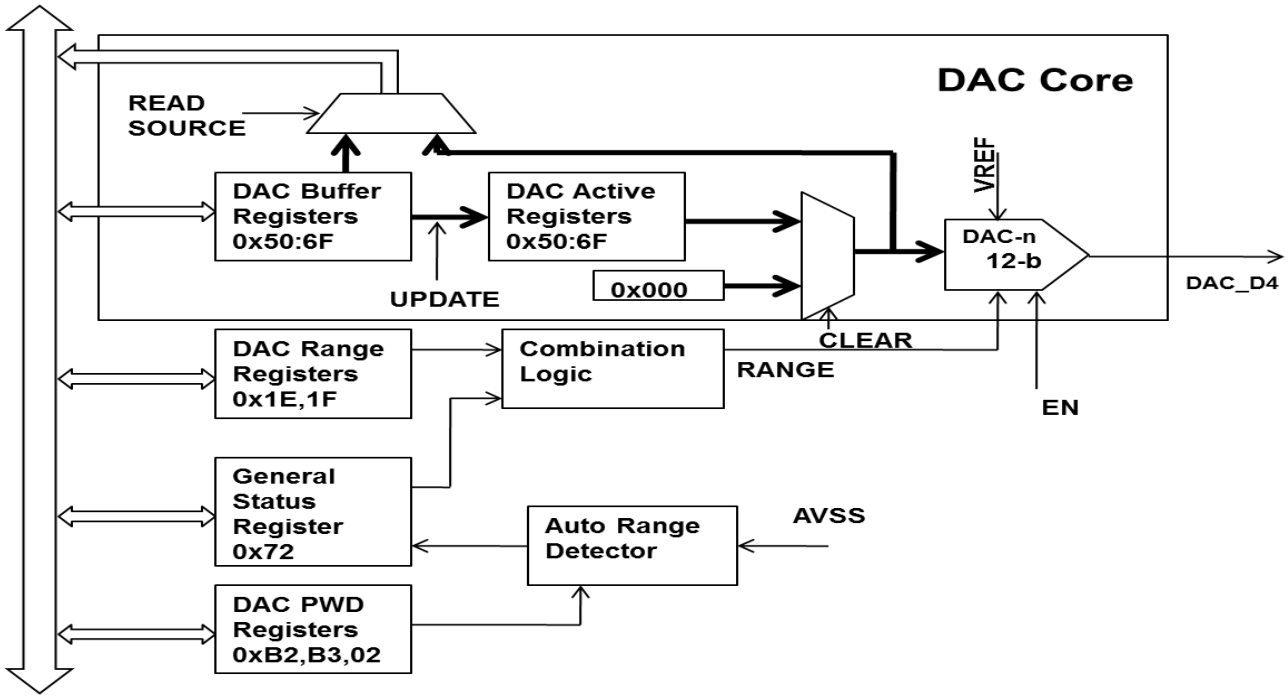
output range and clamp voltage value, however, these settings can be set independently for each DAC group. After power-on or a reset event the following actions take place: the DAC outputs are directed automatically to the corresponding clamp value; the DAC groups output ranges are set by the auto-range detector and; all DAC data registers and data latches are set to the default values



DAC Resistor String

DAC Output Range and Clamp Configuration

The 16 DACs are split into four groups, each with four DACs. All of the DACs in a given group share the same output range and clamp voltage value, however, these settings can be set independently for each DAC group. After power-on or a reset event the following actions take place: the DAC outputs are directed automatically to the corresponding clamp value; the DAC groups output ranges are set by the auto-range detector and; all DAC data registers and data latches are set to the default values. Figure 49 shows a high level block diagram of each DAC in the TPA7836B device.



DAC Block Diagram

Auto-Range Detection

After power-on or a reset event the output range for each DAC group is set automatically by the voltage present in the corresponding AV_{SS} pin (AV_{EE}, AV_{SSB}, AV_{SSC} or AV_{SSD}). When the AV_{SS} voltage of a DAC group is lower than the threshold value, AV_{SSTH}, the output for that DAC group is automatically configured to the –10 to 0 V range. Conversely, if the DAC group AV_{SS} voltage is higher than AV_{SSTH}, the DAC-group output is automatically set to the 0 to 5 V range. The auto-range detector results for each DAC group are stored in the general status register (address 0x72).

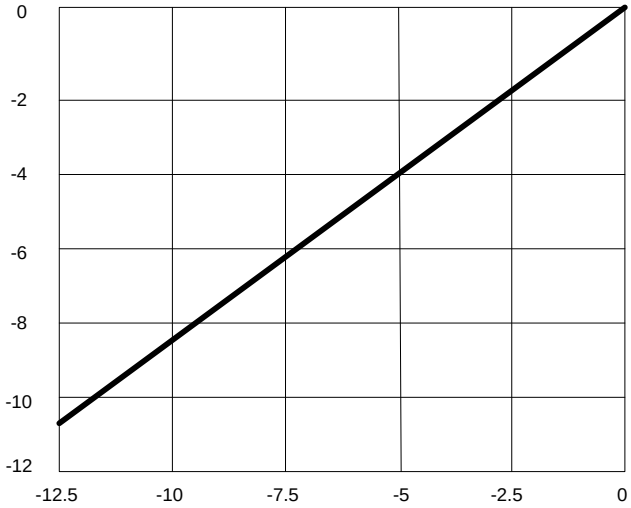
In addition to a power-on or reset event, the auto-range detector is also enabled by a register write to the DAC power down registers (address 0xB2 through 0xB3) or the device configuration register (address 0x02).

Although the initial output-range setting is determined by the auto-range detector, the output range for each DAC-group can be afterwards configured to any of the available output ranges (–10 to 0 V, –5 to 0 V, 0 to 5 V, or 0 to 10 V) through the DAC range registers (address 0x1E through 0x1F).

NOTE

The power-on-reset and clamp-voltage value of each DAC group is set by the corresponding AV_{SS} pin and is independent of the DAC output range. In some applications, matching the clamp-voltage setting to the operating voltage range is imperative. For those applications, the recommended connections for the AV_{SS} pin are:

AGND for the positive output ranges, in which case the clamp voltage is 0 V; a negative supply voltage with a lower value than the minimum DAC output voltage (–5 V or –10 V) for the selected negative output range, in which case the unloaded clamp voltage is determined by the value of the negative supply voltage (see Figure 50).Although not a recommended operating condition, the device allows a DAC group to operate in a positive output range even if its clamp voltage is negative (AV_{SS} connected to a negative supply voltage).



DAC Clamp Output vs AVSS

Aside from setting the clamp voltage and default output range for the DAC group A, the AVEE pin is also the lowest potential in the device. As a consequence the AVEE voltage is dependent on the other AVSS pin connections. The AVEE pin can only be connected to the analog ground if all the other AVSS pins are also connected to the analog ground. If any of the AVSS pins is connected to a negative voltage, the AVEE pin must also be connected to that voltage (see Table 1).

The full-scale output range for each DAC group is limited by the corresponding AVCC and AVSS values. The maximum and minimum outputs cannot exceed the AVCC voltage or be lower than the AVSS voltage, respectively.

DAC GROUP	DAC	AUTO-RANGE AND CLAMP VOLTAGE SELECTION (AVSS)	AVEE = AGND		AVEE = VNEG	
			OUTPUT RANGE	CLAMP VOLTAGE CONNECTION	OUTPUT RANGE	CLAMP VOLTAGE CONNECTION
A	DAC_A0	AVEE	0 to 5 V or 0 to 10 V	AGND	–5 to 0 V or –10 to 0 V	VNEG
	DAC_A1					
	DAC_A2					
	DAC_A3					
B	DAC_B4	AVSSB	0 to 5 V or 0 to 10 V	AGND	–5 to 0 V or –10 to 0 V	VNEG ≤ AVSSB ≤ –5 V
	DAC_B5					
	DAC_B6				0 to 5 V or 0 to 10 V	AGND
	DAC_B7					
C	DAC_C8	AVSSC	0 to 5 V or 0 to 10 V	AGND	–5 to 0 V or –10 to 0 V	VNEG ≤ AVSSC ≤ –5 V
	DAC_C9					
	DAC_C10				0 to 5 V or 0 to 10 V	AGND
	DAC_C11					
D	DAC_D12	AVSSD	0 to 5 V or 0 to 10 V	AGND	–5 to 0 V or –10 to 0 V	VNEG ≤ AVSSD ≤ –5 V
	DAC_D13					
	DAC_D14				0 to 5 V or 0 to 10 V	AGND
	DAC_D15					

Recommended DAC Group Configuration

DAC Register Structure

The input data of the DACs is written to the individual DAC data registers (address 0x50 through 0x6F) in straight binary format for all output ranges (see below Table).

DIGITAL CODE	DAC OUTPUT VOLTAGE (V)			
	0 to 5 V RANGE	0 to 10 V RANGE	–5 to 0 V RANGE	–10 to 0 V RANGE
0000 0000 0000	0	0	–5	–10
0000 0000 0001	0.00122	0.00244	–4.99878	–9.99756
1000 0000 0000	2.5	5	–2.5	–5
1111 1111 1110	4.99756	9.99512	–0.00244	–0.00488
1111 1111 1111	4.99878	9.99756	–0.00122	–0.00244

DAC Data Format

Data written to the DAC data registers is initially stored in the DAC buffer registers. The transfer of data from the DAC buffer registers to the active registers is initiated by an update command in the register update register (address 0x0F). When the active registers are updated, the DAC outputs change to the new values.
The host has the option to read from either the buffer registers or the active registers when accessing the DAC data registers. The DAC read back option is configured by the READBACK bit in the interface configuration 1 register (address 0x01).

DAC Clear Operation

Each DAC can be set to a CLEAR state using either hardware or software. When a DAC goes to CLEAR state, it is loaded with a zero-code input and the output voltage is set according to the operating output range. The DAC buffer or active registers do not change when the DACs enter the CLEAR state which makes it possible to return to the same voltage output before the clear event was issued. Even though the contents of the active register do not change while a DAC is in CLEAR state, a data-register read operation from the active registers while in this state returns zero-code. This functionality enables the ability to determine the DAC output voltage regardless of the operating state (CLEAR or NORMAL).

NOTE

The DAC buffer and active registers can be updated while the DACs are in CLEAR state allowing the DACs to output new values upon return to normal operation. When the DACs exit the CLEAR state, the DACs are immediately loaded with the data in the DAC active registers and the output is set back to the corresponding level to restore operation.

The DAC clear registers (address 0xB0 through 0xB1) enable independent control of each DAC CLEAR state through software. The DACs can also be forced to enter a CLEAR state through hardware using the $\overline{\text{ALARMIN}}$ pin. See the *Programmable Out-of-Range Alarms* section for a detailed description of this method.

The $\overline{\text{ALARMIN}}$-controlled clear mechanism is just a special case of the device capability to force the DACs into the CLEAR state as a response to an alarm event. To enable this function, the alarm events must first be enabled as DAC-clear alarm sources in the DAC clear source registers (address 0x1A through 0x1B). The DAC outputs to be cleared by the selected alarm events must also be specified in the DAC clear enable registers (address 0x18 through 0x19).

An alarm event sets the corresponding alarm bit in the alarm status registers. In addition all the DACs set to clear in response to the alarm event in the DAC clear enable registers enter a CLEAR state. Once the alarm bit

is cleared, as long as no other CLEAR-state controlling alarm events have been triggered, the DACs are reloaded with the contents of the DAC active registers and the outputs update accordingly.

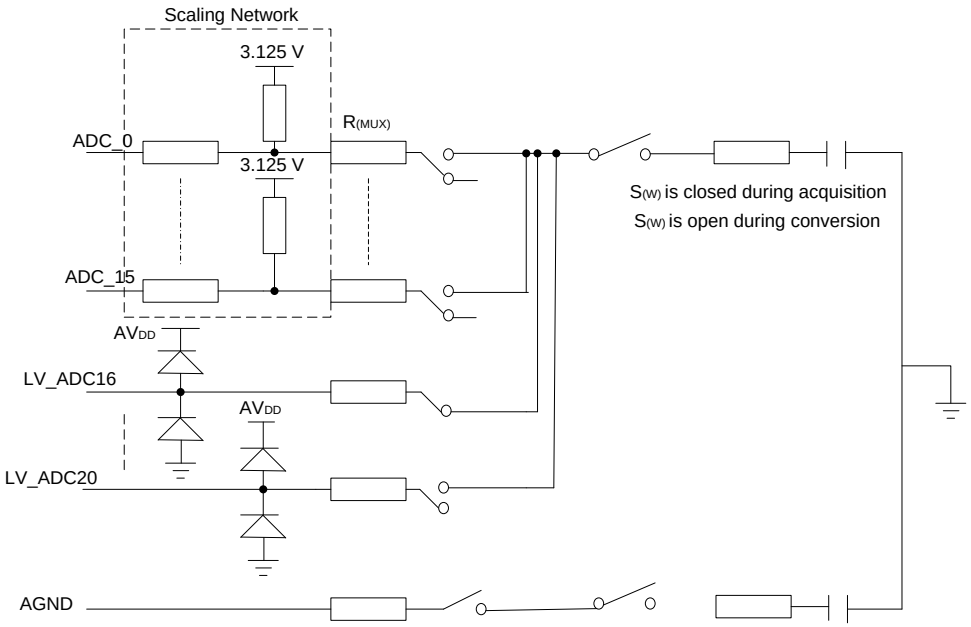
Analog-to-Digital Converter (ADC)

The TP7836 features a monitoring system centered on a 12-bit SAR (successive approximation register) ADC fronted by a 22-channel multiplexer and an on-chip track-and-hold circuit. The monitoring systems is capable of sensing up to 16 external bipolar inputs (–12.5 to 12.5 V range), five external unipolar inputs (0 to 5 V range), and an internal analog temperature sensor.

The ADC operates from an internal 2.5 V reference (V_{ref}, measured at the REF_CMP pin) and the input range is 0 V to 2 × V_{ref}. The external bipolar inputs to the ADC are internally mapped to this range. The ADC timing signals are derived from an on-chip temperature-compensated oscillator. The conversion results can be accessed through the device serial interface

Analog Inputs

The TPA7836B has 21 analog inputs for external voltage sensing. Sixteen of these inputs (ADC_0 through ADC_15) are bipolar and the other five (LV_ADC16 through LV_ADC20) are unipolar. Figure 51 shows the equivalent circuit for the external analog-input pins. All switches are open while the ADC is in the IDLE state.



ADC External Inputs Equivalent Circuit

To achieve the specified performance, especially at higher input frequencies, driving each analog input pin with a low impedance source is recommended. An external amplifier can also be used to drive the input pins.

Bipolar Analog Inputs

The TPA7836B can support up to 16 bipolar analog inputs. The analog input range for these channels is –12.5 to 12.5 V. The bipolar signal is scaled internally through a resistor divider so that it maps to the native input range of the ADC (0 V to 2 × V_{ref}). The input resistance of the scaling network is 170 kΩ.

The bipolar analog input conversion values are stored in straight binary format in the ADC data registers (address 0x20 through 0x49). The LSB (least-significant bit) size for these channels is 25 × V_{ref} / 4096. With the internal reference equal to 2.5 V, the input voltage is calculated by **Voltage=5*(CODE*5/4096-2.5)**

A typical application for the bipolar channels is monitoring of the 16 DAC outputs in the device. In this application the bipolar inputs can be driven directly. However, in applications where the signal source has high impedance, buffering the analog input is recommended. When driven from a low impedance source such as the TPA7836B

DAC outputs, the network is designed to settle before the start of conversion. Additional impedance can affect the settling and divider accuracy of this network

Unipolar Analog Inputs

In addition to the bipolar input channels, the TPA7836B device includes five unipolar analog inputs. The analog input range for these channels is 0 V to 2 × V_{ref} and the LSB size for these channels is 2 × V_{ref} / 4096.

The unipolar analog input conversion values are stored in straight binary format in the ADC-Data registers (address 0x40 through 0x49). With the internal reference equal to 2.5 V, the input voltage is calculated by **Voltage= (CODE*5/4096)**

In applications where the signal source has high impedance, externally buffering the unipolar analog input is Recommended

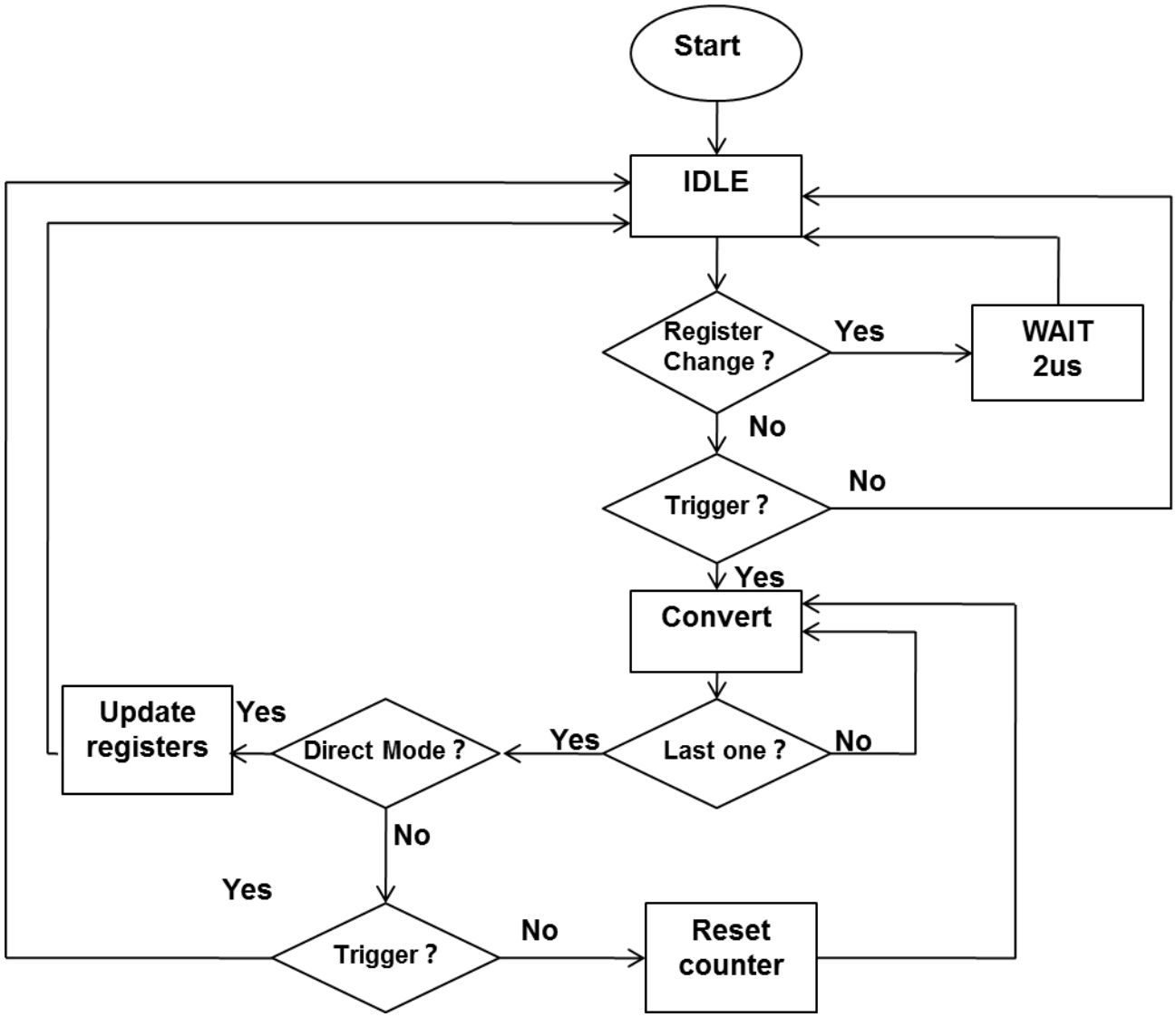
ADC Sequencing

The TPA7836B ADC conversion sequence is shown in Figure 52. The ADC supports direct mode and auto mode conversion. The conversion method is selected in the ADC configuration register (address 0x10). The default conversion method is direct mode.

In both methods, the single channel or sequence of channels to be converted by the ADC must be first configured in the ADC MUX configuration registers (address 0x13 through 0x15). The input channels to the ADC include 16 external bipolar inputs, five external unipolar inputs, and the internal temperature sensor.

In direct-mode conversion, the selected ADC input channels are converted on demand by issuing an ADC trigger signal. After the last enabled channel is converted, the ADC enters IDLE state and waits for a new trigger.

In auto-mode conversion, the selected ADC input channels are converted continuously. The conversion cycle is initiated by issuing an ADC trigger. Upon completion of the first conversion sequence another sequence is automatically started. Conversion of the selected channels occurs repeatedly until the auto-mode conversion is stopped by issuing a second trigger signal.



ADC Conversion Sequence

Regardless of the selected conversion method, the following ADC registers should only be updated while the ADC is in IDLE state

- ADC configuration register (address 0x10)
- False alarm configuration register (address 0x11)
- ADC MUX configuration registers (address 0x13 through 0x15)
- Threshold registers (0x80 through 0x97)
- Hysteresis register (0xA0 through 0xA5)

NOTE

After updating any of the ADC registers listed above, a minimum 2 µs wait time should be implemented before issuing an ADC trigger.

ADC Synchronization

A trigger signal must occur for the ADC to enter and exit the IDLE state. The ADC trigger can be generated either through software (ICONV bit in the ADC trigger register, 0xC0) or hardware (GPIO2/$\overline{\text{ADCTRIG}}$, pin 9). To use the GPIO2/$\overline{\text{ADCTRIG}}$ pin as an ADC trigger, the pin must be configured accordingly in the GPIO configuration register (address 0x12). When the pin is configured as a trigger, a falling edge on it begins the sampling and conversion of the ADC.

In auto mode the ADC and temperature data registers (0x20 through 0x4B) are accessed by first issuing an ADC UPDATE command in the register update register (address 0x0F). The ADC UPDATE command ensures the latest available data for each input channel can be accessed without the need for complex synchronization schemes between the TPA7836B device and the host controller. A single ADC UPDATE command updates all ADC and temperature data registers. Therefore issuing multiple UPDATE commands is not necessary when reading more than one ADC data register.

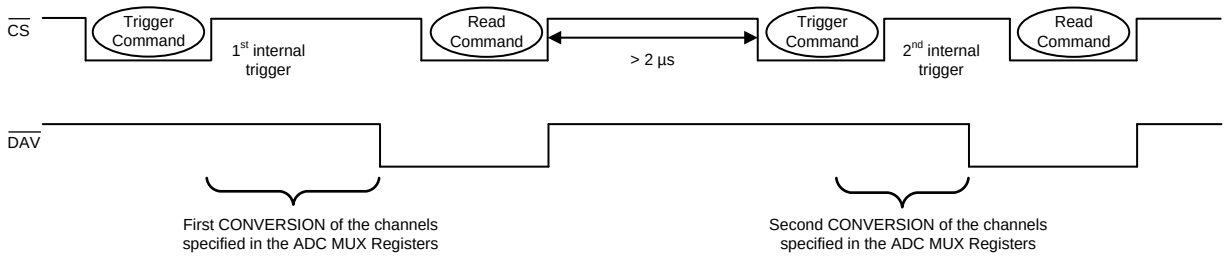
NOTE

The ADC UPDATE command and accessing of the ADC and Temperature data registers does not interfere with the conversion process which ensures continuous ADC operation.

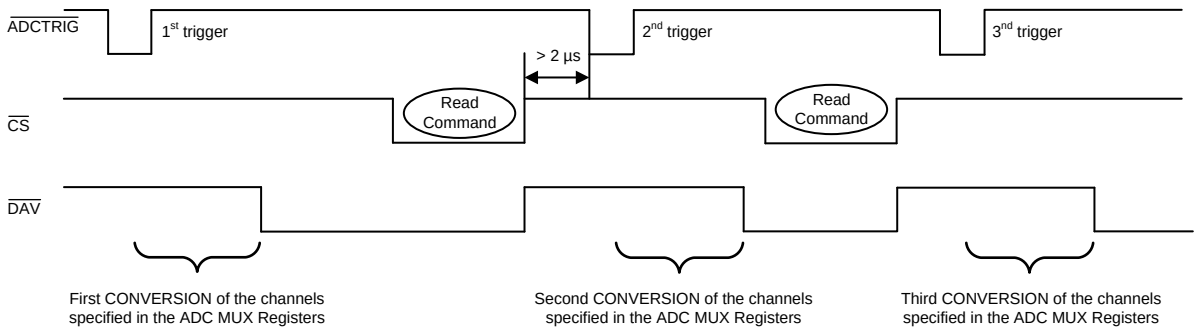
In direct mode the ADC and temperature data registers (0x20 through 0x4B) should only be accessed while the ADC is in the IDLE state (see Figure 53). Although the total update time can be easily calculated, the device provides a data-available indicator signal to track the ADC status. Failure to satisfy the synchronization requirements could lead to erroneous data reads.

The data-available indicator signal is output through the GPIO3/$\overline{\text{DAV}}$ pin and as a data-available flag that is accessible through the serial interface (DAVF bit in the general status register, 0x72). The GPIO3/$\overline{\text{DAV}}$ pin must be configured in the GPIO configuration register (address 0x12) as an interrupt. After a direct-mode conversion is complete and the ADC returns to the IDLE state, the DAVF bit is immediately set to 1 and the $\overline{\text{DAV}}$ pin is active (low) which indicates that new data is available. The pin and flag are cleared automatically when a new conversion begins or one of the ADC data or temperature data registers is accessed

a) Direct Mode, Software Trigger



b) Direct Mode, Hardware Trigger

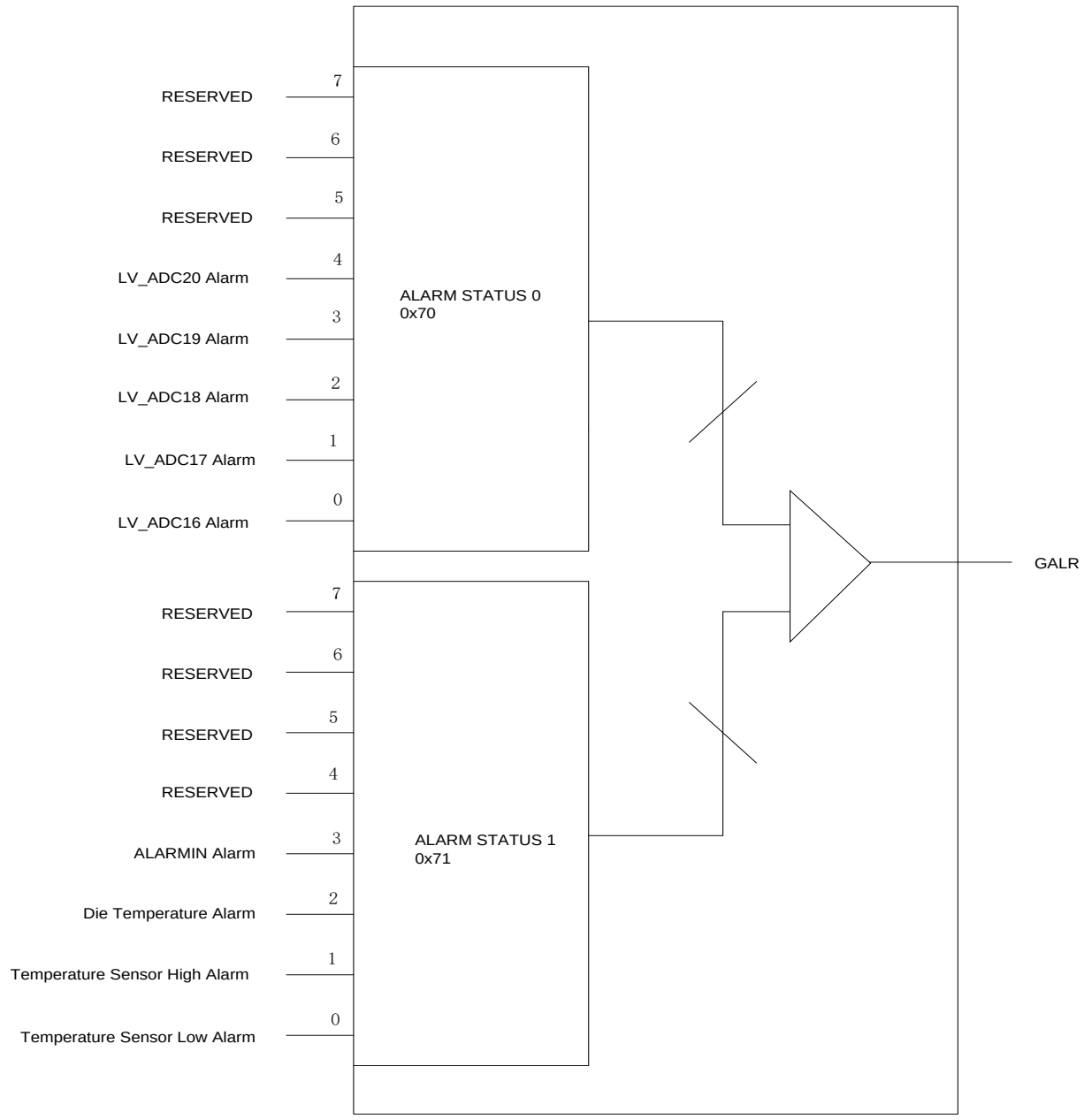


Programmable Out-of-Range Alarms

The TPA7836B device is capable of continuously analyzing the five external unipolar inputs and internal temperature sensor conversion results for normal operation.

Normal operation is established through the lower and upper threshold registers (address 0x80 through 0x97). When any of the monitored inputs is out of the specified range, an alarm event is issued and the global alarm bit,

GALR in the general status register (0x72), is set (see Figure 54). Use the alarm status registers (0x70 through 0x71) to determine the source of the alarm event.



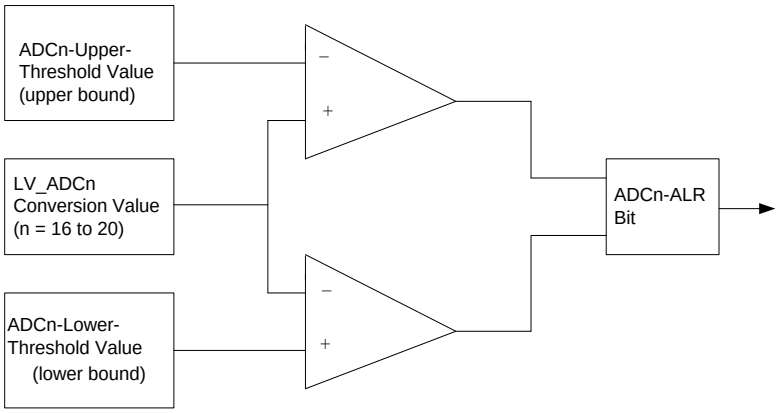
The ALARM-LATCH-DIS bit in the $\overline{\text{ALARMOUT}}$ source 1 register (address 0x1D) sets the latching behavior for all alarms (except for the $\overline{\text{ALARMIN}}$ alarm which is always unlatched). When the ALARM-LATCH-DIS bit is cleared to 0 the alarm bits in the alarm status registers are latched. The alarm bits are referred to as being latched because they remain set until read by software. This design ensures that out-of-limit events cannot be missed if the software is polling the device periodically. All bits are cleared when reading the alarm status registers, and all bits are reasserted if the out-of limit condition still exists on the next monitoring cycle, unless otherwise noted. When the ALARM-LATCH-DIS bit is set to 1, the alarm bits are not latched. The alarm bits in the alarm status registers are set to 0 when the error condition subsides, regardless of whether the bit is read or not.

All of the alarms can be set to activate the $\overline{\text{ALARMOUT}}$ pin. To enable this functionality, the GPIO1/$\overline{\text{ALARMOUT}}$ pin must be configured accordingly in the GPIO configuration register (address 0x12). The ALARMOUT pin works as an interrupt to the host so that it can query the alarm status registers to determine the alarm source.

Any alarm event can activate the pin as long as the alarm is not masked in the $\overline{\text{ALARMOUT}}$ source registers (address 0x1C through 0x1D). When an alarm event is masked, the occurrence of the event sets the corresponding status bit in the alarm status registers, but does not activate the $\overline{\text{ALARMOUT}}$ pin.

Bipolar Inputs Out-of-Range Alarms

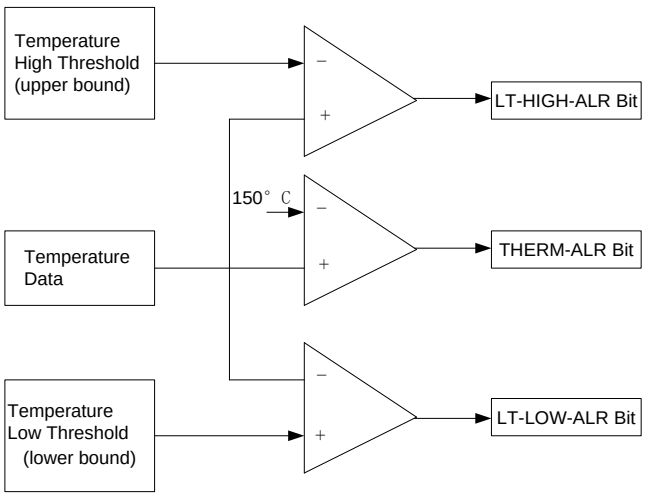
The TPA7836B device provides out-of-range detection for the five external unipolar ADC inputs (LV_ADC16 through LV_ADC20, pins 35 through 39). Figure 55 shows the out-of-range detection block. When the measurement is out-of-range, the corresponding alarm bit in the alarm status 0 register (address 0x70) is set to 1 to flag the out-of-range condition. The values in the ADC upper and lower Threshold registers (address 0x80 through 0x93) define the upper and lower bound thresholds for all five inputs



Unipolar Inputs Out-of-Range Alarms

The TPA7836B includes high-limit and low-limit detection for the internal temperature sensor. Figure 56 shows the temperature detection block. The values in the LT upper and lower threshold registers (address 0x94 through 0x97) set the limits for the temperature sensor. The temperature sensor detector can issue either a high-alarm (LT-HIGH-ALR bit) or a low-alarm (LT-LOW-ALR bit) in the alarm status 1 register (address 0x71) depending on whether the high or low thresholds were exceeded. To implement single, upper-bound threshold detection for the temperature sensor, the host processor can set the upper-bound threshold to the desired value and the lowerbound threshold to the default value. For lower-bound threshold detection, the host processor can set the lowerbound threshold to the desired value and the upper-bound threshold to the default value.

In addition to the programmable threshold alarms the temperature sensor detection circuit also includes a die thermal-alarm flag which continuously monitors the die temperature. When the die temperatures exceeds 150˚C the die thermal alarm flag (THERM-ALR bit) in the alarm status 1 register (address 0x71) is set. The internal temperature sensor must be enabled for this alarm to be functional.



$\overline{\text{ALARMIN}}$ Alarm

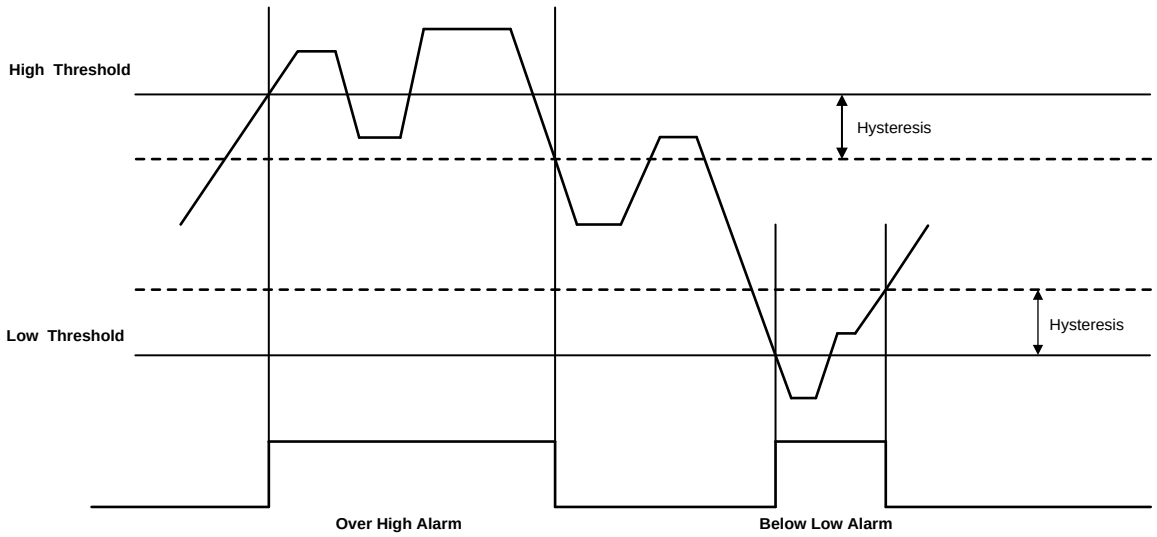
The TPA7836B device offers the option of using an external interrupt signal, such as the output of a comparator as an alarm event. The GPIO0/$\overline{\text{ALARMIN}}$ pin is used as the alarm input and must be configured accordingly in the GPIO configuration register (address 0x12). The pin is active low when configured as an alarm input.

A typical application for $\overline{\text{ALARMIN}}$ pin is to use it as a hardware interrupt that is responsible for forcing one or more DACs to a CLEAR state. The DAC is loaded with a zero-code input and the output voltage is set according to the operating output range, however the DAC buffer or active registers do not change (see the Digital-to-Analog Converters (DACs) section for more details). To enable this functionality the $\overline{\text{ALARMIN}}$ pin must be enabled as a DAC clear-alarm source in the DAC clear source 1 register (address 0x1B). Additionally the DAC outputs to be cleared by the $\overline{\text{ALARMIN}}$ pin must be specified in the DAC clear enable registers (address 0x18 through 0x19).

In this application when the $\overline{\text{ALARMIN}}$ pin goes low, all the DACs that are set to clear in response to the $\overline{\text{ALARMIN}}$ Alarm in the DAC-clear enable registers enter a CLEAR state. When the $\overline{\text{ALARMIN}}$ pin goes back high the DACs are reloaded with the contents of the DAC active registers which allows the DAC outputs to return to the previous operating point without any additional commands.

Hysteresis

the alarm condition is cleared only when the conversion result returns either a value lower than the high threshold register setting or higher than the low threshold register setting by the number of codes specified in the hysteresis setting (see Figure 57). The ADC and LT hysteresis registers (address 0xA0 through 0xA4) store the hysteresis value for the external unipolar inputs and internal temperature sensor programmable alarms. The hysteresis is a programmable value between 0 LSB to 127 LSB for the unipolar inputs alarms and 0°C to 31°C for the internal temperature-sensor alarms. The die thermal alarm hysteresis is fixed at 8°C.



False-Alarm Protection

To prevent false alarms, an alarm event is only registered when the monitored signal is out of range for an *N* number of consecutive conversions. If the monitored signal returns to the normal range before N consecutive conversions, an alarm event is not issued. The false alarm factor, N, for the unipolar input and local temperature sensor out-of-range alarms can be configured in the false alarm configuration register (address 0x11).

Internal Temperature Sensor

The TPA7836B device has an on-chip temperature sensor that measures the device die temperature. The normal operating temperature range for the internal temperature sensor is limited by the operating temperature range of the device (–40°C to 125°C).

The temperature sensor results are converted by the device ADC at a lower speed than the analog input channels. The temperature can be monitored either continuously or as a single-time conversion depending on whether the ADC is configured in auto mode or direct mode (see the *Analog-to-Digital Converter (ADC)* section for more details). If the temperature sensor is not needed, it can be disabled in the ADC MUX configuration 2 register (address 0x15). When disabled, the temperature sensor output is not converted by the ADC.
The temperature sensor provides 0.25°C resolution over the operating temperature range. The temperature value is stored in 12-bit two's complement format in the temperature data registers (address 0x78 through 0x79).

Temperature Sensor Data Format

TEMPERATURE (°C)	DIGITAL CODE
–40	1111 0110 0000
–25	1111 1001 1100
–10	1111 1101 1000
–0.25	1111 1111 1111
0	0000 0000 0000
0.25	0000 0000 0001
10	0000 0010 1000
25	0000 0110 0100
50	0000 1100 1000
75	0001 0010 1100
100	0001 1001 0000
105	0001 1010 0100
125	0001 1111 0100

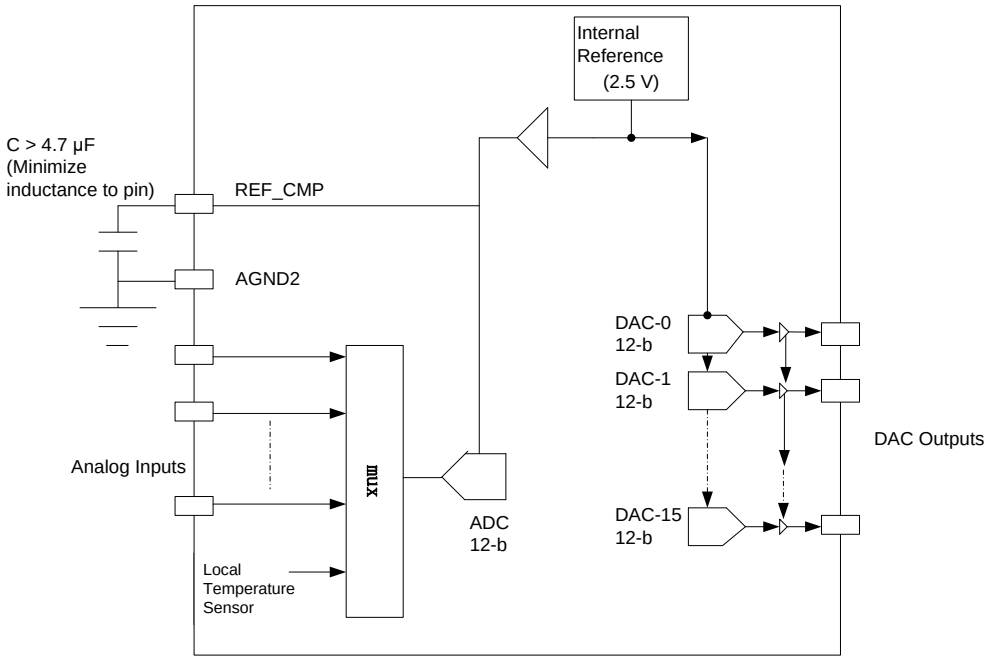
Use Equation 3 and Equation 4 to calculate the positive or negative temperature according to the polarity of the temperature data MSB (0 - positive, 1 - negative).

Positive Temperature (^{0}C) =ADC_CODE/4 (3)

Negative Temperature (^{0}C) = (4096-ADC_CODE)/4 (4)

Internal Reference

The TPA7836B device includes a high-performance internal reference for the on-chip ADC and 16 DACs (see Figure 58). The internal reference is a 2.5 V, bipolar transistor-based, precision bandgap reference. A compensation capacitor (4.7 µF, typical) should be connected between the REF_CMP pin and the AGND2 pin. The TPA7836B device includes a buffer to drive the ADC and should not be used to drive any external circuitry. The ADC reference buffer is powered down by default and should be enabled in the ADC configuration register (address 0x10) during device initialization.



General Purpose I/Os

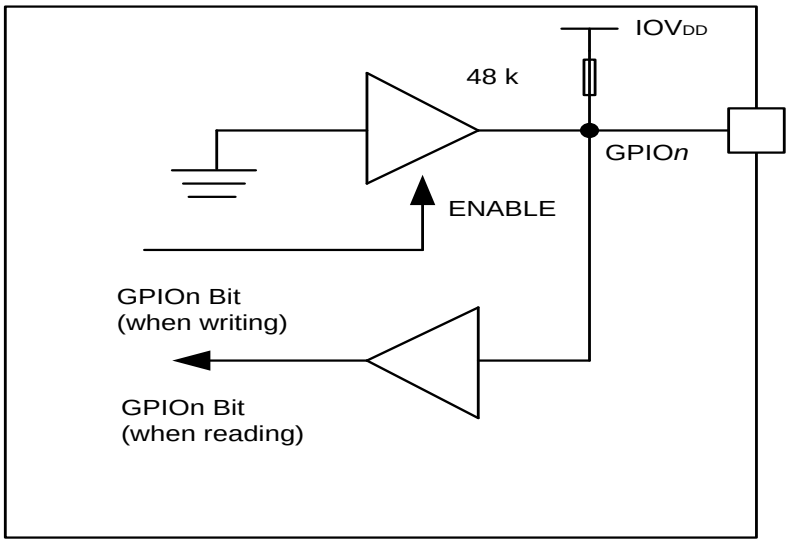
The TPA7836B device includes eight GPIO pins, each with an internal 48-kΩ pullup resistor to the IOV_{DD} pin. The GPIO[0:3] pins have dual functionality and can be programmed as either bidirectional digital I/O pins or interrupt signals in the GPIO configuration register (address 0x12). The GPIO[4:7] pins are dedicated GPIOs. Table 4 lists the dual function of the GPIO[0:3] pins.

Dual Functionality GPIO Pins

PIN	DEFAULT PIN NAME	ALTERNATIVE PIN NAME	ALTERNATIVE FUNCTIONALITY
7	GPIO0	$\overline{\text{ALARMIN}}$	DAC clear control signal.
8	GPIO1	$\overline{\text{ALARMOUT}}$	Global alarm output
9	GPIO2	$\overline{\text{ADCTRIG}}$	External ADC conversion trigger
10	GPIO3	$\overline{\text{DAV}}$	ADC data available indicator

The GPIOs can receive an input or produce an output. When the GPIOn pin acts as an output, the status of the pin is determined by the corresponding GPIO bit in the GPIO register (address 0x7A).

To use a GPIOn pin as an input, the corresponding GPIO bit in the GPIO register must be set to 1. When a GPIOn pin acts as input, the digital value on the pin is acquired by reading the corresponding GPIO bit. After a power-on reset (POR) or any forced reset, all GPIO bits are set to 1, and the GPIOn pins have a 48-kΩ input impedance to the IOV_{DD} pin (see Figure 59). The unused GPIO pins can be left floating.



7.4 Device Functional Modes

The sixteen DACs in the TPA7836B device are split into four groups, each with four DACs. The output range and clamp voltage for each DAC group is set independently which enables the device to operate in one of the following modes:

- All-positive DAC range mode
- All-negative DAC range mode
- Mixed DAC range mode

All-Positive DAC Range Mode

In the TPA7836B all-positive DAC range mode, each of the four DAC groups is set to a positive voltage output range (0 to 5 V or 0 to 10 V).

Because the maximum DAC output for each group cannot exceed the common AV_{CC} voltage for the device ($AV_{CC} = AV_{CC\_AB} = AV_{CC\_CD}$), a DAC group in the 0 to 10 V output range forces the AV_{CC} voltage to a value greater or equal to 10 V even if the remaining DAC groups are set in the 0 to 5 V range. If all DAC groups are set in the 0 to 5 V range the AV_{CC} voltage can be set to a value as low as 5 V.

The minimum DAC output for each group cannot be lower than the AV_{SS} voltage but because the minimum DAC output is 0 V in the all-positive DAC range mode, all of the AV_{SS} pins (AV_{EE}, AV_{SSB}, AV_{SSC}, and AV_{SSD}) as well as the device thermal pad can be tied to AGND thus simplifying the board design. Table 5 lists the typical configurations for this mode.

All-positive DAC Range Mode Typical Configuration

PIN	NOTES	TYPICAL CONNECTION
AV_{DD}		5 V
DV_{DD}	DV_{DD} must be equal to AV_{DD}.	5 V
IOV_{DD}	IOV_{DD} must be equal to or less than DV_{DD}	1.8 V to 5 V
AV_{CC_AB}, AV_{CC_CD}	The AV_{CC_AB} and AV_{CC_CD} pins must be tied to the same potential (AV_{CC}), AV_{CC} must be greater or equal than the maximum possible output voltage for any of the sixteen DACs.	$AV_{CC} \geq 5$ V $AV_{CC} \geq 10$ V
AV_{EE}		AGND
AV_{SSB}, AV_{SSC}, AV_{SSD}		AGND
Thermal Pad		AGND

After power-on or a reset event the output range for each DAC group is set automatically by the voltage present on the corresponding AV_{SS} pin. In the all-positive DAC range mode all AV_{SS} pins are connected to AGND and consequently all four DAC groups will initialize by default to the 0 to 5 V range. The output for any of the DAC groups can be modified to the 0 to 10 V range after initialization by setting the corresponding DAC range register (address 0x1E to 0x1F) to 110b.

In addition to setting the default output range, the AV_{SS} pins also set the clamp voltage for each DAC group. Because the clamp voltage is only dependent on the voltage in the AV_{SS} pin, changes to the DAC range registers do not affect the clamp setting. With the AV_{SS} pins connected to AGND, the clamp voltage for all sixteen DACs is 0 V.

All-Negative DAC Range Mode

In the TPA7836B all-negative DAC range mode, each of the four DAC groups is set to a negative voltage output range (–5 to 0 V or –10 to 0 V).

Although the maximum DAC output does not exceed 0 V, the common AV_{CC} voltage (AV_{CC} = AV_{CC_AB} = AV_{CC_CD}) must still satisfy a minimum voltage of 4.5 V to comply with the device operating conditions. In this case a recommended approach is to tie the AV_{CC}, AV_{DD}, and DV_{DD} supply pins to a common potential.

The minimum DAC output for each group cannot be lower than the voltage on the corresponding AV_{SS} pins (AV_{EE}, AV_{SSB}, AV_{SSC}, and AV_{SSD}). The AV_{SS} pins are not required to be tied to the same potential and typically the negative voltage at each AV_{SS} pin is dictated by the desired operating DAC negative output range. One exception is the AV_{EE} pin which must be the lowest potential in the device. The thermal pad should be either tied to the same potential as the AV_{EE} pin or left disconnected. Table 6 lists the typical configurations for this mode

All-Negative DAC Range Mode Typical Configuration

PIN	NOTES	TYPICAL CONNECTION
AV_{DD}		5 V
DV_{DD}	DV_{DD} must be equal to AV_{DD}	5 V
IOV_{DD}	The AV_{CC_AB} and AV_{CC_CD} pins must be tied to the same potential (AV 5 V CC)	1.8 V to 5 V
AV_{CC_AB}, AV_{CC_CD}	AV_{EE} must be the lowest potential in the device AV_{EE} must be less than or equal to the minimum possible output voltage for DAC group A.	5 V
AV_{EE}	AV_{SSn} must be less than or equal to the minimum possible output voltage for DAC group n (n = B, C, D).	$AV_{EE} \le –5$ V $AV_{EE} \le –10$ V
AV_{SSB}, AV_{SSC}, AV_{SSD}		$AV_{EE} \le AV_{SSn} \le –5$ V $AV_{EE} \le AV_{SSn} \le –10$ V
Thermal Pad		AV_{EE} or Floating

After power-on or a reset event the output range for each DAC group is set automatically by the voltage present in the corresponding AV_{SS} pin. In the all-negative DAC range mode all AV_{SS} pins should be connected to a voltage lower than AV_{SSTH}. If this condition is satisfied, all four DAC groups will initialize by default to the –10- to 0-V range. Because the negative clamp voltage is only dependent on the voltage in the AV_{SS} pin, the default –10- to 0-V output range presents no risk even when the AV_{SS} voltage is greater than –10 V. In this case the DAC group output should be modified to the –5 to 0 V range after initialization by setting the corresponding DAC range register (address 0x1E to 0x1F) to 101b.

Mixed DAC Range Mode

In the TPA7836B mixed DAC range mode, a combination of DAC groups is set to a negative voltage output range (–5 to 0 V or –10 to 0 V) and a positive voltage output range (0 to 5 V or 0 to 10 V).

Because the maximum DAC output for each group cannot exceed the common AV_{CC} voltage for the device (AV_{CC} = AV_{CC_AB} = AV_{CC_CD}), a DAC group in the 0 to 10 V output range forces the AV_{CC} voltage to a value greater or equal to 10 V. If all positive DAC groups are in the 0 to 5 V range the AV_{CC} voltage can be set to a value as low as 5 V.

The minimum DAC output for each group cannot be lower than the voltage on the corresponding AV_{SS} pins (AV_{EE}, AV_{SSB}, AV_{SSC} and AV_{SSD}). The AV_{SS} pins are not required to be tied to the same potential and typically the negative voltage at each AV_{SS} pin is dictated by the desired operating DAC negative output range. One exception is the AV_{EE} pin which must be the lowest potential in the device. The implication of this requirement is that if either DAC group B, C or D is set to a negative output range, DAC group A must also be set to a negative range. The thermal pad should be either tied to the same potential as the AV_{EE} pin or left disconnected. Table 7 lists the typical configurations for this mode.

Mixed DAC Range Mode Typical Configuration

PIN	NOTES	TYPICAL CONNECTION	
AV_{DD}		5 V	
DV_{DD}	DV_{DD} must be equal to AV_{DD}.	5 V	
IOV_{DD}	IOV_{DD} must be equal to or less than DV_{DD}.	1.8 V to 5 V	
AV_{CC_AB}, AV_{CC_CD}	The AV_{CC_AB} and AV_{CC_CD} pins must be tied to the same potential (AV_{CC}). AV_{CC} must be greater or equal to the maximum possible output voltage for any of the positive output range DACs	AV_{CC} ≥ 5 V AV_{CC} ≥ 10 V	
AV_{EE}	AVEE must be the lowest potential in the device. AV_{EE} must be less than or equal to the minimum possible output voltage for DAC group A.	AVEE ≤ –5 V AVEE ≤ –10 V	
AV_{SSB}, AV_{SSC}, AV_{SSD}	AV_{SSn} must be less than or equal than the minimum possible output voltage for DAC group n (n = B, C, D).	Negative Range	AV_{EE} ≤ AV_{SSn} ≤ –5 V AV_{EE} ≤ AV_{SSn} ≤ –10 V
		Positive Range	AGND
Thermal Pad		AV_{EE} or Floating	

After power-on or a reset event the output range for each DAC group is set automatically by the voltage present in the corresponding AV_{SS} pin. When the AV_{SS} voltage of a DAC group is lower than the threshold value, AV_{SSTH}, the output for that DAC group is automatically configured to the –10 to 0 V range. Conversely, if the AV_{SS} voltage of the DAC group is higher than AV_{SSTH}, the DAC-group output is automatically set to the 0 to 5 V range. The output for any of the DAC groups can be modified after initialization by setting the corresponding DAC range register (address 0x1E to 0x1F).

In addition to setting the default output range, the AV_{SS} pins also set the clamp voltage for each DAC group. Because the clamp voltage is only dependent on the voltage in the AV_{SS} pin, changes to the DAC range registers do not affect the clamp setting.

NOTE

Although not a recommended operating condition, the device allows a DAC group to operate in a positive output range even if the clamp voltage is negative (AVSS connected to a negative supply voltage).

7.5 Programming

The TPA7836B device is controlled through a flexible four-wire serial interface that is compatible with SPI-type interfaces used on many microcontrollers and DSP controllers. The interface provides read and write (R/W) access to all registers of the TPA7836B device.

Each serial-interface access cycle is exactly (N + 2) bytes long, where N is the number of data bytes. Asserting the CS pin low initiates a frame. The frame ends when the CS pin is de-asserted high. In MSB-first mode, the first bit transferred is the R/W bit. The next 15 bits are the register address (32768 addressable registers), and the remaining bits are data. For all writes, data is committed in bytes as the eight data bit of a data field that is clocked in on the rising edge of SCLK. If the write access is not an even multiple of 8 clocks, the trailing data bits are not committed. On a read access, data is clocked out on the falling edge of the serial interface clock, SCLK, on the SDO pin.

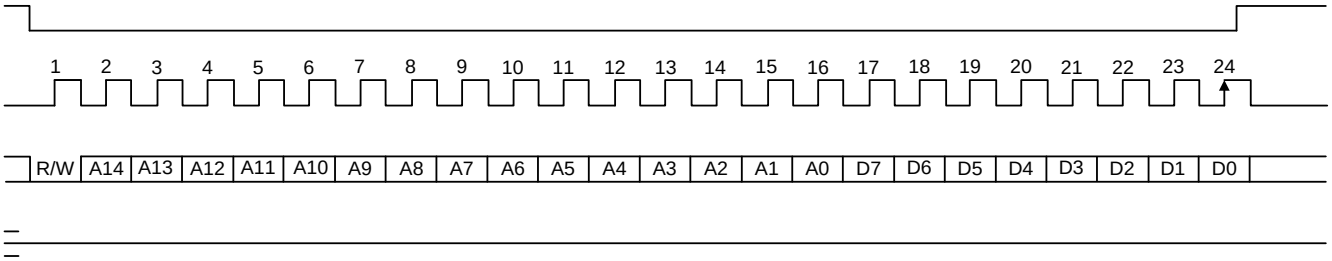


Figure 60. Serial Interface Write Bus Cycle

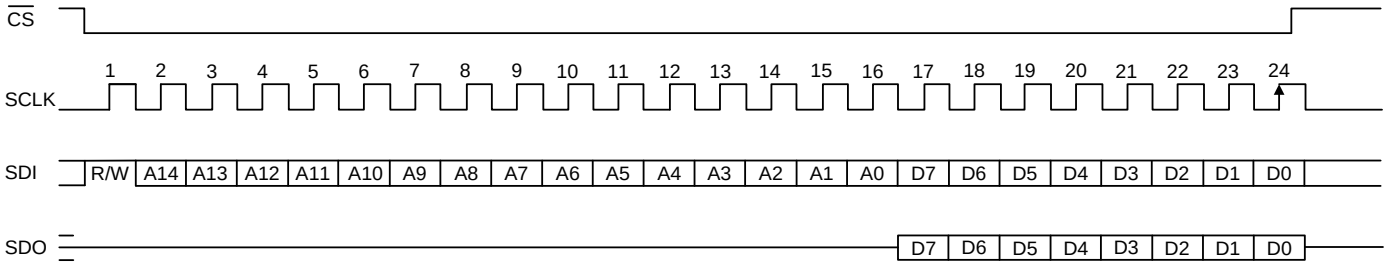


Figure 61. Serial Interface Read Bus Cycle

Streaming mode is supported for operations that require large amounts of data to be passed to or from the TPA7836B. In streaming mode multiple bytes of data can be written to or read from the TPA7836B without specifically providing instructions for each byte. Streaming mode is implemented by continually holding the CS pin active and continuing to shift new data in or old data out of the device.

The instruction phase includes the starting address. The TPA7836B device begins reading or writing data to this address and continues as long as the CS pin is asserted and single byte writes have not been enabled in the interface configuration 1 register (address 0x01). The TPA7836B device automatically increments or decrements the address depending on the setting of the address ascension bit in the interface configuration 0 register (address 0x00).

If the address is decrementing and address 0x0000 is reached, the next address used is 0x7FFF. If the address is incrementing and address 0x7FFF is reached, the next address used is 0x0000. Care should be taken when

writing to address 0x0000 and 0x0001 as writing to these addresses may change the configuration of the serial interface. Therefore address 0x0010 should be the first (ascending) or last (descending) address accessed in streaming mode.

Figure 62 and Figure 63 show the access protocol used in streaming mode.

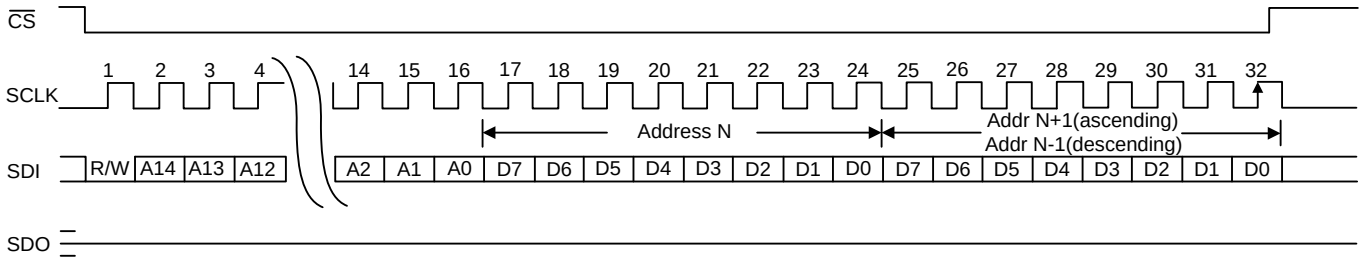


Figure 62. Serial Interface Streaming Write Example

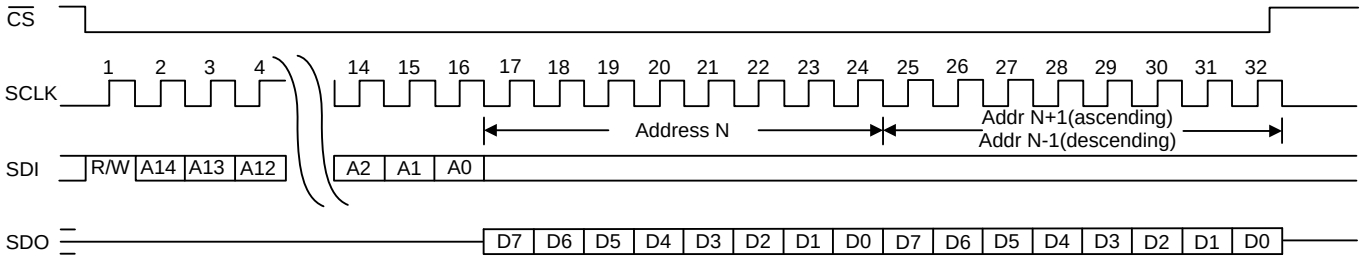


Figure 63. Serial Interface Streaming Read Example

7.6 Register Maps

Address	Type	Default	Register Name
0x00	R/W	30	Interface Configuration 0
0x01	R/W	00	Interface Configuration 1
0x02	R/W	03	Device Configuration
0x03	R	08	Chip Type
0x04	R	36	Chip ID (Low Byte)
0x05	R	0C	Chip ID (High Byte)
0x06	R	01	Chip Version
0x07 – 0x0B	—	—	Reserved
0x0C	R	51	Manufacturer ID (Low Byte)
0x0D	R	04	Manufacturer ID (High Byte)
0x0E	—	—	Reserved
0x0F	R/W	77	Register Update
0x10	R/W	00	ADC Configuration
0x11	R/W	70	False Alarm Configuration
0x12	R/W	00	GPIO Configuration
0x13	R/W	00	ADC MUX Configuration 0
0x14	R/W	00	ADC MUX Configuration 1
0x15	R/W	00	ADC MUX Configuration 2

0x16	—	—	Reserved
0x17	—	—	Reserved
0x18	R/W	00	DAC Clear Enable 0
0x19	R/W	00	DAC Clear Enable 1
0x1A	R/W	00	DAC Clear Source 0
0x1B	R/W	00	DAC Clear Source 1
0x1C	R/W	00	ALARMOUT Source0
0x1D	R/W	00	ALARMOUT Source1
0x1E	R/W	00	DAC Range 0
0x1F	R/W	00	DAC Range 1
0x20	R	00	ADC0-Data (Low Byte)
0x21	R	00	ADC0-Data (High Byte)
0x22	R	00	ADC1-Data (Low Byte)
0x23	R	00	ADC1-Data (High Byte)
0x24	R	00	ADC2-Data (Low Byte)
0x25	R	00	ADC2-Data (High Byte)
0x26	R	00	ADC3-Data (Low Byte)
0x27	R	00	ADC3-Data (High Byte)
0x28	R	00	ADC4-Data (Low Byte)
0x29	R	00	ADC4-Data (High Byte)
Address	**Type**	**Default**	**Register Name**
0x2A	R	00	ADC5-Data (Low Byte)
0x2B	R	00	ADC5-Data (High Byte)
0x2C	R	00	ADC6-Data (Low Byte)
0x2D	R	00	ADC6-Data (High Byte)
0x2E	R	00	ADC7-Data (Low Byte)
0x2F	R	00	ADC7-Data (High Byte)
0x30	R	00	ADC8-Data (Low Byte)
0x31	R	00	ADC8-Data (High Byte)
0x32	R	00	ADC9-Data (Low Byte)
0x33	R	00	ADC9-Data (High Byte)
0x34	R	00	ADC10-Data (Low Byte)
0x35	R	00	ADC10-Data (High Byte)
0x36	R	00	ADC11-Data (Low Byte)
0x37	R	00	ADC11-Data (High Byte)
0x38	R	00	ADC12-Data (Low Byte)
0x39	R	00	ADC12-Data (High Byte)
0x3A	R	00	ADC13-Data (Low Byte)
0x3B	R	00	ADC13-Data (High Byte)
0x3C	R	00	ADC14-Data (Low Byte)
0x3D	R	00	ADC14-Data (High Byte)
0x3E	R	00	ADC15-Data (Low Byte)
0x3F	R	00	ADC15-Data (High Byte)

0x40	R	00	ADC16-Data (Low Byte)
0x41	R	00	ADC16-Data (High Byte)
0x42	R	00	ADC17-Data (Low Byte)
0x43	R	00	ADC17-Data (High Byte)
0x44	R	00	ADC18-Data (Low Byte)
0x45	R	00	ADC18-Data (High Byte)
0x46	R	00	ADC19-Data (Low Byte)
0x47	R	00	ADC19-Data (High Byte)
0x48	R	00	ADC20-Data (Low Byte)
0x49	R	00	ADC20-Data (High Byte)
0x4A	R	00	Temperature Data (Low Byte)
0x4B	R	00	Temperature Data (High Byte)
0x4C-0x4F	—	—	Reserved
0x50	R/W	00	DACA0-Data (Low Byte)
0x51	R/W	00	DACA0-Data (High Byte)
0x52	R/W	00	DACA1-Data (Low Byte)
0x53	R/W	00	DACA1-Data (High Byte)
0x54	R/W	00	DACA2-Data (Low Byte)
0x55	R/W	00	DACA2-Data (High Byte)
0x56	R/W	00	DACA3-Data (Low Byte)
Address	**Type**	**Default**	**Register Name**
0x57	R/W	00	DACA3-Data (High Byte)
0x58	R/W	00	DACB4-Data (Low Byte)
0x59	R/W	00	DACB4-Data (High Byte)
0x5A	R/W	00	DACB5-Data (Low Byte)
0x5B	R/W	00	DACB5-Data (High Byte)
0x5C	R/W	00	DACB6-Data (Low Byte)
0x5D	R/W	00	DACB6-Data (High Byte)
0x5E	R/W	00	DACB7-Data (Low Byte)
0x5F	R/W	00	DACB7-Data (High Byte)
0x60	R/W	00	DACC8-Data (Low Byte)
0x61	R/W	00	DACC8-Data (High Byte)
0x62	R/W	00	DACC9-Data (Low Byte)
0x63	R/W	00	DACC9-Data (High Byte)
0x64	R/W	00	DACC10-Data (Low Byte)
0x65	R/W	00	DACC10-Data (High Byte)
0x66	R/W	00	DACC11-Data (Low Byte)
0x67	R/W	00	DACC11-Data (High Byte)
0x68	R/W	00	DACD12-Data (Low Byte)
0x69	R/W	00	DACD12-Data (High Byte)
0x6A	R/W	00	DACD13-Data (Low Byte)
0x6B	R/W	00	DACD13-Data (High Byte)
0x6C	R/W	00	DACD14-Data (Low Byte)

0x6D	R/W	00	DACD14-Data (High Byte)
0x6E	R/W	00	DACD15-Data (Low Byte)
0x6F	R/W	00	DACD15-Data (High Byte)
0x70	R	00	Alarm Status 0
0x71	R	00	Alarm Status 1
0x72	R	0C	General Status
0x73-0x79	—	—	Reserved
0x7A	R/W	FF	GPIO
0x7B-0x7F	—	—	Reserved
0x80	R/W	FF	ADC16-Upper-Thresh (Low Byte)
0x81	R/W	0F	ADC16-Upper-Thresh (High Byte)
0x82	R/W	00	ADC16-Lower-Thresh (Low Byte)
0x83	R/W	00	ADC16-Lower-Thresh (High Byte)
0x84	R/W	FF	ADC17-Upper-Thresh (Low Byte)
0x85	R/W	0F	ADC17-Upper-Thresh (High Byte)
0x86	R/W	00	ADC17-Lower-Thresh (Low Byte)
0x87	R/W	00	ADC17-Lower-Thresh (High Byte)
0x88	R/W	FF	ADC18-Upper-Thresh (Low Byte)
0x89	R/W	0F	ADC18-Upper-Thresh (High Byte)
0x8A	R/W	00	ADC18-Lower-Thresh (Low Byte)
Address	**Type**	**Default**	**Register Name**
0x8B	R/W	00	ADC18-Lower-Thresh (High Byte)
0x8C	R/W	FF	ADC19-Upper-Thresh (Low Byte)
0x8D	R/W	0F	ADC19-Upper-Thresh (High Byte)
0x8E	R/W	00	ADC19-Lower-Thresh (Low Byte)
0x8F	R/W	00	ADC19-Lower-Thresh (High Byte)
0x90	R/W	FF	ADC20-Upper-Thresh (Low Byte)
0x91	R/W	0F	ADC20-Upper-Thresh (High Byte)
0x92	R/W	00	ADC20-Lower-Thresh (Low Byte)
0x93	R/W	00	ADC20-Lower-Thresh (High Byte)
0x94	R/W	FF	LT-Upper-Thresh (Low Byte)
0x95	R/W	04	LT-Upper-Thresh (High Byte)
0x96	R/W	00	LT-Lower-Thresh (Low Byte)
0x97	R/W	0B	LT-Lower-Thresh (High Byte)
0x98-09F	—	—	Reserved
0xA0	R/W	08	ADC16-Hysteresis
0xA1	R/W	08	ADC17-Hysteresis
0xA2	R/W	08	ADC18-Hysteresis
0xA3	R/W	08	ADC19-Hysteresis
0xA4	R/W	08	ADC20-Hysteresis
0xA5	R/W	08	LT-Hysteresis
0xA6 - 0xAF	—	—	Reserved
0xB0	R/W	00	DAC Clear 0

0xB1	R/W	00	DAC Clear 1
0xB2	R/W	00	Power-Down 0
0xB3	R/W	00	Power-Down 1
0xB4	R/W	00	Power-Down 2
0xB5 - 0xBF	—	—	Reserved
0xC0	R/W	00	ADC Trigger

Interface Configuration: Address 0x00 – 0x02

Interface Configuration 0 Register (address = 0x00) [reset = 0x30]

Interface Configuration 0 (Interface Config 0) Register (R/W)

7	6	5	4	3	2	1	0
SOFT-RESET	Reserved	ADDR-ASCEND	Reserved	Reserved			
R/W-0	R/W-0	R/W-1	R/W-1	R/W-All zeros			

Interface Config 0 Register Field Descriptions (R/W)

Bit	Field	Type	Reset	Description
7	SOFT-RESET	R/W	0	Soft reset (self-clearing) 0:no action 1:reset – resets everything except address 0x00, 0x01
6	Reserved	R/W	0	Reserved for factory use
5	ADDR-ASCEND	R/W	1	Address Ascend 0: Descend – decrements address while streaming (address wrap from 0x0000 to 0x7FFF) 1: Ascend – increments address while streaming (address wrap from 0x7FFF to 0x0000)
4	Reserved	R/W	1	Reserved for factory use
3-0	Reserved	R/W	All zeros	Reserved for factory use

Interface Configuration 1 Register (address = 0x01) [reset = 0x00]

Interface Configuration 1 (Interface Config 1) Register (R/W)

7	6	5	4	3	2	1	0
SINGLE-INSTR	Reserved	READBACK	Reserved				
R/W-0	R/W-0	R/W-0	R/W-All zeros				

Interface Config 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SINGLE-INSTR	R/W	0	Single instruction enable 0: streaming mode (default) 1: single instruction
6	Reserved	R/W	0	Reserved for factory use
5	READBACK	R/W	0	Read back

				0: DAC read back from active registers (default) 1: DAC read back from buffer registers
4-0	Reserved	R/W	All zeros	Reserved for factory use

Device Configuration Register (address = 0x02) [reset = 0x03]

Device Configuration (Device Config) Register (R/W)

7	6	5	4	3	2	1	0
Reserved						POWER-MODE	
R/W-All Zeros						R/W-11	

Device Config Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R/W	All zeros	Reserved for factory use
1-0	POWER-MODE	R/W	11	Mode: 00: Normal operation – full power and full performance 11: Power Down – lowest power, non-operational except SPI One time overwrite of the power-down registers (0xB2, 0xB3 and 0xB4) For normal operation, 0xB2, 0xB3 and 0xB4 need to be set to power up corresponding functions.

Device Identification: Address 0x03 – 0x0D

Chip Type Register (address = 0x03) [reset = 0x08]

Chip Type Register (R)

7	6	5	4	3	2	1	0
Reserved				CHIP-TYPE			
R-0x0				R-0x8			

Chip Type Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R	0x0	Reserved for factory use
3-0	CHIP-TYPE	R	0x8	Identifies the device as a precision analog monitor and control

Chip ID Low Byte Register (address = 0x04) [reset = 0x36]

Chip ID Low Byte Register (R)

7	6	5	4	3	2	1	0
CHIPID-LOW							
R-0x36							

Chip ID Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CHIPID-LOW	R	0x36	Chip ID. Low byte

Chip ID High Byte Register (address = 0x05) [reset = 0x0C]

Chip ID High Byte Register (R)

7	6	5	4	3	2	1	0
CHIPID-HIGH							
R-0x0C							

Chip ID High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CHIPID-HIGH	R	0x0C	Chip ID. High byte

Version ID Register (address = 0x06) [reset = 0x01]

Version ID Register (R)

7	6	5	4	3	2	1	0
VERSIONID							
R-0x00							

Version ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VERSIONID	R	0x01	TPA7836B version ID. Subject to change

Manufacturer ID Low Byte Register (address = 0x0C) [reset = 0x51]

Manufacturer ID Low Byte Register (R)

7	6	5	4	3	2	1	0
VENDORID-LOW							
R-0x51							

Manufacturer ID Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VENDORID-LOW	R	0x51	Manufacturer ID. Low byte

Manufacturer ID High Byte Register (address = 0x0D) [reset = 0x04]

Manufacturer ID High Byte Register

7	6	5	4	3	2	1	0
VENDORID-HIGH							
R-0x04							

Manufacturer ID High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VENDORID-HIGH	R	0x04	Manufacturer ID. High byte

Register Update (Buffered Registers): Address 0x0F

Register Update Register (address = 0x0F) [reset = 0x77]

Register Update Register (Self Clearing) [R/W]

7	6	5	4	3	2	1	0
Reserved			ADC-UPDATE	Reserved			UPDATE
R/W-All Zeros			R/W-0	R/W-All Zeros			R/W-0

Register Update Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	All zeros	Reserved for factory use

4	ADC-UPDATE	R/W	0	When set transfers the latest ADC and temperature conversion data to the ADC and Temperature Data registers. This function is needed when operating the ADC in auto-cycle mode
3-1	Reserved	R/W	All zeros	Reserved for factory use
0	DAC-UPDATE	R/W	0	DAC update (self-clearing) 0: disabled 1: enabled – transfers data from buffers to active registers (DAC registers only)

General Device Configuration: Address 0x10 through 0x17

ADC Configuration Register (address = 0x10) [reset = 0x00]

ADC Configuration Register (R/W)

7	6	5	4	3	2	1	0
CMODE	CONV-RATE[1:0]		ADC-REF-BUFF	Reserved			
R/W-0	R/W-00		R/W-0	R/W-All Zeros			

ADC Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CMODE	R/W	0	ADC Conversion Mode Bit. This bit selects the ADC conversion mode. 0: Direct mode. The analog inputs specified in the ADC channel registers are converted sequentially one time. When one set of conversions is complete, the ADC is idle and waits for a new trigger. 1: Auto mode. The analog inputs specified in the channel registers are converted sequentially and repeatedly. When one set of conversions is complete, the ADC multiplexer returns to the first channel and repeats the process. The ADC-UPDATE bit in register 0x0F must be used to initiate the transfer of the latest conversion data to the ADC Data registers.
6-5	CONV-RATE[1:0]	R/W	00	ADC Conversion rate. See Table XX to configure this setting
4	ADC-REF-BUFF	R/W	0	ADC Reference Buffer bit. This bit must be set to 1 after device power-up to enable the internal reference buffer driving the ADC. 0: ADC reference buffer is disabled. 1: ADC reference buffer is enabled
3-0	Reserved	R/W	All Zeros	Reserved for factory use

ADC Sample time is related with selected channel

Table xx CONV-RATE[1:0] Bit Configuration

CONV-RATE[1:0]	ADC Channel Sample Time (μs) (no matter

	unipolar or bipolar channel, N is selected channel number, temperature channel is not included)
00	N*15.5+(21-N)*0.5
01	N*30+(21-N)*0.5
10	N*45+(21-N)*0.5
11	N*87+(21-N)*0.5

False Alarm Configuration Register (address = 0x11) [reset = 0x70]

False Alarm Configuration Register (R/W)

7	6	5	4	3	2	1	0
CH-FALR-CT[2:0]			TEMP-FALR-CT[1:0]		Reserved		
R/W-011			R/W–10		R/W-All zeros		

False Alarm Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	CH-FALR-CT[2:0]	R/W	011	False alarm protection for ADC channels. See Table 22 to Configure this bit.
4-3	TEMP-FALR-CT[1:0]	R/W	10	False alarm protection for temperature sensor. See Table 23 to configure this bit.
2-0	Reserved	R/W	All zeros	Reserved for factory use

Table 22. CH-FALR-CT Bit Configuration

CH-FALR-CT	N Consecutive Samples Before Alarm is Set
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

Table 23. TEMP-FALR-CT Bit Configuration

TEMP-FALR-CT	N Consecutive Samples Before Alarm is Set
00	1
01	2
10	4
11	8

GPIO Configuration Register (address = 0x12) [reset = 0x00]

GPIO Configuration Register (R/W)

7	6	5	4	3	2	1	0
Reserved				EN-DAV	EN-ADCTRIG	EN-ALARMOUT	EN-ALARMIN
R/W-All zeros				R/W-0	R/W-0	R/W-0	R/W-0

GPIO Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R/W	All zeros	Reserved for factory use
3	EN-DAV	R/W	0	$\overline{DAV}$ pin enable 0:GPIO3 operation (default) 1:$\overline{DAV}$ operation
2	EN-ADCTRIG	R/W	0	$\overline{ADCTRIG}$ pin enable 0: GPIO2 operation (default) 1: $\overline{ADCTRIG}$ operation
1	EN-ALARMOUT	R/W	0	$\overline{ALARMOUT}$ pin enable 0: GPIO1 operation (default) 1: $\overline{ALARMOUT}$ operation
0	EN-ALARMIN	R/W	0	$\overline{ALARMIN}$ pin enable 0: GPIO0 operation (default) 1: $\overline{ALARMIN}$ operation

ADC MUX Configuration 0 Register (address = 0x13) [reset = 0x00]

ADC MUX Configuration 0 Register (R/W)

7	6	5	4	3	2	1	0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

ADC MUX Configuration 0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH7	R/W	0	When set to 1 the corresponding analog input channel ADC_n is accessed during an ADC conversion cycle. When cleared to 0 the corresponding analog input channel ADC_n is ignored during an ADC conversion cycle. Suggest to change the register when ADC is in Idle mode.
6	CH6	R/W	0	
5	CH5	R/W	0	
4	CH4	R/W	0	
3	CH3	R/W	0	
2	CH2	R/W	0	
1	CH1	R/W	0	
0	CH0	R/W	0	

ADC MUX Configuration 1 Register (address = 0x14) [reset = 0x00]

ADC MUX Configuration 1 Register (R/W)

7	6	5	4	3	2	1	0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

ADC MUX Configuration 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH15	R/W	0	When set to 1 the corresponding analog input channel ADC_n is accessed during an ADC conversion cycle. When cleared to 0 the corresponding analog input channel ADC_n is ignored during an ADC conversion cycle. Suggest to change the register when ADC is in Idle
6	CH14	R/W	0	
5	CH13	R/W	0	
4	CH12	R/W	0	
3	CH11	R/W	0	
2	CH10	R/W	0	
1	CH9	R/W	0	

0	CH8	R/W	0	mode.

ADC MUX Configuration 2 Register (address = 0x15) [reset = 0x00]

ADC MUX Configuration 2 Register (R/W)

7	6	5	4	3	2	1	0
Reserved		TEMP-CH	CH20	CH19	CH18	CH17	CH16
R/W-All Zeros		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

ADC MUX Configuration 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	All Zeros	Reserved for factory use
5	TEMP-CH	R/W	0	When set to 1 the local temperature sensor is enabled for ADC conversion. When cleared to 0 the local temperature sensor is ignored
4	CH20	R/W	0	When set to 1 the corresponding analog input channel ADC_n is accessed during an ADC conversion cycle. When cleared to 0 the corresponding input channel ADC_n is ignored during an ADC conversion cycle. Suggest to change the register when ADC is in Idle mode.
3	CH19	R/W	0	
2	CH18	R/W	0	
1	CH17	R/W	0	
0	CH16	R/W	0	

DAC Clear Enable 0 Register (address = 0x18) [reset = 0x00]

DAC Clear Enable 0 Register (R/W)

7	6	5	4	3	2	1	0
CLREN-B7	CLREN-B6	CLREN-B5	CLREN-B4	CLREN-A3	CLREN-A2	CLREN-A1	CLREN-A0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

DAC Clear Enable 0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CLREN-B7	R/W	0	This register determines which DACs go into clear state when a clear event is detected as configured in the DAC-CLEAR5 SOURCE registers If CLRENn = 1, DAC_n is forced into a clear state with a clear event. If CLRENn = 0, a clear event does not affect the state of DAC_n.
6	CLREN-B6	R/W	0	
5	CLREN-B5	R/W	0	
4	CLREN-B4	R/W	0	
3	CLREN-A3	R/W	0	
2	CLREN-A2	R/W	0	
1	CLREN-A1	R/W	0	
0	CLREN-A0	R/W	0	

DAC Clear Enable 1 Register (address = 0x19) [reset = 0x00]

DAC Clear Enable 1 Register (R/W)

7	6	5	4	3	2	1	0
CLREN-D15	CLREN-D14	CLREN-D13	CLREN-D12	CLREN-C11	CLREN-C10	CLREN-C9	CLREN-C8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

DAC Clear Enable 1 Register Field Descriptions

Bit	Field	Type	Reset	
7	CLREN-D15	R/W	0	This register determines which DACs go into clear state

6	CLREN-D14	R/W	0	when a clear event is detected as configured in the DAC-CLEAR5 SOURCE registers If CLRENn = 1, DAC_n is forced into a clear state with a clear event. If CLRENn = 0, a clear event does not affect the state of DAC_n.
5	CLREN-D13	R/W	0	
4	CLREN-D12	R/W	0	
3	CLREN-C11	R/W	0	
2	CLREN-C10	R/W	0	
1	CLREN-C9	R/W	0	
0	CLREN-C8	R/W	0	

DAC Clear and ALARMOUT Source Select: Address 0x1A through 0x1D

DAC Clear Source 0 Register (address = 0x1A) [reset = 0x00]

DAC Clear Source 0 Register (R/W)

7	6	5	4	3	2	1	0
Reserved		ADC20-ALR-CLR	ADC19-ALR-CLR	ADC18-ALR-CLR	ADC17-ALR-CLR	ADC16-ALR-CLR	ADC15-ALR-CLR
R/W-All zeros		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

DAC Clear Source 0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	All zeros	This register selects which alarm forces DACs into a clear state, regardless of which DAC operation mode is active, auto or manual. In order for DAC_n to go into clear mode, it must be enabled in the DAC Clear Enable registers
5	ADC20-ALR-CLR	R/W	0	
4	ADC19-ALR-CLR	R/W	0	
3	ADC18-ALR-CLR	R/W	0	
2	ADC17-ALR-CLR	R/W	0	
1	ADC16-ALR-CLR	R/W	0	
0	ADC15-ALR-CLR	R/W	0	

DAC Clear Source 1 Register (address = 0x1B) [reset = 0x00]

DAC Clear Source 1 Register (R/W)

7	6	5	4	3	2	1	0
Reserved				ALARMIN-ALR	THERM-ALR	LT-HIGH-ALR	LT-LOW-ALR
R/W-All zeros				R/W-0	R/W-0	R/W-0	R/W-0

DAC Clear Source 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R/W	All zeros	Reserved for factory use
3	ALARMIN-ALR	R/W	0	This register selects which alarm forces DACs into a clear state regardless of which DAC operation mode is active, auto or manual. In order for DAC_n to go into clear mode, it must be enabled in the DAC Clear Enable registers
2	THERM-ALR	R/W	0	
1	LT-HIGH-ALR	R/W	0	
0	LT-LOW-ALR	R/W	0	

ALARMOUT Source 0 Register (address = 0x1c) [reset = 0x00]

ALARMOUT Source 0 Register (R/W)

7	6	5	4	3	2	1	0
Reserved			ADC20-ALR- OUT	ADC19-ALR- OUT	ADC18-ALR- OUT	ADC17-ALR- OUT	ADC16-ALR- OUT
R/W-All zeros			R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

ALARMOUT Source 0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	All zeros	Reserved for factory use
4	ADC20-ALR- OUT	R/W	0	This register selects which alarms can activate the $\overline{\text{ALARMOUT}}$ pin. The $\overline{\text{ALARMOUT}}$ must be enabled for this function to take effect.
3	ADC19-ALR- OUT	R/W	0	
2	ADC18-ALR- OUT	R/W	0	
1	ADC17-ALR- OUT	R/W	0	
0	ADC16-ALR- OUT	R/W	0	

ALARMOUT Source 1 Register (address = 0x1D) [reset = 0x00]

ALARMOUT Source 1 Register (R/W)

7	6	5	4	3	2	1	0
Reserved			ALARM-LATCH-DIS	LRIN-ALR-OUT	THERM-ALR- OUT	LT-HIGH-ALR- OUT	LT-LOW-ALR- OUT
R/W-All zeros			R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

ALARMOUT Source 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	All zeros	Reserved for factory use
4	ALARM-LATCH-DIS	R/W	0	Alarm latch disable bit. When cleared to 0 the alarm bits are latched. When an alarm occurs, the corresponding alarm bit is set to “1”. The alarm bit remains until the error condition subsides and the alarm register is read. Before reading, the alarm bit is not cleared even if the alarm condition disappears. When set to 1 the alarm bits are not latched. When the alarm condition subsides, the alarm bits are cleared regardless of whether the alarm bits have been read or not.
3	LRIN-ALR-OUT	R/W	0	This register selects which alarms can activate the $\overline{\text{ALARMOUT}}$ pin. The $\overline{\text{ALARMOUT}}$ must be enabled for this function to take effect.
2	THERM-ALR- OUT	R/W	0	
1	LT-HIGH-ALR- OUT	R/W	0	
0	LT-LOW-ALR- OUT	R/W	0	

DAC Range: Address 0x1E

DAC Range Register 0 (address = 0x1E) [reset = 0x00]

DAC Range 0 Register(R/W)

7	6	5	4	3	2	1	0
Reserved	DAC-RANGEB[2:0]			Reserved	DAC-RANGEA[2:0]		
R/W-0	R/W-All zeros			R/W-0	R/W-All zeros		

DAC Range 0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved for factory use

6-4	DAC-RANGEB[2:0]	R/W	All zeros	DAC group B output voltage selection. Overrides output range set by the auto-range detection circuit. See DAC-RANGEx Bit Configuration to configure this setting.
3	Reserved	R/W	0	Reserved for factory use
2-0	DAC-RANGEA[2:0]	R/W	All zeros	DAC group B output voltage selection. Overrides output range set by the auto-range detection circuit. See DAC-RANGEx Bit Configuration to configure this setting.

DAC-RANGEx Bit Configuration

DAC-RANGEx[2:0]	DAC Group x Output Voltage Range
0xx	Range set by auto-range detection circuit
100	–10 to 0 V
101	-5 to 0 V
110	0 to 10 V
111	0 to 5 V

DAC Range 1 Register (address = 0x1F) [reset = 0x00]

DAC Range 1 Register (R/W)

7	6	5	4	3	2	1	0
Reserved	DAC-RANGEB[2:0]			Reserved	DAC-RANGEA[2:0]		
R/W-0	R/W-All zeros			R/W-0	R/W-All zeros		

DAC Range 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved for factory use
6-4	DAC-RANGEB[2:0]	R/W	All zeros	DAC group D output voltage selection. Overrides output range set by the auto-range detection circuit. See DAC-RANGEx Bit Configuration to configure this setting.
3	Reserved	R/W	0	Reserved for factory use
2-0	DAC-RANGEA[2:0]	R/W	All zeros	DAC group C output voltage selection. Overrides output range set by the auto-range detection circuit. See DAC-RANGEx Bit Configuration to configure this setting.

ADC and Temperature Data: Address 0x20 through 0x4B

ADCn-Data (Low Byte) Register (address = 0x20 through 0x49) [reset = 0x00]

ADCn-Data (Low Byte) Register (R)

7	6	5	4	3	2	1	0
ADCn-DATA(7:0)							
R- Maybe random data after POR, and will be correct after ADC conversion is done.							

ADCn-Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Reset	Description

7-0	ADCn-DATA(7:0)	R	Random	Stores the 12-bit ADC_n conversion results in straight binary format for both types of inputs channels (unipolar and bipolar)

ADCn-Data (High Byte) Register (address = 0x20 through 0x49) [reset = 0x00]

ADCn-Data (High Byte) Register (R)

7	6	5	4	3	2	1	0
Reserved				ADCn-DATA (11:8)			
R- Maybe random data after POR				R- Maybe random data after POR			

ADCn-Data (High Byte) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R	Random	Reserved for factory use
3-0	ADCn-DATA (11:8)	R	Random	Stores the 12-bit ADC_n conversion results in straight binary format for both types of inputs channels (unipolar and bipolar).

Temperature Data (Low Byte) Register (address = 0x4A) [reset = 0x00]

Temperature Data (Low Byte) Register (R)

7	6	5	4	3	2	1	0
TEMP-DATA(7:0)							
R- Maybe random data after POR, and will be correct after ADC conversion is done.							

Temperature Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TEMP-DATA(7:0)	R	Random	Stores the temperature sensor reading in twos complement format

Temperature Data (High Byte) Register (address = 0x4B) [reset = 0x00]

Temperature Data (High Byte) Register (R)

7	6	5	4	3	2	1	0
Reserved				ADCn-DATA (11:8)			
R-Random				R-Random			

Temperature Data (High Byte) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R	Random	Reserved for factory use
3-0	TEMP-DATA(11:8)	R	Random	Stores the temperature sensor reading in twos complement format

DAC Data: Address 0x50 through 0x6F

DACn-Data (Low Byte) Register (address = 0x50 through 0x6F) [reset = 0x00]

DACn-Data (Low Byte) Register (R/W)

7	6	5	4	3	2	1	0
DACn-DATA (7:0)							
R/W-All zeros							

DACn-Data (Low Byte) Register Field Descriptions

Bit	Field	Type	Reset	Description

7-0	DACn-DATA (7:0)	R/W	All zeros	Stores the 12-bit data to be loaded to the DAC_n latches in straight binary format. The straight binary format is used for all DAC ranges

DACn Data (High Byte) Register (address = 0x50 through 0x6F) [reset = 0x00]

DACn Data (High Byte) Register (R/W)

7	6	5	4	3	2	1	0
Reserved				DACn-DATA (11:8)			
R-All zeros				R/W-All zeros			

DACn Data (High Byte) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R/W	All zeros	Reserved for factory use Suggest to ignore read back value since it is not useful.
3-0	DACn-DATA (11:8)	R/W	All zeros	Stores the 12-bit data to be loaded to the DAC_n latches in straight binary format. The straight binary format is used for all DAC ranges

Status Registers: Address 0x70 through 0x72

The TPA7836B device continuously monitors all general purpose analog inputs and local temperature sensor during normal operation. When any input is out of the specified range N consecutive times, the corresponding alarm bit is set (1). If the input returns to the normal range before N consecutive times, the corresponding alarm bit remains clear (0). This configuration avoids any false alarms. When an alarm status occurs, the corresponding alarm bit is set (1). When the corresponding bit in the $\overline{\text{ALARMOUT}}$ Source Registers is cleared (0), the $\overline{\text{ALARMOUT}}$ pin is latched.

Whenever an alarm status bit is set, it remains set until the event that caused it is resolved and its status register is read. Reading the Alarm Status Registers clears the alarm status bits. The alarm bit can only be cleared by reading its Alarm Status register after the event is resolved, or by hardware reset, software reset, or power-on reset. All alarm status bits are cleared when reading the Alarm Status registers, and all these bits are reasserted if the out-of-limit condition still exists after the next conversion cycle, unless otherwise noted

Alarm Status 0 Register (address = 0x70) [reset = 0x00]

Alarm Status 0 Register (R)

7	6	5	4	3	2	1	0
Reserved			ADC20-ALR	ADC19-ALR	ADC18-ALR	ADC17-ALR	ADC16-ALR
R-All zeros			R-0	R-0	R-0	R-0	R-0

Alarm Status 0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R	0	Reserved for factory use
4	ADC20-ALR	R	0	ADC20-ALR = 1 when ADC20 is out of the range defined by the corresponding threshold registers ADC20-ALR = 0 when the analog input is not out of the specified range
3	ADC19-ALR	R	0	ADC19-ALR = 1 when ADC19 is out of the range defined by the corresponding threshold registers ADC19-ALR = 0 when the analog input is not out of the specified range
2	ADC18-ALR	R	0	ADC18-ALR = 1 when ADC18 is out of the range defined by the corresponding threshold registers ADC18-ALR = 0 when the analog input is not out of the specified range

1	ADC17-ALR	R	0	ADC17-ALR = 1 when ADC17 is out of the range defined by the corresponding threshold registers ADC17-ALR = 0 when the analog input is not out of the specified range
0	ADC16-ALR	R	0	ADC16-ALR = 1 when ADC16 is out of the range defined by the corresponding threshold registers ADC16-ALR = 0 when the analog input is not out of the specified range

Alarm Status 1 Register (address = 0x71) [reset = 0x00]

Alarm Status 1 Register (R)

7	6	5	4	3	2	1	0
Reserved				ALARMIN-ALR	THERM-ALR	LT-HIGH-ALR	LT-LOW-ALR
R-All zeros				R-0	R-0	R-0	R-0

Alarm Status 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R	All zeros	Reserved for factory use
3	ALARMIN-ALR	R	0	The ALARMIN-ALR is set to 1 if the $\overline{\text{ALARMIN}}$ pin is enabled and set high.
2	THERM-ALR	R	0	Thermal alarm flag. When the die temperature is equal to or greater than +150°C, the bit is set (1) and the THERM-ALR flag activates. The on-chip temperature sensor (LT) monitors the die temperature. If LT is disabled, the THERM-ALR bit is always 0 The hysteresis of this alarm is 8°C.
1	LT-HIGH-ALR	R	0	LT-HIGH-ALR = 1 when the temperature sensor is out of the range defined by the upper threshold
0	LT-LOW-ALR	R	0	LT-LOW-ALR = 1 when the temperature sensor is out of the range defined by the lower threshold

General Status Register (address = 0x72) [reset = 0x0C]

General Status Register (R)

7	6	5	4	3	2	1	0
AVSSD	AVSSC	AVSSB	AVSSA	ADC_IDLE	Reserved	GALR	DAVF
—	—	—	—	R-1	R-1	R-0	R-0

General Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	AVSSD			This bit is the auto-range detection output for DAC group D. This bit is set to 1 when $AV_{SSD} < AV_{SSTH}$ (–10- to 0-V output range), and 0 when $AV_{SSD} > AV_{SSTH}$ (0- to 5-V output range).
6	AVSSC			This bit is the auto-range detection output for DAC group C. This bit is set to 1 when $AV_{SSC} < AV_{SSTH}$ (–10- to 0-V output range), and 0 when $AV_{SSC} > AV_{SSTH}$ (0- to 5-V output range).
5	AVSSB			This bit is the auto-range detection output for DAC group B. This bit is set to 1 when $AV_{SSB} < AV_{SSTH}$ (–10- to 0-V output range), and 0 when $AV_{SSB} > AV_{SSTH}$ (0- to 5-V output range).
4	AVSSA			This bit is the auto-range detection output for DAC group A. This bit is set to 1 when $AV_{EE} < AV_{SSTH}$ (–10- to 0-V output range), and 0 when $AV_{EE} > AV_{SSTH}$ (0- to 5-V output range).

3	ADC_IDLE	R	1	ADC Idle indicator. Auto mode: 1 by default; goes to 0 once the ADC is triggered and is running. Remains 0 until ADC is stopped, then ADC_IDLE returns to 1. Direct mode: 1 by default; goes to 0 once the ADC is triggered and direct conversions are running and returns to 1 when direct mode conversions are completed.
2	Reserved	R	1	Reserved for factory use
1	GALR	R	0	Global alarm bit. This bit is the OR function or all individual alarm bits of the status register. This bit is set to 1 when any alarm condition occurs and remains set until the status register is read. This bit is cleared after reading the Status Register
0	DAVF	R	0	ADC Data available flag bit. Direct mode only. Always cleared in Auto mode. 0: ADC conversion is in progress or ADC is in Auto mode 1: ADC conversions are complete and new data is available

GPIO: Address 0x7A

GPIO Register (address = 0x7A) [reset = 0xFF]

GPIO Register (R/W)

7	6	5	4	3	2	1	0
GPIO-7	GPIO-6	GPIO-5	GPIO-4	GPIO-3	GPIO-2	GPIO-1	GPIO-0
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

GPIO Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO-7	R/W	1	For write operation the GPIO pin operates as an output. Writing a 1 to the GPIO-n bit sets the GPIO-N pin to high impedance Writing a 0 sets the GPIO-n pin to logic low. For read operations the GPIO pin operates as an input. Read the GPIO-n bit to receive the status of the GPIO-n pin, The GPIO-n pin has 48-kΩ input impedance to IOV_{DD}
6	GPIO-6	R/W	1	
5	GPIO-5	R/W	1	
4	GPIO-4	R/W	1	
3	GPIO-3	R/W	1	
2	GPIO-2	R/W	1	
1	GPIO-1	R/W	1	
0	GPIO-0	R/W	1	

Out-Of-Range ADC Thresholds: Address 0x80 through 0x93

The unipolar analog inputs (LV_ADC16 to LV_ADC20) and the local temperature sensor implement an out-of range alarm function. The Upper-Thresh and Lower-Thresh registers define the upper bound and lower bounds for these inputs. This window determines whether the analog input or temperature is out-of-range. When the input is outside the window, the corresponding CH-ALR-n bit in the Status Register is set to 1. For normal operation, the value of the upper threshold must be greater than the value of lower threshold; otherwise, an alarm is always indicated. The analog input threshold values are specified in straight binary format while the local temperature ones are specified in two's complement format

ADCn-Upper-Thresh (Low Byte) Register (address = 0x80 through 0x93) [reset = 0xFF]

ADCn-Upper-Thresh (Low Byte) Register (R/W)

7	6	5	4	3	2	1	0
THRUn(7:0)							
R/W-All ones							

ADCn-Upper-Thresh (Low Byte) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRUn(7:0)	R/W	All ones	Sets 12-bit upper threshold value for the ADC_n channel in straight binary format.

ADCn-Upper-Thresh (High Byte) Register (address = 0x80 through 0x93) [reset = 0x0F]

ADCn-Upper-Thresh (High Byte) Register (R/W)

7	6	5	4	3	2	1	0
reserved				THRUn(11:8)			
R/W-All zeros				R/W-0xF			

ADCn-Upper-Thresh (High Byte) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R/W	All zeros	Reserved for factory use.
3-0	THRUn(11:8)	R/W	0xF	Sets 12-bit upper threshold value for the ADC_n channel in straight binary format.

ADCn-Lower-Thresh (Low Byte) Register (address = 0x80 through 0x93) [reset = 0x00]]

ADCn-Lower-Thresh (Low Byte) Register (R/W)

7	6	5	4	3	2	1	0
THRLn(7:0)							
R/W-All zeros							

ADCn-Lower-Thresh (Low Byte) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRLn(7:0)	R/W	All ones	Sets 12-bit lower threshold value for the ADC_n channel in straight binary format.

ADCn-Lower-Thresh (High Byte) Register (address = 0x80 through 0x93) [reset = 0x00]

ADCn-Lower-Thresh (High Byte) Register (R/W)

7	6	5	4	3	2	1	0
reserved				THRLn(11:8)			
R/W-All zeros				R/W-All zeros			

ADCn-Lower-Thresh (High Byte) Register Field Descriptions Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R/W	All zeros	Reserved for factory use.
3-0	THRLn(11:8)	R/W	All zeros	Sets 12-bit lower threshold value for the ADC_n channel in straight binary format.

LT-Upper-Thresh (Low Byte) Register (address = 0x94) [reset = 0xFF]

LT-Upper-Thresh (Low Byte) Register (R/W)

7	6	5	4	3	2	1	0
THRU-LT(7:0)							
R/W-All ones							

LT-Upper-Thresh (Low Byte) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRU-LT(7:0)	R/W	All ones	Sets 12-bit upper threshold value for the local temperature sensor in two's complement format

LT-Upper-Thresh (High Byte) Register (address = 0x95) [reset = 0x04]

LT-Upper-Thresh (High Byte) Register (R/W)

7	6	5	4	3	2	1	0

Reserved	THRU-LT(11:8)
R/W-All zeros	R/W-0x4

LT-Upper-Thresh (High Byte) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R/W	All zeros	Reserved for factory use.
3-0	THRU-LT(11:8)	R/W	0x4	Sets 12-bit upper threshold value for the local temperature sensor in two's complement format

LT-Lower-Thresh (Low Byte) Register (address = 0x96) [reset = 0x00]

LT-Lower-Thresh (Low Byte) Register (R/W)

7	6	5	4	3	2	1	0
THRL-LT(7:0)							
R/W- All zeros							

LT-Lower-Thresh (Low Byte) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRL-LT(7:0)	R/W	All zeros	Sets 12-bit lower threshold value for the local temperature sensor in two's complement format

LT-Lower-Thresh (High Byte) Register (address = 0x97) [reset = 0x0B]

LT-Lower-Thresh (High Byte) Register (R/W)

7	6	5	4	3	2	1	0
Reserved				THRL-LT(11:8)			
R/W-All zeros				R/W-0xB			

LT-Lower-Thresh (High Byte) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R/W	All zeros	Reserved for factory use.
3-0	THRL-LT(11:8)	R/W	0xB	Sets 12-bit lower threshold value for the local temperature sensor in two's complement format

Alarm Hysteresis Configuration: Address 0xA0 and 0xA5

The hysteresis registers define the hysteresis in the out-of-range alarms.

ADCn-Hysteresis Register (address = 0xA0 through 0xA4) [reset = 0x08]

ADCn-Hysteresis Register (R/W)

7	6	5	4	3	2	1	0
Reserved	HYSTn(6:0)						
R/W-0	R/W-0x08						

ADCn-Hysteresis Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved for factory use.
6-0	HYSTn(6:0)	R/W	0x08	Hysteresis of general purpose ADC_n, 1 LSB per step

LT-Hysteresis Register (address = 0xA5) [reset = 0x08]

LT-Hysteresis Register (R/W)

7	6	5	4	3	2	1	0
Reserved			HYST-LT(4:0)				
R/W-All zeros			R/W-0x08				

LT-Hysteresis Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	All zeros	Reserved for factory use
4-0	HYST-LT(4:0)	R/W	0x08	Hysteresis of local temperature sensor, 1°C per step. The range is 0°C to 31°C.

Clear and Power-Down Registers: Address 0xB0 through 0XB4

DAC Clear 0 Register (address = 0xB0) [reset = 0x00]

DAC Clear 0 Register (R/W)

7	6	5	4	3	2	1	0
CLR-B7	CLR-B6	CLR-B5	CLR-B4	CLR-A3	CLR-A2	CLR-A1	CLR-A0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

DAC Clear 0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CLR-B7	R/W	0	This register uses software to force the DAC into a clear state. If CLRn = 1, DAC_n is forced into a clear state. If CLRn = 0, DAC_n is restored to normal operation.
6	CLR-B6	R/W	0	
5	CLR-B5	R/W	0	
4	CLR-B4	R/W	0	
3	CLR-A3	R/W	0	
2	CLR-A2	R/W	0	
1	CLR-A1	R/W	0	
0	CLR-A0	R/W	0	

DAC Clear 1 Register (address = 0xB1) [reset = 0x00]

DAC Clear 1 Register (R/W)

7	6	5	4	3	2	1	0
CLR-D15	CLR-D14	CLR-D13	CLR-D12	CLR-C11	CLR-C10	CLR-C9	CLR-C8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

DAC Clear 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CLR-D15	R/W	0	This register uses software to force the DAC into a clear state. If CLRn = 1, DAC_n is forced into a clear state. If CLRn = 0, DAC_n is restored to normal operation.
6	CLR-D14	R/W	0	
5	CLR-D13	R/W	0	
4	CLR-D12	R/W	0	
3	CLR-C11	R/W	0	
2	CLR-C10	R/W	0	
1	CLR-C9	R/W	0	
0	CLR-C8	R/W	0	

Power-Down 0 Register (address = 0xB2) [reset = 0x00]

Power-Down 0 Register (R/W)

7	6	5	4	3	2	1	0
PDAC-B7	PDAC-B6	PDAC-B5	PDAC-B4	PDAC-A3	PDAC-A2	PDAC-A1	PDAC-A0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Power-Down 0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PDAC-B7	R/W	0	After power-on or reset, all bits in the power-down register are cleared to

6	PDAC-B6	R/W	0	0, and all the components controlled by this register are either powered-down or off. The power-down register allows the host to manage the TPA7836B power dissipation. When not required, any of the DACs can be put into clamp mode and the ADC and internal reference into an inactive low-power mode to reduce current drain from the supply. The bits in the power-down register control this power-down function. Set the respective bit to 1 to activate the corresponding function. Suggest to enable DAC after Reference is enabled (PREF=1).
5	PDAC-B5	R/W	0	
4	PDAC-B4	R/W	0	
3	PDAC-A3	R/W	0	
2	PDAC-A2	R/W	0	
1	PDAC-A1	R/W	0	
0	PDAC-A0	R/W	0	

Power-Down 1 Register (address = 0xB3) [reset = 0x00]

Power-Down 1 Register (R/W)

7	6	5	4	3	2	1	0
PDAC-D15	PDAC-D14	PDAC-D13	PDAC-D12	PDAC-C11	PDAC-C10	PDAC-C9	PDAC-C8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Power-Down 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PDAC-D15	R/W	0	After power-on or reset, all bits in the power-down register are cleared to 0, and all the components controlled by this register are either powered-down or off. The power-down register allows the host to manage the TPA7836B power dissipation. When not required, any of the DACs can be put into clamp mode and the ADC and internal reference into an inactive low-power mode to reduce current drain from the supply. The bits in the power-down register control this power-down function. Set the respective bit to 1 to activate the corresponding function. Suggest to enable DAC after Reference is enabled (PREF=1).
6	PDAC-D14	R/W	0	
5	PDAC-D13	R/W	0	
4	PDAC-D12	R/W	0	
3	PDAC-C11	R/W	0	
2	PDAC-C10	R/W	0	
1	PDAC-C9	R/W	0	
0	PDAC-C8	R/W	0	

Power-Down 2 Register (address = 0xB4) [reset = 0x00]

Power-Down 2 Register (R/W)

7	6	5	4	3	2	1	0
Reserved						PREF	PADC
R/W-All zeros						R/W-0	R/W-0

Power-Down 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R/W	All zeros	Reserved for factory use.
1	PREF	R/W	0	After power-on or reset, all bits in the power-down register are cleared to 0, and all the components controlled by this register are either powered-down or off. The power-down register allows the host to manage the TPA7836B power dissipation. When not required, any of the DACs can be put into clamp mode and the ADC and internal reference into an inactive low-power mode to reduce current drain from the supply. The bits in the power-down register control this power-down function. Set the respective bit to 1 to activate the corresponding function
0	PADC	R/W	0	

ADC Trigger: Address 0xC0

ADC Trigger Register (address = 0xC0) [reset = 0x00]

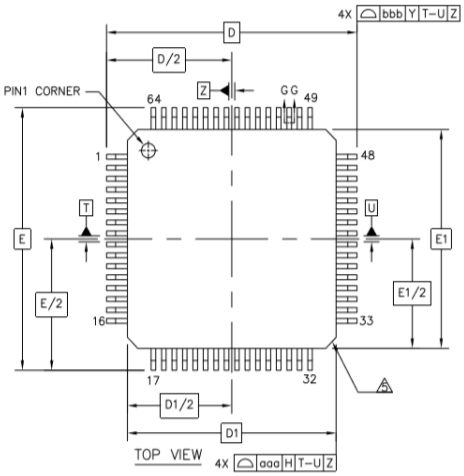
ADC Trigger Register (R/W)

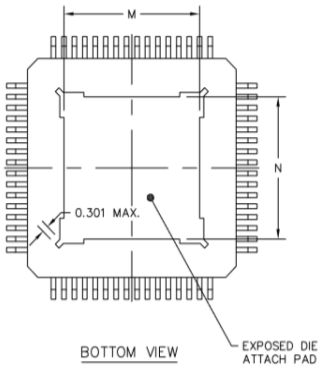
7	6	5	4	3	2	1	0
Reserved							ICONV
R/W-All zeros							R/W-0

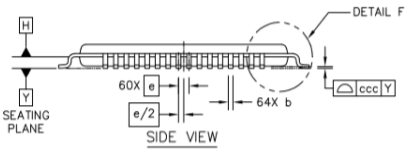
ADC Trigger Register Field Descriptions

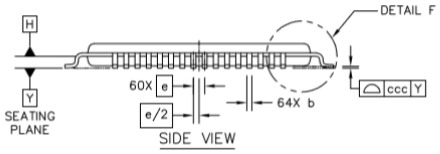
Bit	Field	Type	Reset	Description
7-1	Reserved	R/W	All zeros	Reserved for factory use
0	ICONV	R/W	0	Internal ADC conversion bit. Set this bit to 1 to start the ADC conversion internally. The bit is automatically cleared to 0 after the ADC conversion starts.

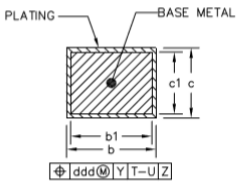
8 Mechanical, Packaging, and Orderable Information



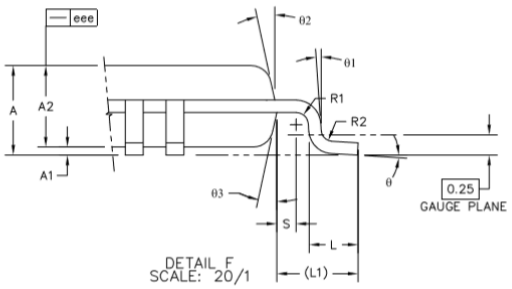








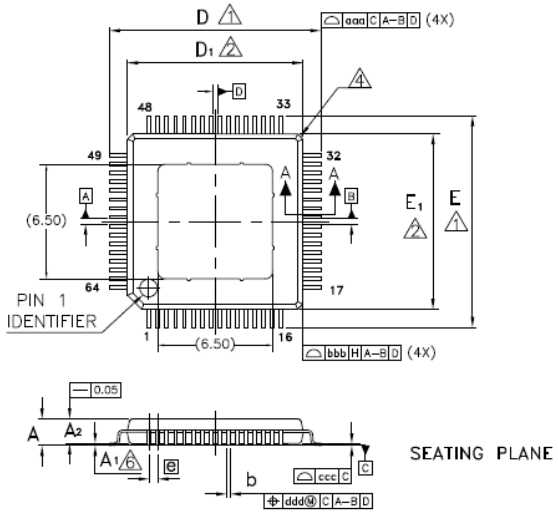
SECTION G-G
SCALE: 100/1

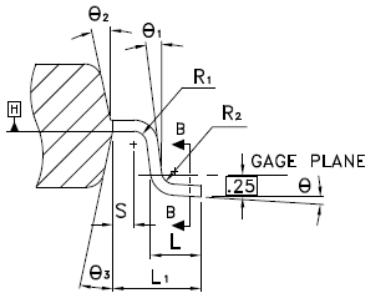


DETAIL F
SCALE: 20/1

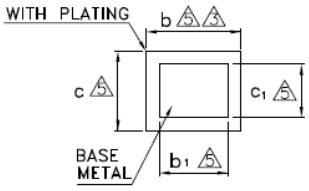
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.2
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	0.95	---	1.05
LEAD WIDTH(PLATING)		b	0.17	0.22	0.27
LEAD WIDTH		b1	0.17	0.2	0.23
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	12 BSC		
	Y	E	12 BSC		
	X	D1	10 BSC		
	Y	E1	10 BSC		
LEAD PITCH		e	0.5 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
EP SIZE	X	M	6.4	6.5	6.6
	Y	N	6.4	6.5	6.6
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.08		
MOLD FLATNESS		eee	0.05		

TQFP EP 64





SECTION A–A



SECTION B–B

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.20	—	—	0.047
A1	0.025	—	0.127	0.001	—	0.005
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	0.14	0.20	0.004	0.006	0.008
c1	0.09	0.12	0.16	0.004	0.005	0.006
D	11.85	12.00	12.15	0.467	0.472	0.478
D1	9.90	10.00	10.10	0.390	0.394	0.398
E	11.85	12.00	12.15	0.467	0.472	0.478
E1	9.90	10.00	10.10	0.390	0.394	0.398
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTE :

1. TO BE DETERMINED AT SEATING PLANE C .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS–026
9. SPECIAL CHARACTERISTICS C CLASS: ccc

Revision history:

Version	Date	Note
A.1	2020/12/15	
A.2	2020/01/12	Add second package POD, and revise mark.
A.3	2020/04/26	Add Typical Characteristics waveform.
A.4	2021/10/8	Correct inconsistent descriptions of 0x95 and 0x97 default value.
A.5	2021/11/18	Correct description of DAC registers, and add introduction of 0x02 register power mode registers to remind 0xB2~0xB4 operations.
A.6	2022/3/25	Update description of registers with 0x77 value.