36-V, 16-Bit, I2C Output Current, Voltage, and Power Monitor With Alert

Features

- Senses Bus Voltages from 0 V to 36 V
- High-Side or Low-Side Sensing
- Reports Current, Voltage, and Power
- High Accuracy
- Configurable Averaging Options
- 16 Programmable Addresses
- Operates from 2.7-V to 5.5-V Power Supply
- QFN3×3-16 Package

Applications

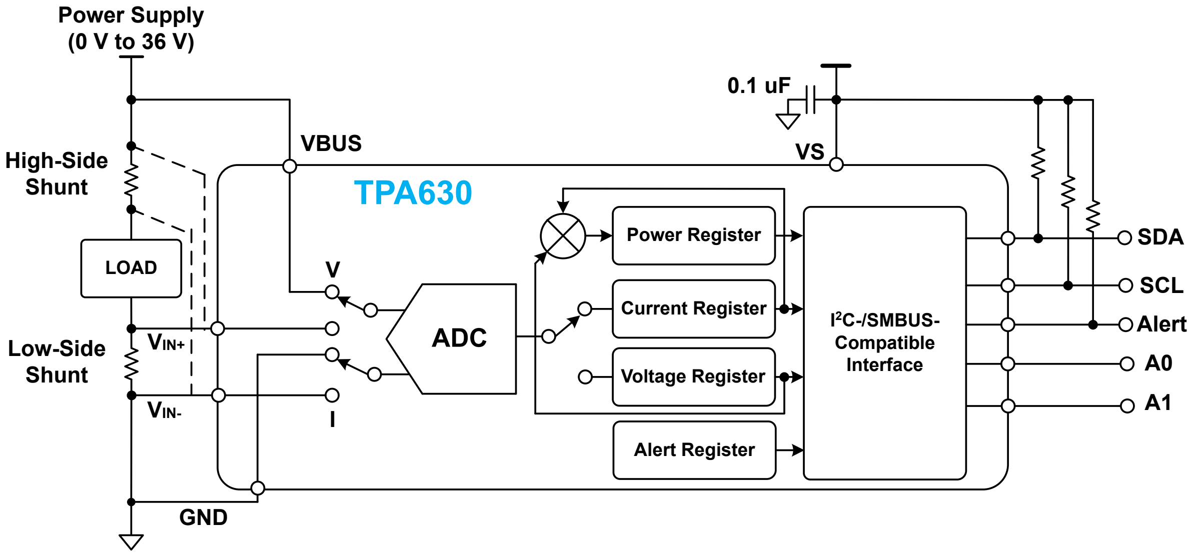
- Power management
- Servers
- Telecom Equipment
- Computing
- Test Equipment

Description

The TPA630 is an I^{2}C-compatible current-shunt and power monitor that supports 16 programmable addresses or an SMBUS-compatible interface. It measures both shunt voltage drop and bus supply voltage. With programmable calibration settings, conversion times, and averaging options—along with an integrated multiplier—the device provides direct readings of current in amperes and power in watts.

The TPA630 can accurately sense current across bus voltages ranging from 0 V to 36 V. It operates from a single 2.7 V to 5.5 V supply and typically consumes just 1.1 mA. The device is designed to operate over a temperature range of –40 °C to +125 °C.

Typical Application Circuit



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Revision History

Date	Revision	Notes
2026-01-08	Rev.A.0	Initial released version.

Pin Configuration and Functions

TPA630
QFN3×3-16
Top View

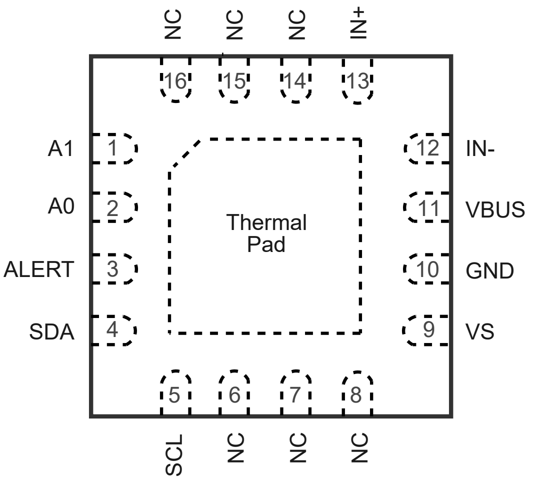


Table 1. Pin Functions

Pin No.	Name	I/O	Description
2	A0	Digital I	Address pin. Connect to GND, SCL, SDA, or VS. Table 3 shows pin settings and corresponding addresses.
1	A1	Digital I	Address pin. Connect to GND, SCL, SDA, or VS. Table 3 shows pin settings and corresponding addresses.
3	Alert	Digital O	Multi-functional alert, open-drain output.
10	GND	Analog	Ground.
6,7,8,14,15, 16	NC	—	No internal connection.
5	SCL	Digital I	Serial bus clock line, open-drain input.
4	SDA	Digital I/O	Serial bus data line, open-drain input/output.
9	VS	Analog I	Power supply, 2.7 V to 5.5 V.
11	VBUS	Analog I	Bus voltage input.
12	IN−	Analog I	Input for Negative Differential Shunt Voltage. This input measures the voltage across a current sense resistor. In a high-side configuration, it should be connected to the load side of the resistor. In a low-side configuration, connect it to the ground-referenced side.
13	IN+	Analog I	Input for Positive Differential Shunt Voltage. This input, along with the negative input, measures the voltage across a sense resistor. For high-side configurations, connect it to the bus voltage side. For low-side configurations, it should be connected to the load side

Pin No.	Name	I/O	Description
—	Thermal Pad	—	This pad can be connected to ground or left floating.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{VS}	Supply Voltage		6	V
Analog Inputs, IN+, IN–	Differential Mode (V_{IN+} − $V_{IN–}$) (2)	−40	40	V
	Common Mode (V_{IN+} + $V_{IN–}$) / 2	−0.3	40	V
V_{VBUS}		−0.3	40	V
V_{SDA}		GND − 0.3	6	V
V_{SCL}		GND − 0.3	V_{VS} + 0.3	V
I_{IN}	Input Current into any Pin		5	mA
I_{OUT}	Open-Drain Digital Output Current		10	mA
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) IN+ and IN− may have a differential voltage between −40 V and 40 V. However, the voltage at these pins must not exceed the range from −0.3 V to 40 V.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JESD22-C101 (2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_{CM}	Common-Mode Input Voltage		12		V
V_{VS}	Operating Supply Voltage		3.3		V
T_A	Operating Free-Air Temperature	−40		125	℃

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
QFN3×3-16	56	47	°C/W

Electrical Characteristics

All test conditions: V_{VS} = 3.3 V, T_A = 25°C, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} − V_{IN-}) = 0 mV, V_{VBUS} = 12 V, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input						
	Shunt Voltage Input Range		−81.9175		81.92	mV
	Bus Voltage Input Range (1)		0		36	V
CMRR	Common-Mode Rejection	0 V ≤ V_{IN+} ≤ 36 V	120	140		dB
V_{OS}	Shunt Offset Voltage, RTI (2)			±2.5	±30	µV
	Shunt Offset Voltage, RTI (2) vs. Temperature	−40°C ≤ T_A ≤ 125°C		0.15		µV/°C
PSRR	Shunt Offset Voltage, RTI (2) vs. Power Supply	2.7 V ≤ V_S ≤ 5.5 V		5		µV/V
V_{OS}	Bus Offset Voltage, RTI (2)			±10	±20	mV
	Bus Offset Voltage, RTI (2) vs. Temperature	−40°C ≤ T_A ≤ 125°C		60		µV/°C
PSRR	Bus Offset Voltage, RTI (2) vs. Power Supply			1		mV/V
I_B	Input Bias Current				10	µA
	VBUS Input Impedance			830		kΩ
	Input Leakage (3)	(IN+) + (IN−), Power-down Mode		1		µA
DC Accuracy						
	ADC Native Resolution			16		Bits
	1-LSB Step Size	Shunt Voltage		2.5		µV
		Bus Voltage		1.25		mV
	Shunt Voltage Gain Error			0.02	0.4	%FSR
	Shunt Voltage Gain Error vs. Temperature	−40°C ≤ T_A ≤ 125°C		50		ppm/°C
	Shunt Voltage Linearity				0.5%	
	Bus Voltage Gain Error			0.02	0.4	%FSR
	Bus Voltage Gain Error vs. Temperature	−40°C ≤ T_A ≤ 125°C		50		ppm/°C
	Bus Voltage Linearity				0.5%	
t_{CT}	ADC Conversion Time	CT bit = 000		66		µs
		CT bit = 001		134		µs
		CT bit = 010		269		µs
		CT bit = 011		542		µs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		CT bit = 100		1085		µs
		CT bit = 101		2170		µs
		CT bit = 110		4341		µs
		CT bit = 111		8682		µs
SMBus						
	SMBus Timeout (4)			28		ms
Digital Input/Output						
	Input Capacitance			3		pF
	Leakage Input Current	0 V ≤ V_{SCL} ≤ V_{VS}		0.1		µA
		0 V ≤ V_{SDA} ≤ V_{VS}		0.1		µA
		0 V ≤ V_{Alert} ≤ V_{VS}		0.1		µA
		0 V ≤ V_{A0} ≤ V_{VS}		0.1		µA
		0 V ≤ V_{A1} ≤ V_{VS}		0.1		µA
V_{IH}	High-Level Input Voltage		0.7 × V_{VS}			V
V_{IL}	Low-Level Input Voltage				0.3 × V_{VS}	V
V_{OL}	Low-Level Output Voltage, SDA, Alert		0		0.4	V
	Hysteresis			150		mV
Power Supply						
	Operating Supply Range		2.7		5.5	V
I_Q	Quiescent Current			1100		µA
	Quiescent Current, Power-down (Shutdown) Mode			8		µA
V_{POR}	Power-on Reset Threshold			2.2		V

(1) While the input range is 36 V, the full-scale range of the ADC scaling is 40.96 V.

(2) RTI = referred-to-input.

(3) The input leakage is positive (current flowing into the pin) for the conditions shown at the top of this table. Negative leakage currents can occur under different input conditions.

(4) The SMBus timeout in the TPA630 resets the interface any time SCL is low for more than 28 ms.

(5) Test Levels:

1. Tested at the final test. Over-temperature limits are set by characterization and simulation.
2. Set by characterization and simulation.
3. Typical value only for information, provided by design simulation.

Typical Performance Characteristics

All test conditions: V_{VS} = 3.3 V, T_A = 25°C, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} − V_{IN-}) = 0 mV, V_{VBUS} = 12 V, unless otherwise noted.

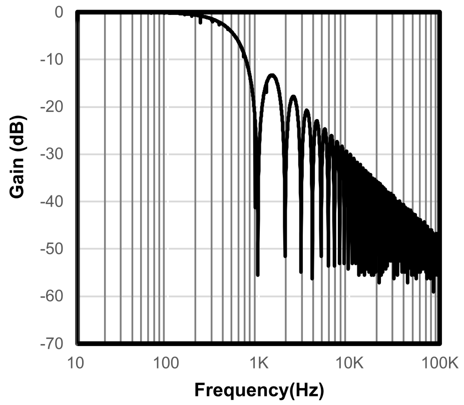


Figure 1. Frequency Response

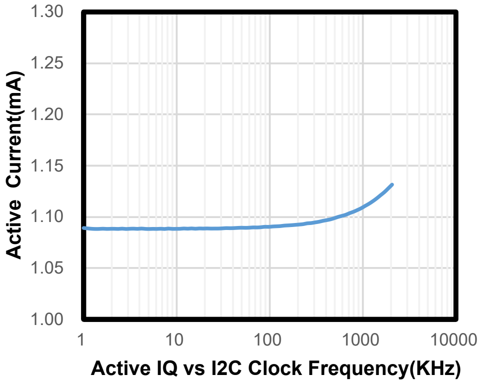


Figure 2. Active IQ vs. I^2C Clock Frequency

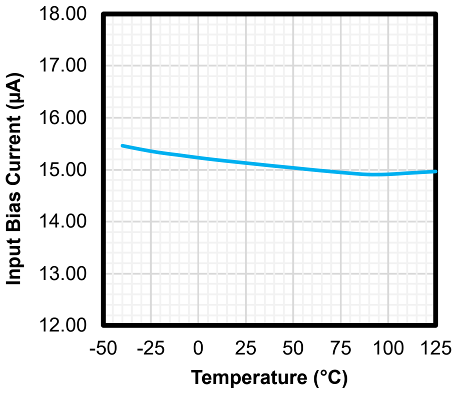


Figure 3. Input Bias Current vs. Temperature

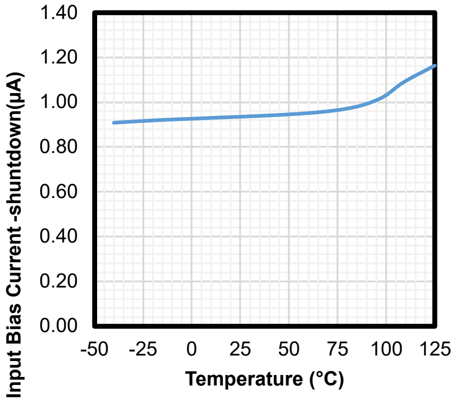


Figure 4. Input Bias Current (Shutdown) vs. Temperature

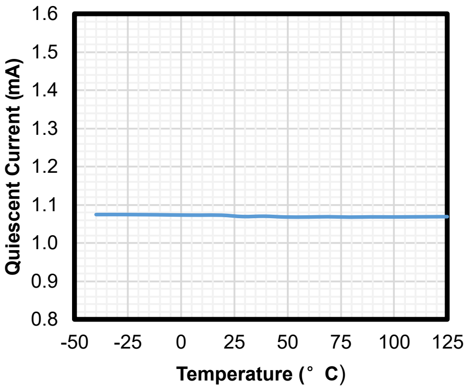


Figure 5. Quiescent Current vs. Temperature

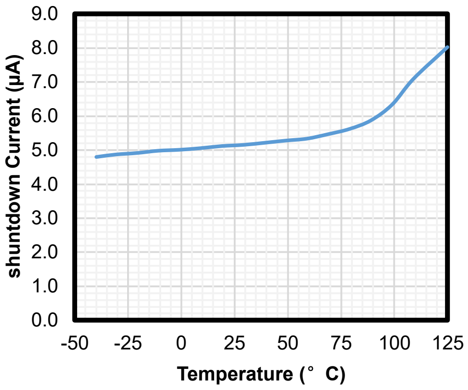


Figure 6. Shutdown Current vs. Temperature

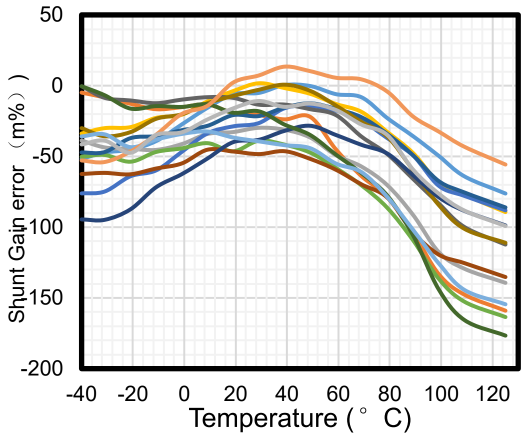


Figure 7. ADC Shunt Gain Error vs. Temperature

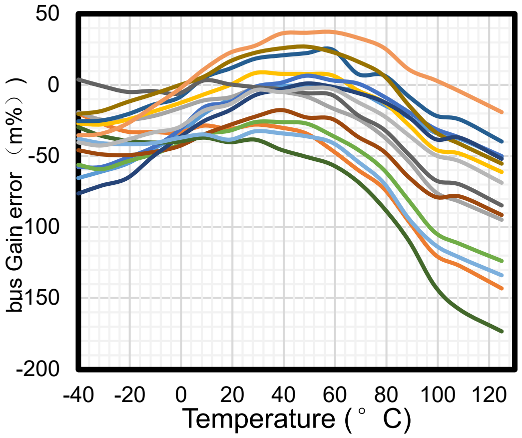


Figure 8. ADC Bus Gain Error vs. Temperature

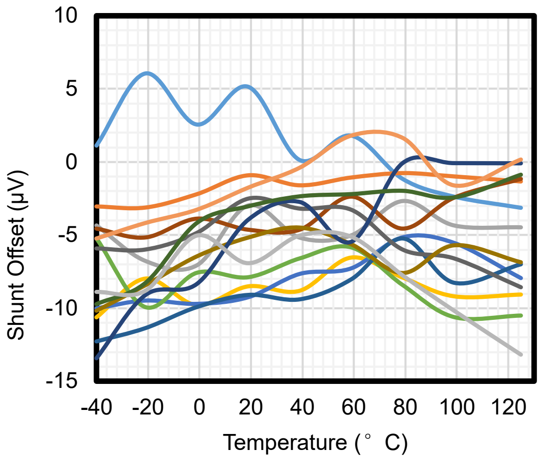


Figure 9. ADC Shunt Offset vs. Temperature

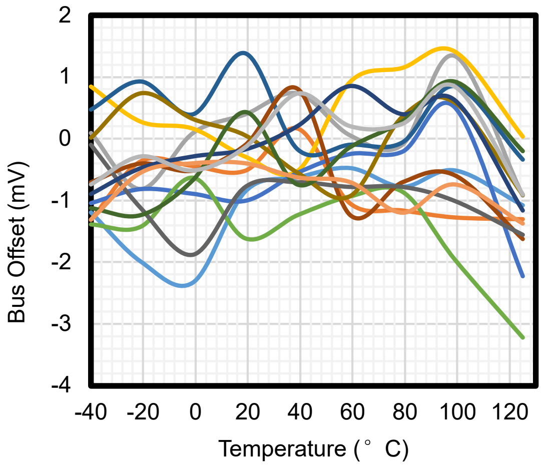


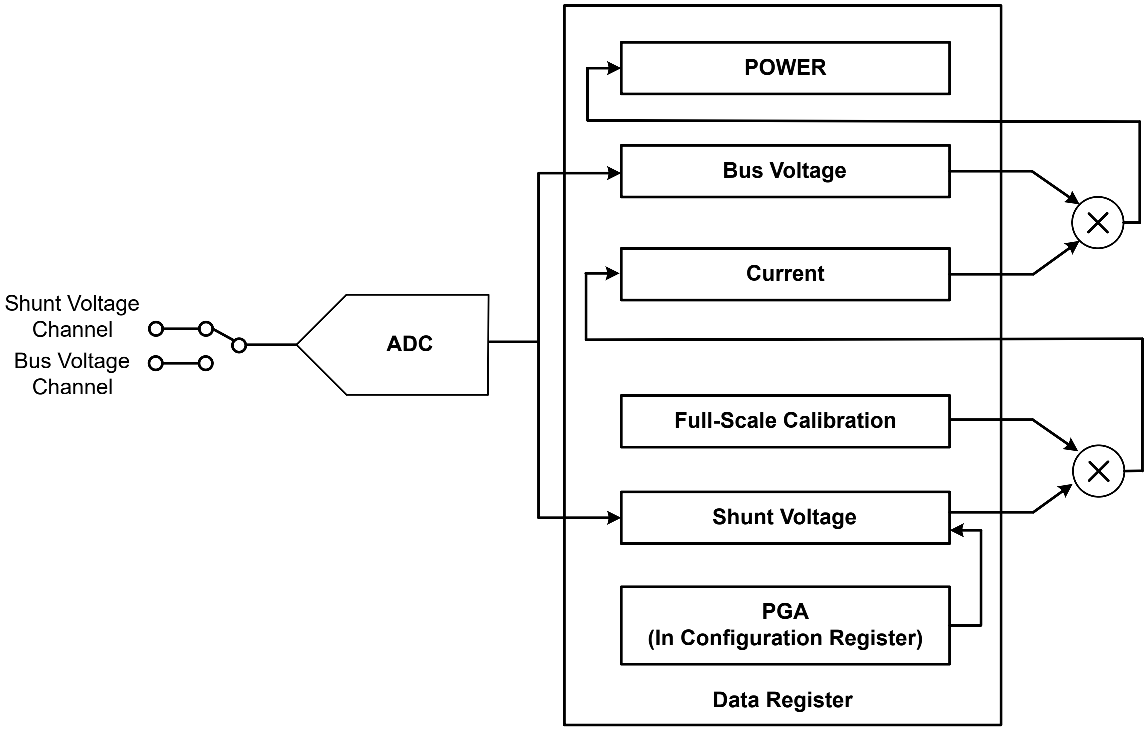
Figure 10. ADC Bus Voltage Offset vs. Temperature

Detailed Description

Overview

The TPA630 is a digital current-sense amplifier featuring an I^{2}C- and SMBus-compatible interface. This device delivers digital current, voltage, and power readings—critical data for making accurate decisions in precision-controlled systems. Programmable registers enable flexible configuration, supporting adjustments to measurement resolution as well as the selection between continuous and triggered operating modes. Comprehensive register information is provided at the end of this data sheet.

Functional Block Diagram



Feature Description

Basic ADC Functions

The TPA630 performs two measurements on the target power-supply bus. Load current flowing through a shunt resistor develops a voltage, which forms a shunt voltage measured at the IN+ and IN– pins. Additionally, the device can measure the power-supply bus voltage by connecting this voltage to the VBUS pin. Specifically, the differential shunt voltage is measured relative to the IN– pin, while the bus voltage is measured relative to ground (GND).

The TPA630 is typically powered by a separate supply, with a voltage range of 2.7 V to 5.5 V. The monitored bus voltage can range from 0 V to 36 V.

The device performs two measurements: shunt voltage and bus voltage. It then converts these measurements into current based on the value of the Calibration Register, and then calculates the power.

The device has two operating modes, continuous and triggered, that determine how the ADC operates following these conversions.

When in normal operating mode (i.e., the MODE bits of the Configuration Register (00h) are set to '111'), the device continuously converts a shunt voltage reading followed by a bus voltage reading. After the shunt voltage is read, a current value is calculated (using Equation 3), and this current value is then used to compute the power result (using Equation 4). These values are stored in an accumulator, and the measurement/calculation sequence repeats until the number of averages set in the Configuration Register (00h) is achieved. After each sequence, the currently measured and calculated values are appended to previously collected data. Once all averaging is completed, the final values for shunt voltage, bus voltage, current, and power are updated in their respective registers, which can then be read. These values remain in the data output registers until replaced by the next fully completed conversion results. Reading the data output registers does not interfere with an ongoing conversion.

The mode control in the Conversion Register (00h) also permits selecting modes to convert only the shunt voltage or the bus voltage to further allow the user to configure the monitoring function to fit the specific application requirements.

All current and power calculations are performed in the background and do not consume conversion time.

In triggered mode, writing any triggered conversion mode into the Configuration Register (00h) (i.e., the MODE bits of the Configuration Register (00h) are set to ‘001’, ‘010’, or ‘011’) triggers a single-shot conversion. This action generates one set of measurement data; therefore, to trigger another single-shot conversion, the Configuration Register (00h) must be written to a second time—even if the mode remains unchanged.

In addition to the two operating modes (continuous and triggered), the device also includes a power-down mode. This mode reduces quiescent current and turns off current into the device inputs, minimizing the impact of power drain when the device is not in use. The registers of the device can still be read from and written to while in power-down mode. The device remains in power-down mode until one of the active mode settings is written into the Configuration Register (00h).

Although the device can be read at any time and data from the last conversion remains available, a Conversion Ready flag bit (Mask/Enable Register, CVRF bit) is provided to assist in coordinating single-shot or triggered conversions. The Conversion Ready flag (CVRF) bit is set high once all conversions, averaging, and multiplication operations are completed.

The Conversion Ready flag (CVRF) bit clears under these conditions:

- Writing to the Configuration Register(00h), except when configuring the MODE bits for power-down mode
- Reading the Mask/Enable Register(06h)

Power Calculation

Current and power are calculated after measuring the shunt voltage and bus voltage, as illustrated in Figure 11. Specifically, current is computed following a shunt voltage measurement, based on the value set in the Calibration Register. If no value is loaded into the Calibration Register, the stored current value will be zero. Power is calculated after a bus voltage measurement, using the previously computed current value and the currently measured bus voltage value. Similarly, if no value is loaded into the Calibration Register, the stored power value will also be zero. It should be noted again that these calculations are performed in the background and do not increase the overall conversion time. These current and power values are regarded as intermediate results (unless the number of averages is set to 1) and are stored in an internal accumulation register rather than the corresponding output registers. After each sample is measured, the newly calculated current and power values are appended to this accumulation register. This process continues until all samples have been measured and averaged in accordance with the number of averages set in the Configuration Register (00h).

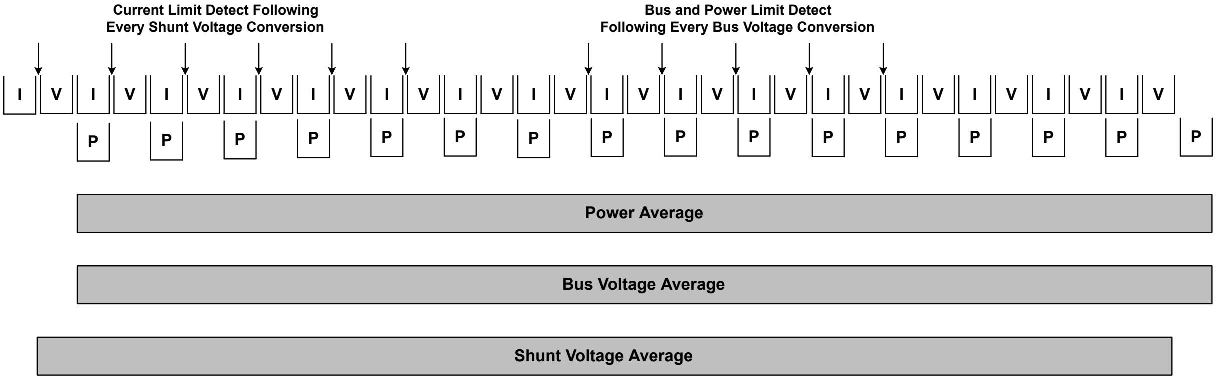


Figure 11. Power Calculation Scheme

In addition to the current and power accumulating after every sample, the shunt and bus voltage measurements are also collected. After all of the samples have been measured and the corresponding current and power calculations have been made, the accumulated average for each of these parameters is then loaded to the corresponding output registers, where the average can then be read.

Alert Pin

The TPA630 is equipped with a single Alert Limit Register (07h), which enables programming of the Alert pin to respond to either a single user-defined event or a Conversion Ready notification, depending on the user’s needs. The Mask/Enable Register allows the user to select one of the five available functions for monitoring and/or set the Conversion Ready bit to control how the Alert pin responds. Based on the function being monitored, the user then inputs a value into the Alert Limit Register to set the corresponding threshold—once this threshold is reached, the Alert pin is asserted.

The Alert pin allows for one of several available alert functions to be monitored to determine if a user-defined threshold has been exceeded. The five alert functions that can be monitored are:

- Shunt Voltage Over-Limit (SOL)
- Shunt Voltage Under-Limit (SUL)
- Bus Voltage Over-Limit (BOL)
- Bus Voltage Under-Limit (BUL)
- Power Over-Limit (POL)

The Alert pin is an open-drain output. This pin is asserted when the alert function selected in the Mask/Enable Register exceeds the value programmed into the Alert Limit Register. Only one of these alert functions can be enabled and monitored simultaneously. If multiple alert functions are enabled, the function selected at the highest significant bit position takes priority and is the only one that responds to the value in the Alert Limit Register. For example, if both the Shunt Voltage Over-Limit function and the Shunt Voltage Under-Limit function are selected, the Alert pin is asserted when the value in the Shunt Voltage Register exceeds the value stored in the Alert Limit Register.

The device's Conversion Ready state can also be monitored via the Alert pin to notify the user when the device has completed the previous conversion and is ready to start a new one. The Conversion Ready state can be monitored through the Alert pin alongside any one of the alert functions. If both an alert function and the Conversion Ready state are configured to be monitored via the Alert pin, after the Alert pin is asserted, the Mask/Enable Register must be read post-alert to identify the source of the alert. The alert source can be determined by reading the Conversion Ready Flag (CVRF, bit 3) and the Alert Function Flag (AFF, bit 4) in the Mask/Enable Register. If the Conversion Ready feature is not required and the CNVR bit is not set, the Alert pin only responds to the exceeded limit condition associated with the enabled alert function.

If the alert function is not in use, the Alert pin can be left floating.

Refer to Figure 11 to get the relative timing of the comparison between the value in the Alert Limit Register and the corresponding converted value. For example, if the enabled alert function is Shunt Voltage Over-Limit (SOL), after each shunt voltage conversion, the value in the Alert Limit Register is compared with the measured shunt voltage to check if the measured value exceeds the programmed limit. Whenever the measured voltage exceeds the value programmed into the Alert Limit Register, bit 4 (the AFF bit) of the Mask/Enable Register is set high. In addition to the assertion of the AFF bit, whether the Alert pin is asserted depends on the setting of the Alert Polarity Bit (APOL, bit 1 of the Mask/Enable Register). If the Alert Latch feature is enabled, the AFF bit and the Alert pin remain asserted until data is written to the Configuration Register (00h) or the Mask/Enable Register is read.

The Bus Voltage-related alert functions compare the measured bus voltage with the value in the Alert Limit Register after each bus voltage conversion. If the limit threshold is exceeded, the AFF bit is set and the Alert pin is asserted.

The Power Over-Limit alert function compares the calculated power value with the value in the Alert Limit Register after each bus voltage measurement conversion. If the limit threshold is exceeded, the AFF bit is set and the Alert pin is asserted.

Device Functional Modes

Averaging and Conversion Time Considerations

The TPA630 provides programmable conversion times (t_{CT}) for both shunt voltage and bus voltage measurements. When combined with the programmable averaging mode, the conversion time settings allow the device to be configured to optimize the available timing requirements in a specific application. Additionally, the device can be configured with different conversion time settings for shunt voltage and bus voltage measurements—a common approach in applications where the bus voltage remains relatively stable. In such cases, the time allocated to bus voltage measurement can be reduced compared to that for shunt voltage measurement.

There are trade-offs between the conversion time settings and the averaging mode used. The averaging feature can significantly enhance measurement accuracy by effectively filtering the signal, which helps reduce measurement noise caused by noise coupling into the signal. A higher number of averages enables the device to more effectively suppress the noise component in the measurement.

The selected conversion times also have an impact on measurement accuracy.

Filtering and Input Considerations

Measuring current is often noisy, and such noise can be difficult to define. The TPA630 provides multiple filtering options through the selection of resolution and averaging modes in the Configuration Register. These filtering options can be configured independently for either voltage measurement or current measurement.

The internal ADC is based on a delta-sigma (ΔΣ) front-end with a 556 kHz (±30%) typical sampling rate. This architecture has good inherent noise rejection; however, transients that occur at or very close to the sampling rate harmonics can cause problems. Since these interfering signals operate at frequencies of 1 MHz and above, they can be mitigated by integrating filtering circuitry at the input of the TPA630. The high frequency enables the use of low-value series resistors on the filter for negligible effects on measurement accuracy. Filter using the lowest possible series resistance and ceramic capacitor. Recommended values are 0.1 to 1 μF. Figure 12 shows the TPA630 with an additional filter added at the input.

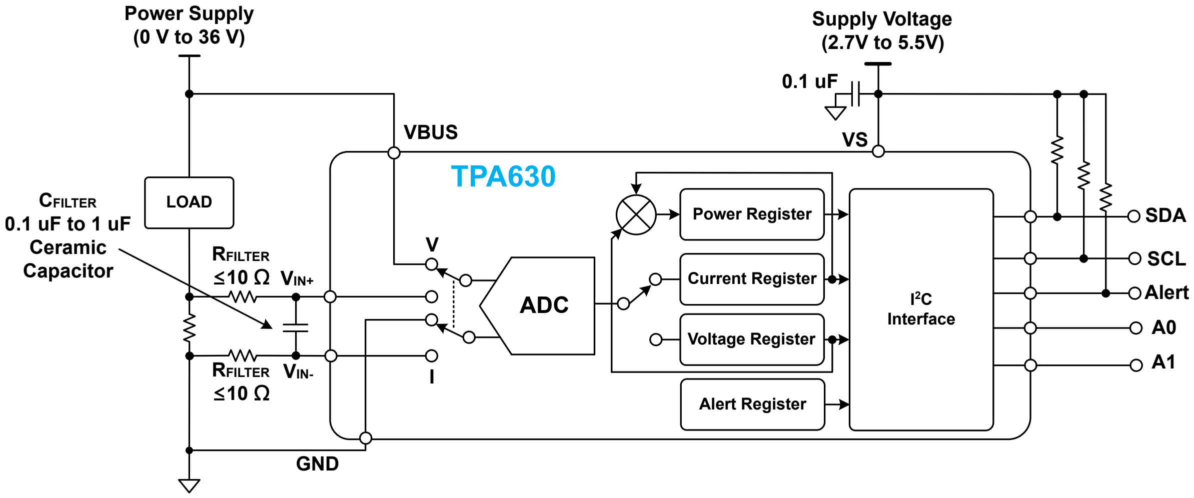


Figure 12. Input Filtering

Overload conditions represent an additional consideration for the TPA630 inputs. The device inputs are specified to tolerate 40 V across the inputs. A large differential scenario might be a short to ground on the load side of the shunt. This type of event can result in full power-supply voltage across the shunt (as long the power supply or energy storage capacitors support it). It must be remembered that removing a short to ground can result in inductive kickbacks that could exceed the 40 V differential and common-mode rating of the TPA630. The most effective approach to mitigating inductive kickback voltages involves the use of zener-type transient-absorbing devices, combined with energy storage capacitors of sufficient capacitance.

In applications that do not have large energy storage electrolytics on one or both sides of the shunt, an input overstress condition may result from an excessive dV/dt of the voltage applied to the input. A hard physical short circuit is the most probable cause of this issue—especially in setups that lack large electrolytic capacitors, where the problem becomes more noticeable. This problem occurs because an excessive dV/dt can activate the ESD protection in the TPA630 in systems where large currents are available. Testing has demonstrated that the addition of 10 Ω resistors in series with each input of the TPA630 sufficiently protects the inputs against dV/dt failure up to the 40 V rating of the TPA630. These resistors have no significant effect on accuracy.

Programming

An important feature of the TPA630 device is that it can perform current or power measurement if programmed according to system requirements. The device measures both the differential voltage applied between the IN+ and IN- input pins and the voltage applied to the VBUS pin. For the device to report both current and power values, the user must program the resolution of the Current Register (04h) and the value of the shunt resistor present in the application to develop the differential voltage applied between the input pins. The Power Register (03h) is internally set to be 25 times the programmed Current_LSB. Both the Current_LSB and shunt resistor value are used in the calculation of the Calibration Register value that the device uses to calculate the corresponding current and power values based on the measured shunt and bus voltages.

After programming the Calibration Register, the Current Register (04h) and Power Register (03h) update accordingly based on the corresponding shunt voltage and bus voltage measurements. Until the Calibration Register is programmed, the Current Register (04h) and Power Register (03h) remain at zero.

Programming the Calibration Register

The Calibration Register is calculated based on Equation 1. This equation includes the term Current_LSB, which is the programmed value for the LSB for the Current Register (04h). The user uses this value to convert the value in the Current Register (04h) to the actual current in amperes. The highest resolution for the Current Register (04h) can be obtained by using the smallest allowable Current_LSB based on the maximum expected current as shown in Equation 2. While this value yields the highest resolution, it is common to select a value for the Current_LSB to the nearest round number above this value to simplify the conversion of the Current Register (04h) and Power Register (03h) to amperes and watts respectively. The R_{SHUNT} term is the value of the external shunt used to develop the differential voltage across the input pins.

$$\text{Cal} = \text{trunc}\left(\frac{0.00512}{\text{Current\_LSB} \times R_{SHUNT}}\right) \tag{1}$$

where

- 0.00512 is an internal fixed value used to ensure scaling is maintained properly

$$\text{Current\_LSB} = \frac{\text{Maximum Expected Current}}{2^{15}} \tag{2}$$

The value of the Current Register (04h) is calculated by multiplying the decimal value of the content in the Shunt Voltage Register (01h) by the decimal value of the Calibration Register, then dividing the product by 2048—this calculation is detailed in Equation 3.

$$\text{Current} = \frac{\text{Shunt Voltage} \times \text{Calibration Register}}{2048} \tag{3}$$

The LSB for the Bus Voltage Register (02h) is a fixed 1.25 mV/bit. Note that the MSB of the Bus Voltage Register (02h) is always zero because the VBUS pin is only able to measure positive voltages.

The value expected in the Power register (03h) can be calculated by multiplying the Current register value by the Bus Voltage register value and then dividing by 20000 as shown in Equation 4.

$$\text{Power} = \frac{\text{Current} \times \text{Bus Voltage}}{20000} \tag{4}$$

Table 2 lists the steps for configuring, measuring, and calculating the values for current and power for this device.

Table 2. Calculating Current and Power

STEP	REGISTER NAME	ADDRESS	CONTENTS	DEC	LSB	VALUE(1)
Step 1	Configuration Register	00h	4127h			
Step 2	Shunt Register	01h	1F40h	8000	2.5 µV	20 mV
Step 3	Bus Voltage Register	02h	2570h	9584	1.25 mV	11.98 V
Step 4	Calibration Register	03h	A00h	2560		
Step 5	Current Register	04h	2710	10000	1 mA	10 A
Step 6	Power Register	05h	12B8h	4792	25 mW	119.82 W

(1) Conditions: Load = 10 A, V_{CM} = 12 V, R_{SHUNT} = 2 mΩ, and V_{VBUS} = 12 V.

Calibration Register and Scaling

The Calibration Register enables the user to scale the Current Register (04h) and Power Register (03h) to the most useful value for a given application. For example, set the Calibration Register such that the largest possible number is generated in the Current Register (04h) or Power Register (03h) at the expected full-scale point. This approach yields the highest resolution using the previously calculated minimum Current_LSB in the equation for the Calibration Register. The Calibration Register can also be selected to provide values in the Current Register (04h) and Power Register (03h) that either provide direct decimal equivalents of the values being measured, or yield a round LSB value for each corresponding register. After these choices have been made, the Calibration Register also offers possibilities for end-user system-level calibration. After determining the exact current by using an external ammeter, the value of the Calibration Register can then be adjusted based on the measured current result of the TPA630 to cancel the total system error as shown in Equation 5 .

$$\text{Corrected\_Full\_Scale\_Cal} = \text{trunc}\left(\frac{\text{Cal} \times \text{MeasShuntCurrent}}{\text{Device\_Current}}\right) \tag{5}$$

Simple Current Shunt Monitor Usage (No Programming Necessary)

The TPA630 can be used without any programming if it is only necessary to read a shunt voltage drop and bus voltage with the default power-on reset configuration and continuous conversion of shunt and bus voltage.

The Current register and Power register are only available if the Calibration register contains a programmed value.

Default Settings

The default power-up states of the registers are shown in the Register Details section of this data sheet. These registers are volatile, and if programmed to other than default values, must be re-programmed at every device power-up. Detailed information on programming the Calibration register specifically is given in the section, Programming the Calibration Register.

Bus Overview

The TPA630 offers compatibility with both I^{2}C and SMBus interfaces. The I^{2}C and SMBus protocols are essentially compatible with one another.

The I^{2}C interface is used throughout this data sheet as the primary example, with SMBus protocol specified only when a difference between the two systems is being addressed. Two bidirectional lines, SCL and SDA, connect the TPA630 to the bus. Both SCL and SDA are open-drain connections.

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates START and STOP conditions.

To address a specific device, the master initiates a START condition by pulling the data signal line (SDA) from a HIGH to a LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and eight bits of data are sent, followed by an Acknowledge bit. During data transfer, SDA must remain stable while SCL is HIGH. Any change in SDA while SCL is HIGH is interpreted as a START or STOP condition.

Once all data has been transferred, the master generates a STOP condition, indicated by pulling SDA from LOW to HIGH while SCL is HIGH. The TPA630 includes a 28-ms timeout on its interface to prevent locking up a bus.

The device can not accept a stop command immediately after a start operation. To reset the I^{2}C communication, send 9 clocks (with SDA HIGH) to the TPA630 after a start operation, to make sure the device is quite to default mode, and then wait for a new I^{2}C start operation.

Serial Bus Address

TPA630 has two I^{2}C address pins, A0 and A1. 16 addresses are available by connecting A0 and A1 to different logic levels. At the beginning of I^{2}C communication, the states of A0 and A1 are sampled by the chip to set the I^{2}C address. Following is the address table:

Table 3. I^{2}C Address Table

A1	A0	Slave Address
GND	GND	1000000
GND	V_S	1000001
GND	SDA	1000010

A1	A0	Slave Address
GND	SCL	1000011
V_S	GND	1000100
V_S	V_S	1000101
V_S	SDA	1000110
V_S	SCL	1000111
SDA	GND	1001000
SDA	V_S	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V_S	1001101
SCL	SDA	1001110
SCL	SCL	1001111

Serial Interface

The TPA630 operates only as a slave device on the I^2C bus and SMBus. Connections to the bus are made through the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. Although the device incorporates spike suppression into its digital I/O lines, proper layout techniques help minimize the amount of interference coupled into the communication lines. This noise injection can stem from two sources: capacitive coupling of signal edges between the two communication lines themselves, or other switching noise sources present in the system. Routing traces in parallel with ground planes between layers of a printed circuit board (PCB) typically mitigates the effects of coupling between the communication lines. Using shielded communication lines reduces the likelihood of unintended noise coupling into the digital I/O lines—such coupled noise could be misinterpreted as start or stop commands.

The TPA630 supports the transmission protocol for fast (1- to 400-kHz) and high-speed (1-kHz to 2.94-MHz) modes. All data bytes are transmitted most significant byte first.

Writing to and Reading from the TPA630

Accessing a particular register on the TPA630 is accomplished by writing the appropriate value to the register pointer. Refer to Table 5 for a complete list of registers and corresponding addresses. The value for the register pointer as shown in Figure 16. Writing to and Reading from the TPA630 is the first byte transferred after the slave address byte with the R/W bit LOW. Every write operation to the device requires a value for the register pointer.

Writing to a register begins with the first byte transmitted by the master. This byte is the slave address, with the R/W bit LOW. The TPA630 then acknowledges receipt of a valid address. The next byte transmitted by the master is the address of the register to which data will be written. This register address value updates the register pointer to the desired register. The next two bytes are written to the register addressed by the register pointer. The TPA630 acknowledges receipt of each data byte. The master may terminate data transfer by generating a START or STOP condition.

When reading from the TPA630, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a slave address byte with the R/W bit LOW, followed by the register pointer byte. No additional data is required. The master then generates a START condition and sends the slave address byte with the R/W bit HIGH to initiate the read command. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register pointer. This byte is followed by an Acknowledge from the master; then the slave transmits the least significant byte. The master acknowledges receipt of the data byte. The master may terminate data transfer by generating a *Not-Acknowledge* after receiving any data byte, or generating a START or STOP condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the TPA630 retains the register pointer value until it is changed by the next write operation.

Figure 13 and Figure 14 show write and read operation timing diagrams, respectively. Note that register bytes are sent most-significant byte first, followed by the least-significant byte. Figure 15 shows the timing diagram for the SMBus Alert response operation. Figure 16 shows a typical register pointer configuration.

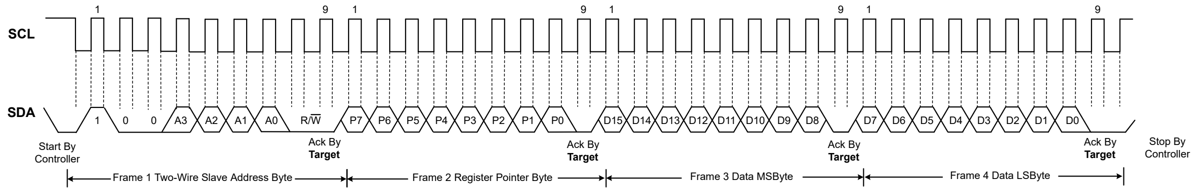


Figure 13. Timing Diagram for Write Word Format

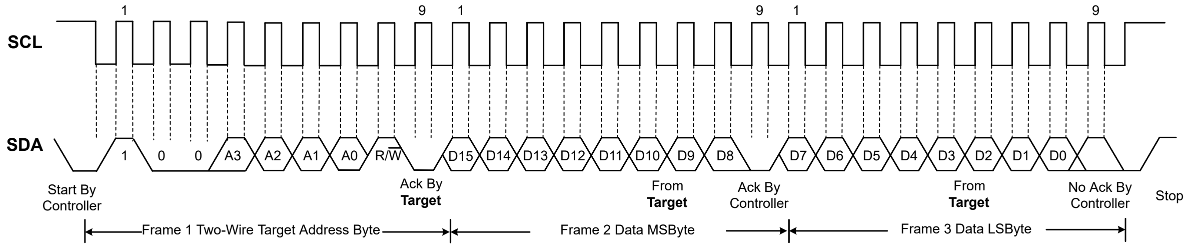


Figure 14. Timing Diagram for Read Word Format

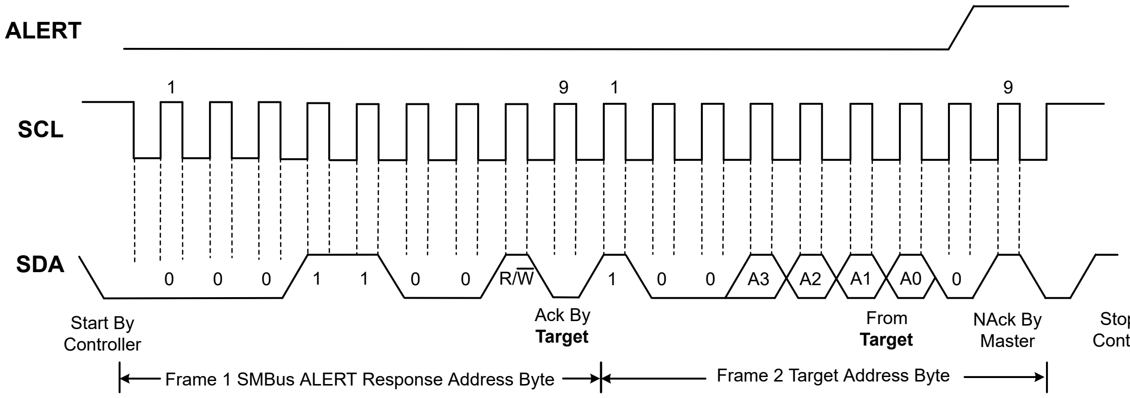


Figure 15. Timing Diagram for SMBus Alert

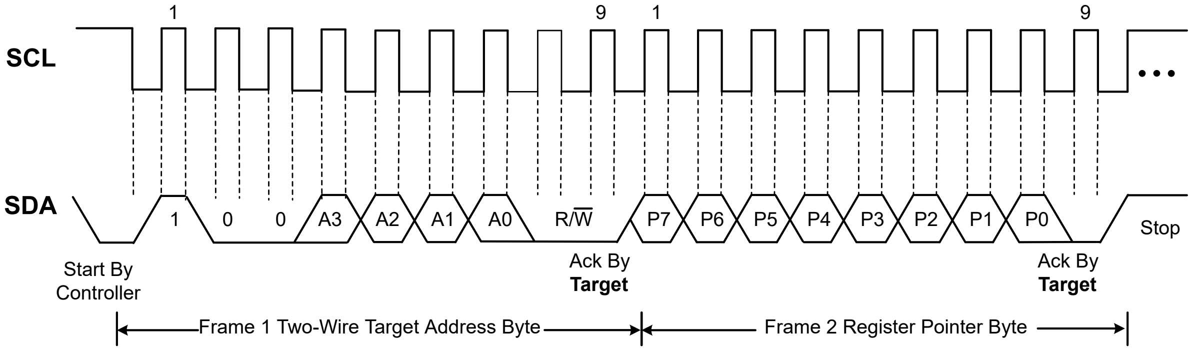


Figure 16. Typical Register Pointer Set

High-Speed I^2C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pull-up devices. The master generates a start condition followed by a valid serial byte containing high-speed (HS) master code *00001XXX*. This transmission is made in fast (400 kHz) or standard (100 kHz) (F/S) mode at no more than 400 kHz. The TPA630 does not acknowledge the HS master code, but does recognize it and switches its internal filters to support 2.94 MHz operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 2.94 MHz are allowed. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS-mode. A stop condition ends the HS-mode and switches all the internal filters of the TPA630 to support the F/S mode.

Table 4. Bus Timing Diagram Definitions (1)

Parameter		Fast Mode		High-speed Mode		Unit
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL operating frequency	0.001	0.4	0.001	2.94	MHz
t_{BUF}	Bus free time between STOP and START condition.	600		160		ns
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock is generated.	100		100		ns
t_{SUSTA}	Repeated START condition setup time	100		100		ns
t_{SUSTO}	STOP condition setup time	100		100		ns
t_{HDDAT}	Data hold time	10	900	10	100	ns
t_{SUDAT}	Data setup time	100		10		ns
t_{LOW}	SCL clock LOW period	1300		250		ns
t_{HIGH}	SCL clock HIGH period	600		60		ns
t_FDA	Data fall time		300		150	ns
t_FCL	Clock fall time		300		40	ns
t_RCL	Clock rise time		300		40	ns
t_RCL	Clock rise time for SCLK≤ 100kHz		1000			ns

(1) Values based on a statistical analysis of a one-time sample of devices. Minimum and maximum values are not ensured and not production tested.

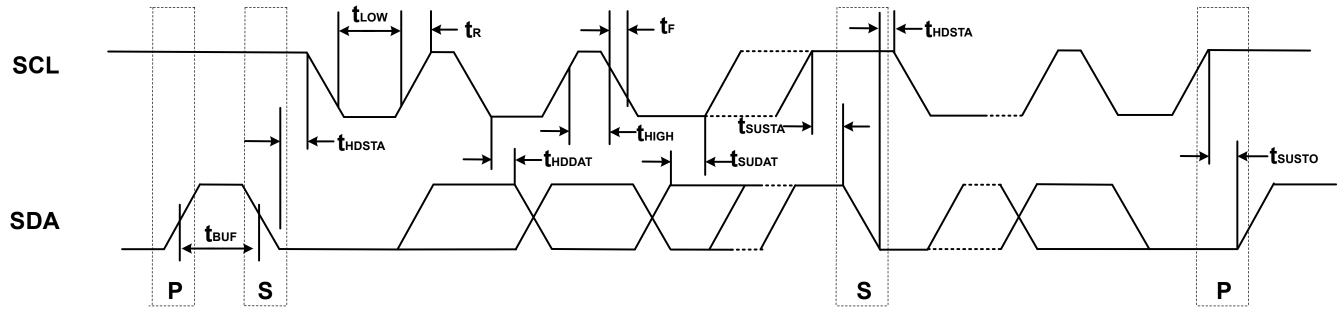


Figure 17. Bus Timing Diagram

SMBus Alert Response

The TPA630 is designed to respond to the SMBus Alert Response address. The SMBus Alert Response feature enables rapid fault identification for simple slave devices. When an alert occurs, the master device can broadcast the Alert Response slave address (0001100) with the Read/Write bit set high. After this Alert Response operation, any slave device that has generated an alert will identify itself by acknowledging the Alert Response and transmitting its own address on the bus. The Alert Response can activate multiple distinct slave devices simultaneously, similar to the General Call function of the I^2C bus. If more than one slave device attempts to respond, the bus arbitration rules shall apply. The device that loses the arbitration will not generate an acknowledge signal and will keep the Alert line low until the interrupt is cleared.

Registers

Register Maps

Table 5. Register Set Summary

Pointer Address	Register Name	Function	Power-on Reset		Type (1)
Hex			Binary	Hex	
00h	Configuration Register	All-register reset, shunt voltage and bus voltage ADC conversion times and averaging, operating mode.	01000001 00100111	4127	R/W
01h	Shunt Voltage Register	Shunt voltage measurement data.	00000000 00000000	0000	R
02h	Bus Voltage Register	Bus voltage measurement data.	00000000 00000000	0000	R
03h	Power Register (2)	Contains the value of the calculated power being delivered to the load.	00000000 00000000	0000	R
04h	Current Register (2)	Contains the value of the calculated current flowing through the shunt resistor.	00000000 00000000	0000	R
05h	Calibration Register	Sets full-scale range and LSB of current and power measurements. Overall system calibration.	00000000 00000000	0000	R/W
06h	Mask/Enable Register	Alert configuration and Conversion Ready flag.	00000000 00000000	0000	R/W
07h	Alert Limit Register	Contains the limit value to compare to the selected Alert function.	00000000 00000000	0000	R/W
FEh	Manufacturer ID Register	Contains unique manufacturer identification number.	0101010001001001	5549	R
FFh	Die ID Register	Contains unique die identification number.	0010001001100000	2260	R

Configuration Register (00h, Read/Write)

Table 6. Configuration Register (00h) (Read/Write) Descriptions

Bit No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RST	—	—	—	AVG2	AVG1	AVG0	VBUSCT2	VBUSCT1	VBUSCT0	VSHCT2	VSHCT1	VSHCT0	MODE3	MODE2	MODE1
Por Value	0	1	0	0	0	0	0	1	0	0	1	0	0	1	1	1

Configuration register settings govern the operating modes of the TPA630. This register determines the conversion time for both shunt and bus voltage measurements, as well as the averaging mode applied. It also programs the operating mode that selects which signals are to be measured.

The Configuration register can be read at any time without disrupting device settings or ongoing conversions. However, writing to this register suspends any active conversion until the write operation is complete, after which a new conversion begins based on the updated register contents. This ensures clear and deterministic conditions for each subsequent conversion.

RST: Reset Bit

Bit 15

Setting this bit to '1' generates a system reset that is the same as a power-on reset; all registers are reset to default values. This bit self-clears.

AVG: Averaging Mode

Bits 9–11

Sets the number of samples that are collected and averaged together. Table 7 summarizes the AVG bit settings and related number of averages for each bit.

Table 7. AVG Bit Settings [11:9] Combinations (1)

AVG2 D11	AVG1 D10	AVG0 D9	Number of Averages
0	0	0	1
0	0	1	4
0	1	0	16
0	1	1	64
1	0	0	128
1	0	1	256
1	1	0	512
1	1	1	1024

(1) Shaded values are default.

VBUSCT: Bus Voltage Conversion Time

Bits 6–8

Sets the conversion time for the bus voltage measurement. Table 8 shows the VBUS CT bit options and related conversion times for each bit.

Table 8. VBUSCT Bit Settings [8:6] Combinations (1)

VBUSCT2 D8	VBUSCT1 D7	VBUSCT0 D6	Conversion Time (µS)
0	0	0	66
0	0	1	134
0	1	0	269
0	1	1	542
1	0	0	1085
1	0	1	2170

VBUSCT2 D8	VBUSCT1 D7	VBUSCT0 D6	Conversion Time (µS)
1	1	0	4341
1	1	1	8682

(1) Shaded values are default.

VSHCT: Shunt Voltage Conversion Time

Bits 3–5

Sets the conversion time for the shunt voltage measurement. Table 9 shows the VSH CT bit options and related conversion times for each bit.

Table 9. VSHCT Bit Settings [5:3] Combinations (1)

VSHCT2 D5	VSHCT1 D4	VSHCT0 D3	Conversion Time
0	0	0	66
0	0	1	134
0	1	0	269
0	1	1	542
1	0	0	1085
1	0	1	2170
1	1	0	4341
1	1	1	8682

(1) Shaded values are default.

MODE: Operating Mode

Bits 0–2

Selects continuous, triggered, or power-down mode of operation. These bits default to continuous shunt and bus measurement mode. The mode settings are shown in Table 10

Table 10. Mode Settings [2:0] Combinations (1)

Mode3 D2	Mode2 D1	Mode1 D0	Mode (1)
0	0	0	Power-Down (or Shutdown)
0	0	1	Shunt Voltage, Triggered
0	1	0	Bus Voltage, Triggered
0	1	1	Shunt and Bus, Triggered
1	0	0	Power-Down (or Shutdown)
1	0	1	Shunt Voltage, Continuous
1	1	0	Bus Voltage, Continuous
1	1	1	Shunt and Bus, Continuous

(1) Shaded values are default.

Shunt Voltage Register (01h, Read-Only)

The Shunt Voltage register holds the measured shunt voltage value, VSHUNT. Negative values are expressed in two's complement form. To obtain the two's complement of a negative number, take the binary representation of its absolute value, invert all bits, and then add 1. Sign extension is applied, where a negative number is indicated by setting the Most Significant Bit (MSB) to '1'.

Example: For a value of VSHUNT = –80 mV:

- 1. Take the absolute value: 80 mV
- 2. Translate this number to a whole decimal number (80 mV ÷ 2.5 μV) = 32000
- 3. Convert this number to binary = 111 1101 0000 0000
- 4. Complement the binary result = 000 0010 1111 1111
- 5. Add '1' to the complement to create the twos complement result = 000 0011 0000 0000
- 6. Extend the sign and create the 16-bit word: 1000 0011 0000 0000 = 8300h

If averaging is enabled, this register displays the averaged value. Full-scale range = 81.9175 mV (decimal = 7FFF); LSB: 2.5 μV.

Table 11. Shunt Voltage Register (01h) (Read-Only) Description

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	SIGN	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Por Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bus Voltage Register (02h, Read-Only)

The Bus Voltage register stores the most recent bus voltage reading, VBUS. If averaging is enabled, this register displays the averaged value. Full-scale range = 40.95875 V (decimal = 7FFF); LSB = 1.25 mV. Do not apply more than 36 V on the BUS pin.

Table 12. Bus Voltage Register (02h) (Read-Only) Description

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	—	BD14	BD13	BD12	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
Por Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Power Register(03h, Read-Only)

If averaging is enabled, this register displays the averaged value. The Power register records power in watts by multiplying the decimal values of the current register with the decimal value of the bus voltage register according to Equation 4

Table 13. Power Register (03h) (Read-Only) Description

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Por Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Current Register (04h, Read-Only)

If averaging is enabled, this register displays the averaged value. The value of the Current register is calculated by multiplying the decimal value in the Shunt Voltage register with the decimal value of the Calibration register, according to Equation 3

Table 14. Current Register (04h) (Read-Only) Register Description

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	CSIGN	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
Por Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Calibration Register (05h, Read/Write)

This register supplies the shunt resistor value to the TPA630, which is used to generate the measured differential voltage. It also defines the resolution of the Current register. By programming this register, the LSB (Least Significant Bit) values for both the Current and Power registers are configured. Additionally, this register serves for overall system calibration.

Table 15. Calibration Register (05h) (Read/Write) Description

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	—	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0
Por Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mask/Enable Register (06h, Read/Write)

The Mask/Enable register configures the source and function of the ALERT pin. In cases where multiple alerts are enabled, the function mapped to the most significant bits (D15:D11) becomes active and responds to the Alert Limit register.

Table 16. Mask/Enable Register (06h) (Read/Write)

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	SOL	SUL	BOL	BUL	POL	CNVR	—	—	—	—	—	AFF	CVRF	OVF	APOL	LEN
Por Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SOL: Shunt Voltage Over-Voltage

Bit 15

Setting this bit high configures the alert pin to be asserted if the shunt voltage measurement following a conversion exceeds the value programmed in the alert limit register.

SUL: Shunt Voltage Under-Voltage

Bit 14

Setting this bit high configures the alert pin to be asserted if the shunt voltage measurement following a conversion drops below the value programmed in the alert limit register.

BOL: Bus Voltage Over-Voltage

Bit 13

Setting this bit high configures the alert pin to be asserted if the bus voltage measurement following a conversion exceeds the value programmed in the alert limit register.

BUL: Bus Voltage Under-Voltage

Bit 12

Setting this bit high configures the alert pin to be asserted if the bus voltage measurement following a conversion drops below the value programmed in the alert limit register.

POL: Power Over-Limit

Bit 11

Setting this bit high configures the alert pin to be asserted if the Power calculation made following a bus voltage measurement exceeds the value programmed in the alert limit register.

CNVR: Conversion Ready

Bit 10

Setting this bit high configures the alert pin to be asserted when the conversion ready flag, Bit 3, is asserted indicating that the device is ready for the next conversion.

AFF: Alert Function Flag

Bit 4

While only one alert function can be monitored at the alert pin at a time, the conversion ready can also be enabled to assert the alert pin. Reading the alert function flag following an alert allows the user to determine if the alert function is the source of the alert.

When the alert latch enable bit is set to latch mode, the alert function flag bit clears only when the mask/enable register is read. When the alert latch enable bit is set to transparent mode, the alert function flag bit is cleared following the next conversion that does not result in an alert condition.

CVRF: Conversion Ready Flag

Bit 3

Although the device can be read at any time, and the data from the last conversion is available, the conversion ready flag bit is provided to help coordinate one-shot or triggered conversions. The conversion ready flag bit is set after all conversions, averaging, and multiplications are complete. The conversion ready flag bit clears under the following conditions:

1. Writing to the configuration register (except for the power-down selection).
2. Reading the mask/enable register.

OVF: Math Overflow Flag

Bit 2

This bit is set to '1' if an arithmetic operation results in an overflow error. It indicates that current and power data may be invalid.

APOL: Alert Polarity bit; sets the Alert pin polarity.

Bit 1

1 = inverted (active-high open collector)

0 = normal (active-low open collector) (default)

LEN: Alert Latch Enable; configures the latching feature of the Alert pin and Alert Flag bits.

Bit 0

1 = latch enabled

0 = transparent (default)

When the alert latch enable bit is set to transparent mode, the alert pin and flag bit resets to the idle states when the fault is cleared. When the alert latch enable bit is set to latch mode, the alert pin and alert flag bit remain active following a fault until the mask/enable register is read.

Alert Limit Register (07h, Read/Write)

To determine if a limit has been exceeded, the value in the register selected by the Mask/Enable register is compared against the threshold stored in the Alert Limit register.

Table 17. Alert Limit Register (07h) (Read/Write) Description

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	AUL15	AUL14	AUL13	AUL12	AUL11	AUL10	AUL9	AUL8	AUL7	AUL6	AUL5	AUL4	AUL3	AUL2	AUL1	AUL0
Por Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Power Supply Recommendations

The input circuitry of the device is capable of accurately measuring signals with common-mode voltages that exceed the power supply voltage, VVS. For instance, while the voltage applied to the V_{VS} power supply terminal may be 5 V, the load power-supply voltage under monitoring (i.e., the common-mode voltage) can reach up to 36 V. It should also be noted that the device can withstand the full 0 V to 36 V range at its input terminals, regardless of whether the device is powered or not.

For optimal stability, place the required power-supply bypass capacitors as close as possible to the device's power and ground pins. A typical value for this bypass capacitor is 0.1 µF. In applications with noisy or high-impedance power supplies, additional decoupling capacitors may be necessary to effectively suppress power-supply noise

Layout

Connect the input pins (IN+ and IN-) to the sensing resistor using a Kelvin connection or a 4-wire connection. These connection techniques verify that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current-sensing resistor, any additional high-current carrying impedance causes significant measurement errors. Place the power-supply bypass capacitor as close as possible to the supply and ground pins.

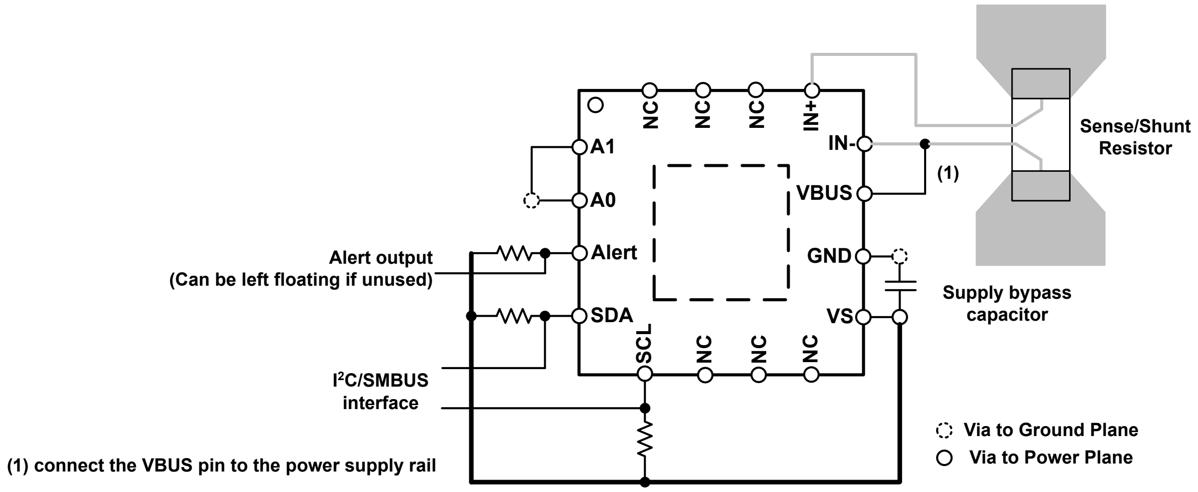
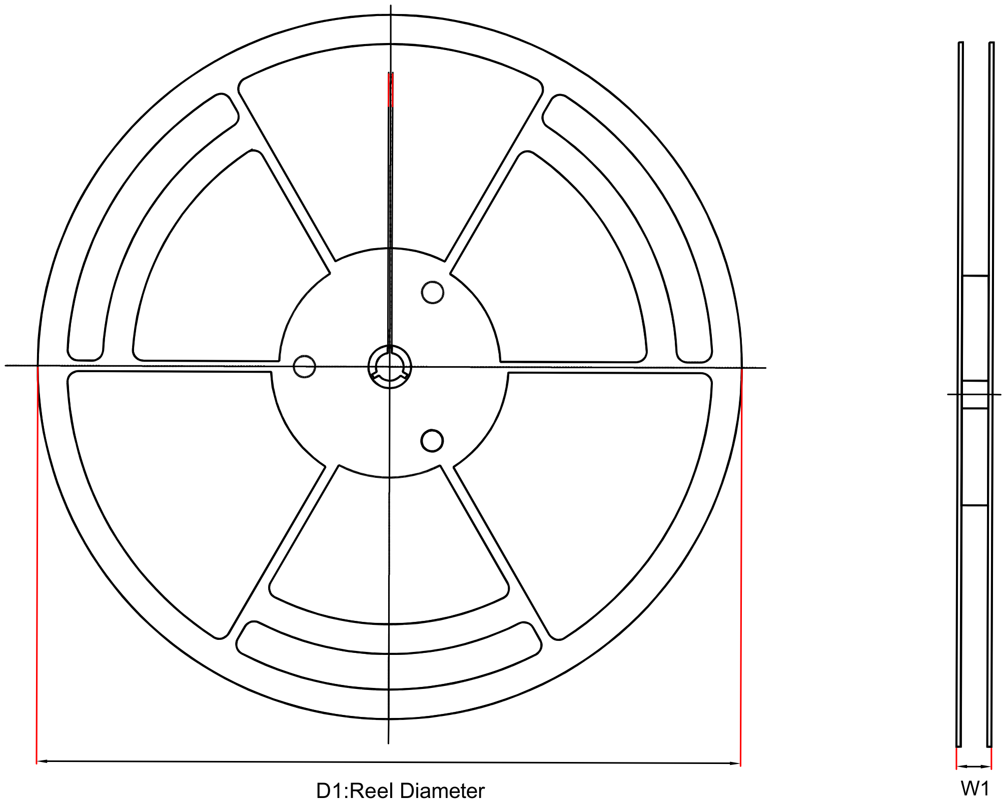
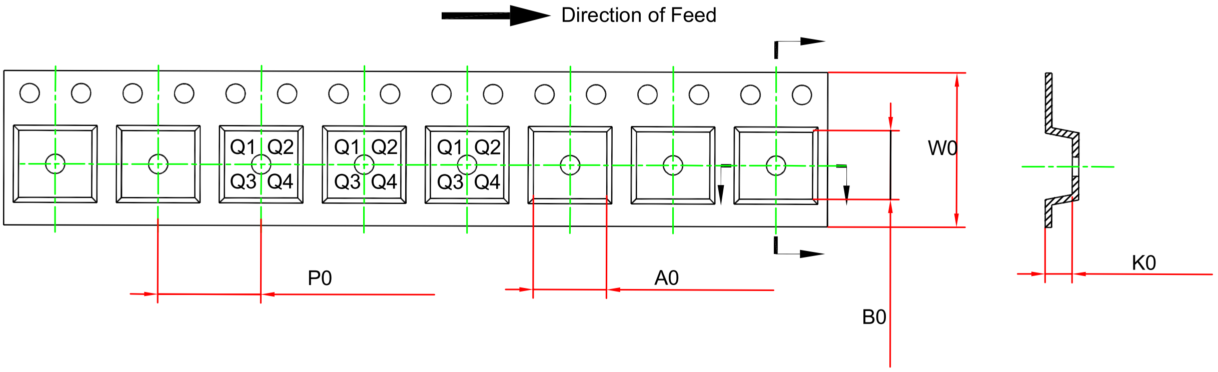


Figure 18. Layout Example

Tape and Reel Information



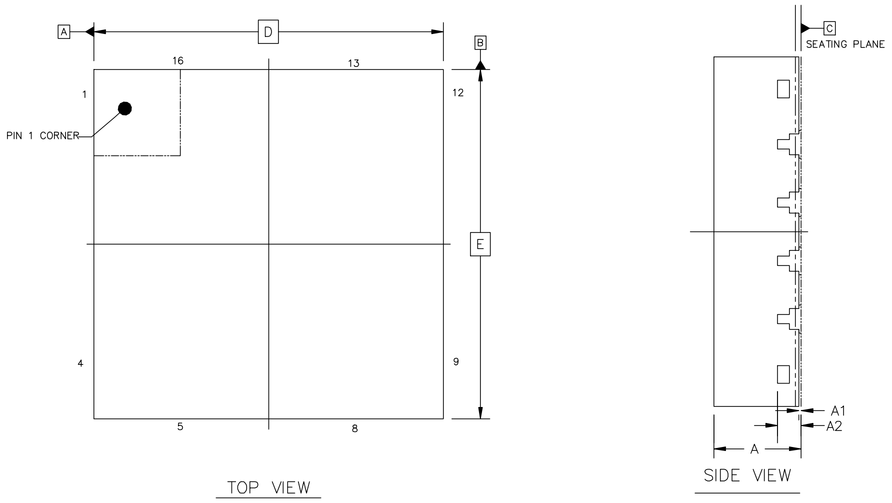


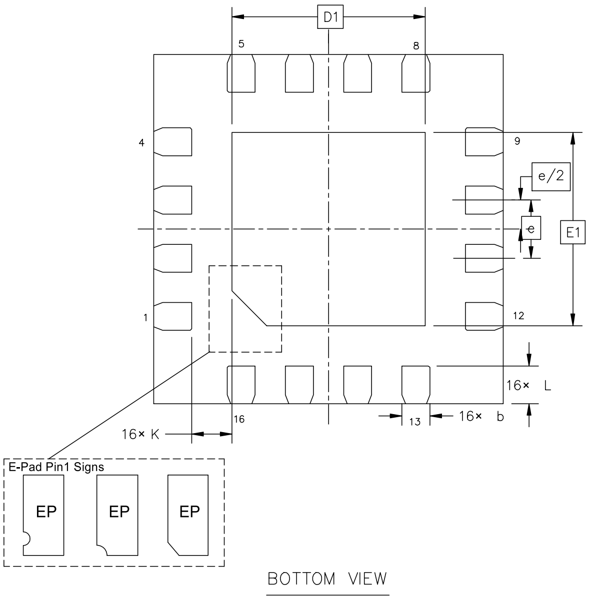
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPA630-QFNR	QFN3×3-16	330.0	17.6	3.3	3.30	1.10	8.0	12.0	Q1

Package Outline Dimensions

QFN3X3-16

Package Outline Dimensions QFN(QFN3X3-16-D)





Symbol	Dimensions In Millimeters MIN	Dimensions In Millimeters MAX	Dimensions In Inches MIN	Dimensions In Inches MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
b	0.180	0.300	0.007	0.012
D	3.000 BSC		0.118 BSC	
D1	1.560	1.760	0.061	0.069
e	0.500 BSC		0.020 BSC	
E	3.000 BSC		0.118 BSC	
E1	1.560	1.760	0.061	0.069
L	0.300	0.500	0.012	0.020
k	0.345 BSC		0.064 BSC	

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPA630-QFNR	−40 to 125℃	QFN3×3-16	TPA630	1	Tape and Reel,4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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