3-Channel, Shunt and Bus Voltage Monitor with I²C and SMBUS Compatible Interface

Features

- Shunt and Bus Voltages up to 36 V
- 3-Channel Monitor
- High Accuracy:
  - Offset Voltage: ±20 μV
  - Gain Error: 0.15%
- Configurable Average Options
- Programmable Addresses
- Programmable Alert and Warning Outputs

Applications

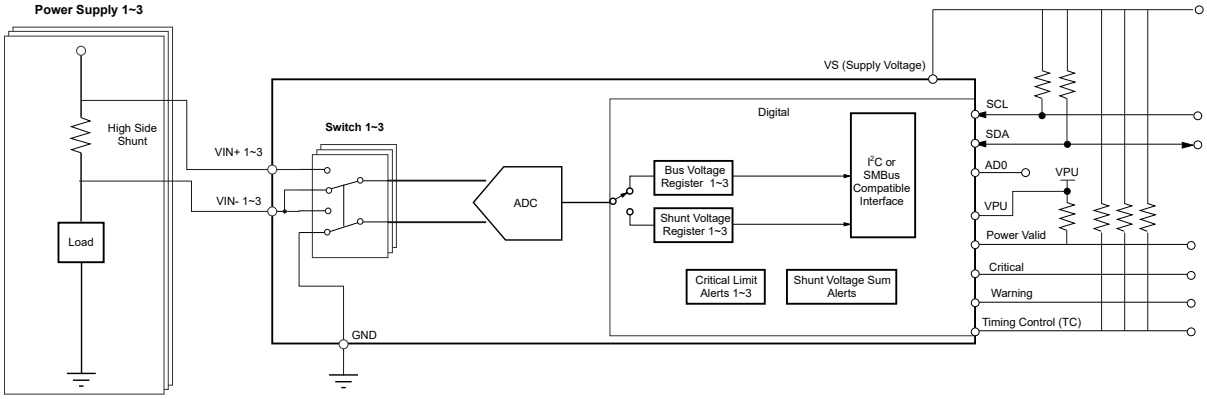
- Servers
- Switches
- Telecom Equipment
- Computers

Description

The TPA6290 is a 3-channel high-side current and bus voltage monitor with I²C/SMBUS compatible interfaces. The device monitors both shunt voltage and bus power supply voltage, and also has programmable conversion time and averaging modes. The device also provides several critical and warning alarms to detect multiple out-of-programmable ranges for each channel.

The TPA6290 can sense a shunt voltage drop on the bus, with bus voltage ranging up to 36 V. The device is powered by a 2.7-V to 5.5-V power supply. The TPA6290 has an operating temperature range of −40°C to +125°C. The I²C and SMBUS-compatible interface has four programmable addresses.

Typical Application Circuit



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Product Family Table

Order Number	Channels	Resolution	Interface	Package
TPA6290-QFPR	3	13 Bit	I²C, SMBUS	QFN4X4-16

Revision History

Date	Revision	Notes
2025-03-28	Rev.A.0	Released version.

Pin Configuration and Functions

TPA6290
QFN4x4-16
Top View

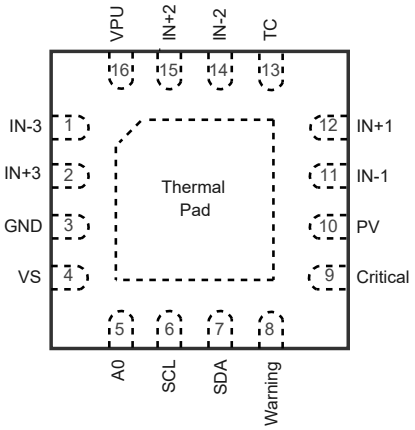


Table 1. Pin Functions:

Pin		I/O	Description
Pin No.	Pin Name		
5	A0	Digital input	Address pin. Connect to GND, SCL, SDA, or V_S.
9	Critical	Digital output	Conversion-triggered critical alert; open-drain output.
3	GND	Analog	Ground
11	IN–1	Analog input	Connect to the load side of the channel 1 shunt resistor. Bus voltage is the measurement from this pin to ground.
12	IN+1	Analog input	Connect to the supply side of the channel 1 shunt resistor.
14	IN–2	Analog input	Connect to the load side of the channel 2 shunt resistor. Bus voltage is the measurement from this pin to ground.
15	IN+2	Analog input	Connect to the supply side of the channel 2 shunt resistor.
1	IN–3	Analog input	Connect to the load side of the channel 3 shunt resistor. Bus voltage is the measurement from this pin to ground.
2	IN+3	Analog input	Connect to the supply side of the channel 3 shunt resistor.
10	PV	Digital output	Power valid alert; open-drain output.
6	SCL	Digital input	Serial bus clock line; open-drain input.
7	SDA	Digital I/O	Serial bus data line; open-drain input/output.
13	TC	Digital output	Timing control alert; open-drain output.
16	VPU	Analog input	Pull-up supply voltage used to bias power valid output circuitry.
4	VS	Analog	Power supply.
8	Warning	Digital output	Averaged measurement warning alert; open-drain output.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Analog Inputs	Differential (V_{IN+}) – (V_{IN-})	−36	36	V
	Common Mode (V_{IN+}) + (V_{IN-})/2	−0.3	36	V
	VPU		36	V
Digital Outputs	Critical, Warning, Power Valid		6	V
	Timing Control		36	V
Serial Bus	SDA	−0.3	6	V
	SCL	−0.3	V_S + 0.3	V
Supply Voltage	V_S	−0.3	6	V
Current	Input, into Any Pin		5	mA
	Open Drain, Digital Output		10	mA
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_S	Operating Supply Voltage	2.7		5.5	V
T_A	Operating temperature	−40		125	℃

Thermal Information

Package Type	θ_{JA}	θ_{JC}	θ_{JB}	Unit
QFN4X4-16	36.5	42.7	14.7	°C/W

Electrical Characteristics

All test conditions: T_A = 25°C, V_S = 3.3 V, V_{IN+} = 12 V, V_{SHUNT} = (V_{IN+}) – ($V_{IN–}$) = 0 mV, and V_{BUS} = $V_{IN–}$ = 12 V, unless otherwise noted.

Parameter		Test Conditions	Min	Typ	Max	Unit
Input						
V_{SHUNT}	Shunt Voltage Input		–163.84		163.8	mV
V_{BUS}	Bus Voltage Input		0		36	V
CMR	Common-mode Rejection	V_{IN+} = 0 V to +36 V	110	120		dB
V_{OS}	Shunt Offset Voltage, RTI (1)			±5	±20	μV
		T_A = −40°C to +125°C		0.1		μV/°C
PSRR		Power supply, V_S = 2.7 V to 5.5 V		15		μV/V
V_{OS}	Bus Offset Voltage, RTI (1)			±2	±4	mV
		T_A = −40°C to +125°C		20		μV/°C
PSRR		V_S power supply		0.5		mV/V
I_{IN+}	Input Bias Current at IN+			6		μA
I_{IN-}	Input Bias Current at IN-			20 || 750		μA || kΩ
	Input Leakage (2)	(IN+ pin) + (IN– pin), power-down mode		0.1	0.5	μA
DC Accuracy						
	ADC Native Resolution			13		Bits
	1-LSB Step Size	Shunt voltage		40		μV
		Bus voltage		8		mV
	Shunt Voltage Gain Error			0.05%	0.15%	
		T_A = −40°C to +125°C		10		ppm/°C
	Bus Voltage Gain Error			0.05%	0.15%	
		T_A = −40°C to +125°C		10		ppm/°C
DNL	Differential Nonlinearity			±0.1		LSB
$t_{CONVERT}$	ADC Conversion Time	CT bit = 000		140		μs
		CT bit = 001		204		
		CT bit = 010		332		
		CT bit = 011		588		
		CT bit = 100		1.1		ms
		CT bit = 101		2.116		
		CT bit = 110		4.156		
		CT bit = 111		8.244		
SMBus						
SMBus Timeout (3)				28	35	ms

Parameter		Test Conditions	Min	Typ	Max	Unit
Digital Input/Output						
C_I	Input Capacitance			3		pF
	Leakage Input Current	$0\ V \le V_{IN} \le V_S$		0.1	1	µA
V_{IH}	High-level Input Voltage		0.7 (V_S)		6	V
V_{IL}	Low-level Input Voltage		–0.5		0.3 (V_S)	V
V_{OL}	Low-level Output Voltage	V_S > +2.7 V, I_{OL} = 3 mA	0		0.4	V
		V_S > +2.7 V, I_{OL} = 1.2 mA	0		0.4	
V_{hys}	Hysteresis Voltage			500		mV
Power Supply						
	Quiescent Current			650	850	µA
		Power-down mode		2	5	
	Power-on Reset Threshold			2		V

(1) RTI = Referred-to-input.
(2) Input leakage is positive (current flows into the pin) for the conditions shown at the top of this table. Negative leakage currents can occur under different input conditions
(3) SMBus timeouts reset the interface whenever SCL is low for more than 28 ms.

Timing Requirements

All parameters are provided by design simulation, unless otherwise noted.

Table 2. Bus Timing Definitions

Parameter		Fast Mode		High-Speed Mode		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL operating frequency	0.001	0.4	0.001	2.44	MHz
$t_{(BUF)}$	Bus free time between stop and start conditions	1300		160		ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	600		160		ns
$t_{(SUSTA)}$	Repeated start condition setup time	600		160		ns
$t_{(SUSTO)}$	STOP condition setup time	600		160		ns
$t_{(HDDAT)}$	Data hold time	0		0		ns
$t_{(VDDAT)}$	Data valid time		1200		260	ns
$t_{(SUDAT)}$	Data setup time	100		10		ns
$t_{(LOW)}$	SCL clock low period	1300		270		ns
$t_{(HIGH)}$	SCL clock high period	600		60		ns
t_{fDA}	Data fall time		500		150	ns
t_{fCL}	Clock fall time		300		40	ns
t_r	Clock rise time		300		40	ns
	Clock rise time for SCLK ≤ 100 kHz		1000			ns

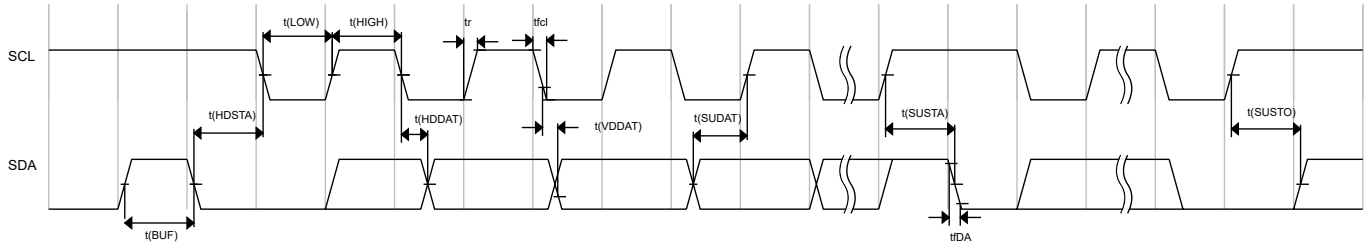


Figure 1. Serial Interface Timing Diagram

Typical Performance Characteristics

All test conditions: $+V_A$ = 5 V, $+V_{BD}$ = 5 V, T_A = +25°C, unless otherwise noted.

Table 3. General

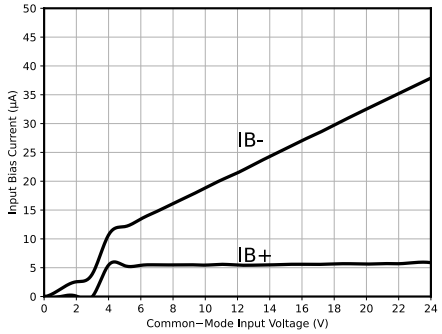


Figure 2. Input Bias Current vs. Common-Mode Voltage

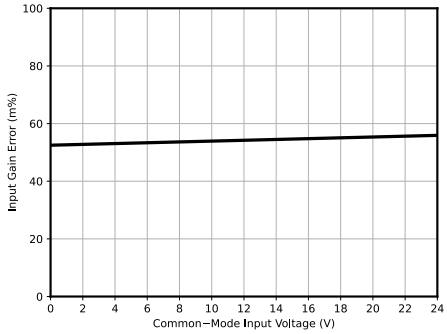


Figure 3. Shunt Gain Error vs. Common-Mode Voltage

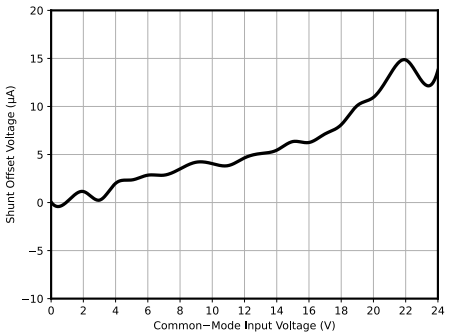


Figure 4. Shunt Offset Voltage vs. Common-Mode Voltage

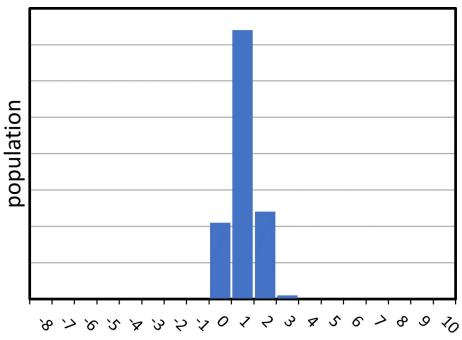


Figure 5. Shunt Offset Voltage Distribution

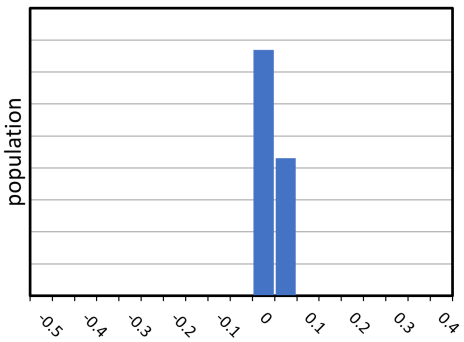


Figure 6. Shunt Offset Voltage Temperature Drift

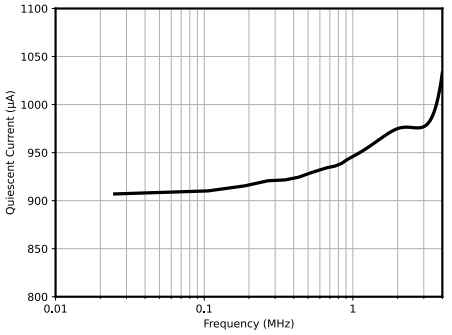


Figure 7. Active IQ vs. I²C Clock Frequency

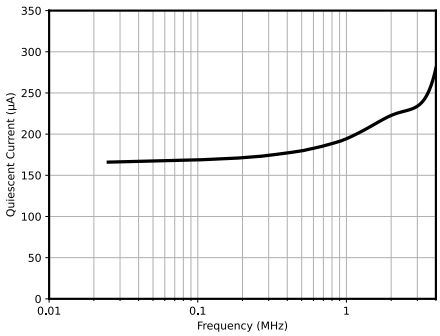


Figure 8. Shutdown IQ vs. I²C Clock Frequency

Detailed Description

Overview

The device is a current-shunt and bus voltage monitor, with an I²C- and SMBus-compatible interface, providing digital shunt and bus voltage. The device also monitors multiple voltage rails and reports error if any voltage fails. Programmable registers offer flexible configuration for measurement precision, and continuous versus single-shot operation modes.

Functional Block Diagram

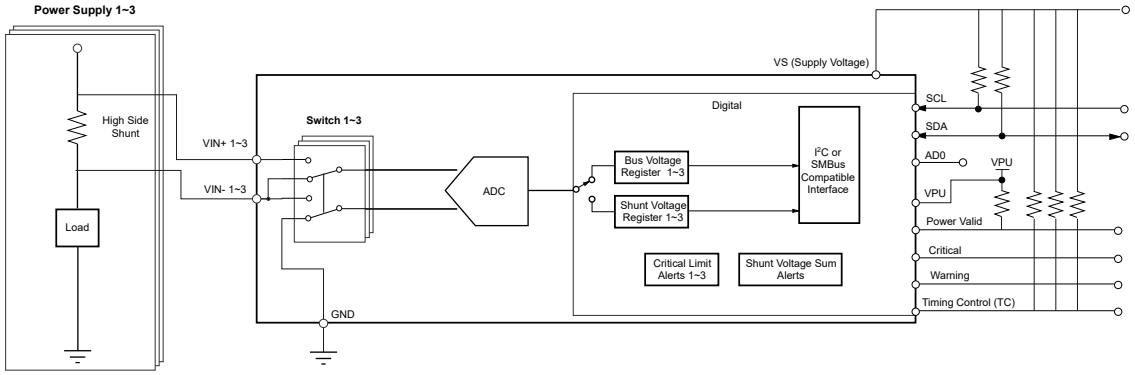


Figure 9. TPA6290 Block Diagram

Feature Description

Basic ADC Functions

The device performs two measurements on three power supplies:

1. The voltage developed from the load current passing through a shunt resistor creates a shunt voltage that is measured between the IN+ and IN– pins. The differential shunt voltage is measured with respect to the IN– pin.
2. The device also internally measures the power-supply bus voltage at the IN– pin for each channel. The bus voltage is measured with respect to ground.

Each measurement can be independently or sequentially measured based on the MODE setting register.

The device has two operating modes, continuous and single-shot， based on the MODE settings.

In single-shot (triggered) mode, setting any single-shot convert mode to the Configuration register (that is, the Configuration register MODE bits set to 001, 010, or 011) triggers a single-shot conversion. When a single-shot conversion is initiated, all enabled channels are measured once and then the device enters a power-down state.

The conversion-ready flag bit (CVRF bit) helps coordinate single-shot conversions, and is especially helpful during longer conversion time settings. The CVRF bit is set after all conversions are complete.

1. Writing to the Configuration register, except when configuring the MODE bits for power-down mode; or
2. Reading the Mask/Enable register.

When the device is set to be in continuous mode (using the MODE bit settings), the device continues to cycle through all enabled channels until a new configuration setting is programmed.

The device also has a separate selectable power-down mode that reduces the quiescent current.

There is no requirement for power sequencing between the input voltage and the power supply voltage.

Alert Monitoring

The device also has multiple monitoring functions with programmable thresholds. The functions are available using 4 alert pins: Critical, Warning, PV (power valid), TC (timing control). These alert pins are open-drain connections.

Critical Alert

The critical-alert feature monitors the functions of each shunt-voltage channel, monitoring their individual conversions. This feature compares the conversion values obtained from each shunt-voltage channel to the programmed threshold values stored in their respective limit registers. The purpose of this comparison is to detect whether the measured values exceed the pre-set limits. If a programmed limit is exceeded, it indicates an abnormally high current flow through the shunt resistor.

Upon initial power-up, the default critical-alert limit for each channel is set to the maximum positive value. However, you can program the limit registers at any time to activate monitoring for any out-of-range conditions. If the measurement of any channel exceeds the limit set in its corresponding critical-alert limit register, the Critical alert pin will be pulled low.

Summation Control Function

The device also incorporates the capability to control the Critical alert pin through the summation control function. This functionality allows for the aggregation of individual shunt-voltage conversions from designated channels (specified by SCC1-3 in the Mask/Enable register). The combined sum is then compared against a programmed limit.

The SCC bits serve a dual purpose: they can either disable the summation control function or enable it to toggle between including two or three channels in the Shunt-Voltage Sum register. The Shunt-Voltage Sum Limit register holds the programmed threshold value that is matched against the value stored in the Shunt-Voltage Sum register. This comparison determines whether the total summed limit has been exceeded.

In the event that the shunt-voltage sum limit is breached, the Critical alert pin will be pulled low. The source of the alert, when the Critical alert pin is triggered, is indicated by either the summation alert flag indicator bit (SF) or the individual critical alert limit bits (CF1-3) within the Mask/Enable register.

It is crucial to note that for the summation limit to yield meaningful results, it is necessary to employ the same shunt-resistor value across all included channels. Unless identical shunt-resistor values are used for each channel, it is not advisable to utilize this function to directly aggregate individual conversion values in the Shunt-Voltage Sum register as a means to report the overall current.

Warning Alert

The warning alert function in the device continuously monitors the average value of each shunt-voltage channel. This average value is determined based on the number of averages specified through the averaging mode bits (AVG1-3) within the Configuration register. Whenever a conversion occurs on a particular channel, the average value is updated in the corresponding shunt-voltage output register.

The device compares this average value against the programmed threshold in the Warning Alert Limit register for each channel. This comparison determines whether the average value has surpassed the limit, indicating whether the average current level is excessively high. Upon initial power-up, the default warning-alert limit for each channel is set to the positive full-scale value, effectively disabling the alert functionality. However, the corresponding limit registers can be programmed at any time to initiate monitoring for conditions outside the desired range.

If any of the channel measurements exceed the limit set in the Warning Alert Limit register for that particular channel, the Warning alert pin will be pulled low. When this occurs, it is necessary to read the Mask/Enable register to identify which channel warning alert flag indicator bit (WF1-3) is active (i.e., set to 1). This information allows for quick identification of the channel responsible for triggering the warning alert.

Power Valid Alert

The Power-Valid alert function of the device is designed to confirm that all monitored power rails are within the required operational levels. This feature is crucial for managing power sequencing and validating the accuracy of the reported measurements based on the system's configuration.

Upon power-up, the Power-Valid mode initiates and detects when each channel exceeds a predefined threshold, which is by default set to 10 volts in the Power-Valid Upper-Limit register. This threshold can be reprogrammed as needed when the device is powered up to a valid supply voltage of at least 2.7 volts.

Once all three bus voltage measurements have reached the value programmed into the Power-Valid Upper-Limit register, the Power-Valid (PV) alert pin asserts a high signal. The PV pin is active low, meaning it remains in a low state until the power-valid conditions are met, at which point it goes high, indicating that all bus voltage rails are above the power-valid upper-limit value.

The Power-Valid alert function also monitors for any bus voltage measurements falling below a lower threshold of 9 volts, which is the default value in the Power-Valid Lower-Limit register. This value is also programmable. If any bus voltage measurement drops below this lower limit, the PV pin returns to a low state, signaling that the power-valid condition is no longer satisfied. At this point, the device resumes monitoring the power rails for a power-valid condition as set in the Power-Valid Upper-Limit register.

It is important to note that for the power-valid alert function to operate correctly, all three channels must be monitored. If not all three channels are in use, the unused channel IN- pin should be connected externally to one of the used channels to ensure the power-valid alert function can detect when all channels reach the power-valid level. Additionally, the power-valid function requires bus voltage measurements to be monitored. Without taking periodic bus voltage measurements, the device cannot determine if the power-valid conditions are maintained.

The PV pin is designed to produce a 0-V output, serving as an indicator for a power-invalid condition. Conversely, when the output is equivalent to the pull-up supply voltage connected to the VPU pin, it signifies a power-valid condition. Additionally, for situations where it's necessary to interface with lower-voltage circuitry, it's possible to reduce the high power-valid pull-up voltage by incorporating a resistor to ground at the PV output. This flexibility allows the function to adapt to different voltage requirements, if required.

Timing Control Alert

The device incorporates a Timing-Control alert function that is designed to ensure the correct sequencing of power supply rails during system startup or reset conditions. This feature is particularly useful for verifying that the power rails are powered up in the proper order, which is critical for preventing potential damage to sensitive components or ensuring system stability.

At startup, the device automatically begins by comparing the bus voltage of channel 1 to detect when it reaches a level of 1.2 volts. This comparison is repeated each time the device cycles back to measuring the bus voltage of channel 1. Once a 1.2-volt level is detected on channel 1, the device then starts checking for the same voltage level on the bus voltage of channel 2.

If the device does not detect a 1.2-volt or higher level on the bus voltage measurement of channel 2 within four complete cycles of all three channels, the Timing-Control (TC) alert pin will assert a low signal. This indication signals that the device has not observed a valid power rail on channel 2 within the expected timeframe. As shown in the Timing Control Timing Diagram, this allows for approximately 28.6 milliseconds from the time a 1.2-volt level is confirmed on channel 1 for a valid voltage to be detected on channel 2.

It is important to note that the Timing-Control alert function is only active during power-up or when a software reset is initiated by setting the reset bit (RST) in the Configuration register. The timing of the alert is based on the default device settings at power-up, and any write to the Configuration register before the Timing-Control alert function completes its full sequence will disable the alert until the next power cycle or software reset occurs.

Software Reset

The device incorporates a software reset feature, enabling the device to reset its configuration and registers to their factory-default state without requiring a power cycle. This is achieved by setting the reset bit (RST) in the Configuration register. Upon activation of the RST bit, the device reverts all settings to their initial defaults, with the exception of the power-valid output state, which remains unaffected. Following a software reset, the device retains the output of the Power-Valid (PV) pin until the power-valid detection sequence is fully executed. This ensures that the power-valid conditions are validated as per the original thresholds, preventing any disruption to the connected circuitry during the reset process. This functionality is crucial for maintaining system integrity and allows for quick troubleshooting and configuration adjustments without the need for physical power cycling.

Averaging Function

The device is equipped with an averaging function that enhances the measurement accuracy by smoothing out the data from the shunt and bus voltage measurements. This feature is particularly beneficial in systems with multiple power rails, where noise and voltage fluctuations can impact the precision of the readings.

The averaging function operates by taking multiple readings of the input signals and combining them to produce a single, averaged value. This process reduces the effect of transient noise and provides a more stable and consistent measurement. The number of averages can be configured through the Configuration register, allowing the user to choose the level of noise reduction based on the specific requirements of the application.

The process of averaging in the device starts with the measurement of the shunt input signal from channel 1. This measured value is then subtracted from the existing value in the data output register. The resulting difference is divided by the number set by the averaging mode configuration (determined by bits 11-9 in the Configuration register, labeled AVG2-0). This quotient is then stored in an internal register.

Subsequently, this quotient is added to the current content of the data output register. The new sum is then written back into the data output register. Once this update is complete, the system proceeds to measure the next signal following the same procedure. The impact of each new measurement on the overall average is reduced as the averaging mode setting increases. Essentially, the averaging feature acts as a noise filter, minimizing the effect of input noise on the measured average.

Multiple Channel Monitoring

The device is capable of monitoring shunt and voltage measurements across up to three distinct power-supply rails, while also measuring up to six diverse signals. Users can regulate the number of channels and signals being gauged by configuring the channel enable (ranging from CH1en to CH3en) and mode (MODE3-1) bits within the Configuration register. This flexibility enables the device to be tailored and optimized precisely based on the specific application requirements of the system in operation.

Channel Configuration

If it is necessary to monitor all three channels upon system startup but only require monitoring of a single channel once the system is stable, the other two channels should be disabled post power-up. This approach ensures that the device focuses solely on the power-supply rail of interest. Disabling unused channels enhances the system's response time by allowing the device to return more swiftly to sampling the active channel. The device provides linear monitoring of the enabled channels. For instance, if all channels are active and are set to measure both shunt and bus voltages, the device will complete five additional conversions before it revisits a specific signal for another conversion cycle. To accelerate this process, reducing the wait to two conversions before re-initiating a conversion on the same channel, the operating mode can be adjusted to measure only the shunt voltage. This modification streamlines the monitoring process and prioritizes the channel of interest.

Timing also plays a critical role in managing the reduction of measured signals. The total duration to finish a sequence that includes shunt- and bus-voltage measurements for all channels equates to the sum of the individual shunt-voltage conversion time and the bus-voltage conversion time, both of which are set by the CT bits in the Configuration register—multiplied by three for the three channels. While the conversion times for shunt and bus voltages can be programmed separately, the chosen durations influence all active channels uniformly.

To focus exclusively on monitoring a single channel with a single signal, enable only that specific channel. This configuration ensures the quickest response to any changes in the monitored signal, as it eliminates any interval between the completion of one measurement cycle and the commencement of the next for that channel. The conversion time remains consistent regardless of whether other channels are enabled or disabled. Choosing to measure both shunt- and bus-voltages, along with enabling multiple channels, will increase the time gap between successive measurements of the same signal. This is because the device must cycle through the additional conversions for the other settings and channels before it can return to measure the same signal again.

Averaging and Conversion-Time Considerations

The device offers adjustable conversion times for both shunt and bus voltage measurements, with options ranging from 140 microseconds to 8.244 milliseconds. These customizable settings, in conjunction with the programmable averaging mode, allow the device to adapt to the timing demands of various applications. For instance, to accommodate a system needing readings every 2 milliseconds across all three channels, the device can be set with a conversion time of 332 microseconds for both shunt and bus voltage measurements.

The device also permits separate conversion times for shunt and bus voltages, which is useful in scenarios where the bus voltage is less volatile. This customization can reduce the measurement time for bus voltage relative to shunt voltage. For instance, a shunt voltage conversion time of 4.156 milliseconds can be paired with a bus voltage conversion time of 588 microseconds, allowing for a 5-millisecond update cycle. However, there are trade-offs with the selection of conversion time and averaging mode. The averaging function enhances measurement precision by filtering out noise from the signal, leading to more accurate readings. Increasing the number of averages further refines this noise reduction. Yet, this improved accuracy comes with a longer response time to changes in the input signal, as the averaged value takes more time to represent the most recent input condition. To counterbalance this, the device features a critical-alert function that evaluates each individual conversion, determining if the measured signal, inclusive of noise, has surpassed the maximum threshold. This ensures that rapid responses to critical conditions are maintained, even while benefiting from the noise reduction provided by the averaging mode.

Filtering and Input Considerations

Current measurement often involves noise, which can be challenging to characterize. The device provides multiple filtering capabilities by enabling the independent selection of conversion times and the number of averages in the Configuration

register. This feature allows for the independent setting of conversion times for shunt- and bus-voltage measurements, offering greater adaptability in monitoring power supply buses.

The device's internal ADC employs a delta-sigma (ΔΣ) architecture, which typically operates at a 500 kHz sampling rate with a ±30% variance. This design inherently rejects noise well. However, issues can arise from transients that coincide with or are very close to the harmonics of the sampling rate, particularly those at 1 MHz and above. To manage these high-frequency transients, the device input should be equipped with a filter. The use of low-value series resistors in conjunction with high-frequency signals is permissible and has a minimal impact on the accuracy of the measurements. In most cases, input filtering for the device is only required if there are transients at precise harmonics of the 500 kHz sampling rate that exceed 1 MHz. It is recommended to use the lowest possible series resistance, generally 10 Ω or lower, in conjunction with a ceramic capacitor. The suggested range for capacitor values is between 0.1 μF and 1.0 μF.

The device is designed to handle input voltages up to the specification across its terminals. Nonetheless, it is essential to consider potential overload scenarios, such as a short circuit to ground on the shunt's load side. In such a case, the full power supply voltage could be applied across the shunt if the power supply or energy storage capacitors allow it. It's important to note that clearing a ground short can lead to inductive kickbacks that might surpass differential and common-mode voltage limits of the device. To mitigate this, zener-type transient-absorbing devices, known as transzorbs, along with adequate energy storage capacitance, are recommended. In systems lacking substantial energy-storage capacitors across the shunt, an excessive rate of voltage change (dV/dt) can lead to an overstress condition at the inputs. A physical short circuit is often the cause of such an event, especially in the absence of large electrolytic capacitors. The high dV/dt can trigger the device's ESD protection mechanism in systems with high current availability. To counteract this, it has been found that incorporating 10-ohm resistors in series with each input of the device can effectively safeguard against dV/dt-induced failures up to the device's specification. Using resistors within the specified range has a negligible impact on the measurement accuracy.

Programming

Bus Overview

The device is designed to be compatible with both I2C and SMBus interfaces, which are fundamentally compatible protocols.

The I2C interface is predominantly utilized as the reference protocol in this datasheet, with the SMBus protocol mentioned only in instances where it deviates from the I2C standard. Communication with the device is established through two I/O lines: the serial clock (SCL) and the serial data (SDA), both of which are configured as open-drain outputs. In the I²C framework, the device that initiates communication is termed the 'master,' while the devices it controls are referred to as 'slaves.' The master is responsible for generating the SCL signal, managing bus access, and initiating start and stop conditions on the bus.

To communicate with a specific slave device, the master starts by generating a start condition, which involves pulling the SDA line from high to low while the SCL line is high. Upon the rising edge of the SCL, all slaves on the bus sample the slave address byte, where the last bit of this byte indicates the direction of the transaction (read or write). At the ninth clock pulse, the addressed slave acknowledges the master by setting an acknowledge bit and pulling the SDA line low. Once acknowledged, the master proceeds to transfer data, sending eight bits of information followed by an acknowledge bit from the slave.

It is crucial that the SDA line remains stable when the SCL is high, as any change during this period would be recognized as a start or stop condition. Upon completion of the data transfer, the master signals a stop condition by transitioning the SDA line from low to high with the SCL line high.

The device is equipped with a 28-millisecond timeout feature to prevent potential bus lockups during communication.

Serial Bus Address

To establish communication with the device, the master device must initially target the slave devices using a specific slave address byte. This byte comprises seven address bits along with a direction bit, which serves as an indicator for the intended operation — whether it's a read or a write. The device incorporates a single address pin, labeled A0.

Table 1 enumerates the logic levels of this pin for each of the four potential addresses. The A0 pin's state is examined during every bus communication, thus necessitating its configuration prior to any activity on the interface.

Table 4. Address Pins and Slave Addresses

A0	Slave Address
GND	1000000
VS	1000001
SDA	1000010
SCL	1000011

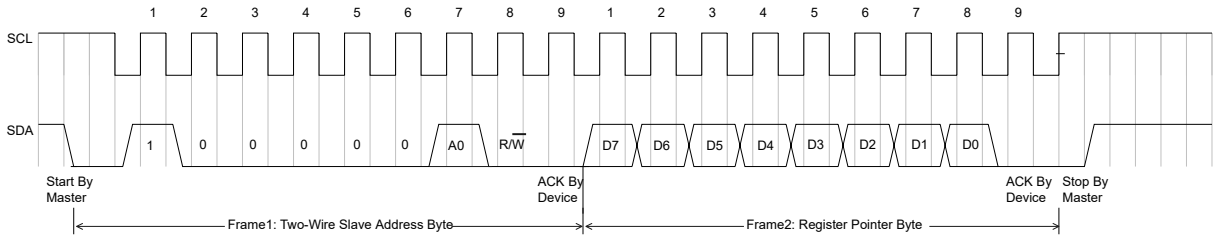
Serial Interface

The device functions exclusively as a slave device on both the I2C bus and SMBus. Its bus connections are established through open-drain I/O lines, namely SDA and SCL. These pins are equipped with integrated spike-suppression filters and Schmitt triggers, designed to minimize the impact of input spikes and bus noise. Although the digital I/O lines incorporate spike suppression, it is crucial to adopt an appropriate layout to further reduce any potential coupling onto the communication lines. Noise may arise from capacitive coupling of signal edges between the communication lines themselves or from other switching noise sources within the system. To minimize coupling effects, routing traces parallel to the ground layer on a printed circuit board (PCB) is generally recommended. Additionally, shielding the communication lines can help reduce the likelihood of unintended noise coupling into the digital I/O lines, which could lead to misinterpretation as start or stop commands.

The device supports a transmission protocol for Fast (1 kHz to 400 kHz) and High-speed (1 kHz to 2.44 MHz)modes. All data bytes are transmitted MSB first.

Writing to and Reading from the Device

To access a specific register, write the appropriate value to the register pointer. The value for the register pointer is the first byte transferred after the slave address byte with the R/W bit low. Every write operation to the device requires a register pointer value.



(1) The value of the Slave Address Byte is determined by the A0 pin setting

Figure 10. Typical Register Pointer Set

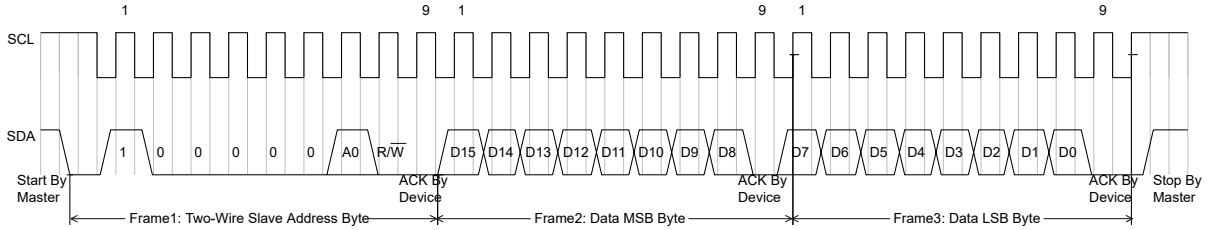
The process of writing to registers begins with the master transmitting the first byte, which serves as the slave address with the R/W bit set to low. Upon receipt of this valid address, the device acknowledges its recognition. Subsequently, the master sends the next byte, indicating the register address where the data is to be written. This value updates the register pointer, directing it to the designated register. Following this, the master writes the next two bytes directly to the register addressed by the pointer. Each data byte is acknowledged by the device. The master then terminates the data transfer by initiating a start or stop condition.

When reading from the device, the register to be accessed is determined by the last value stored in the register pointer during a write operation. To change the register being read, a new value must be written to the register pointer. This is achieved by sending a slave address byte with the R/W bit set to low, followed by the updated register pointer byte. No additional data is required at this stage. Subsequently, the master generates a start condition and transmits the slave address byte with the R/W bit set to high, initiating the read command. The slave then transmits the most significant byte of the

designated register, followed by an acknowledgment from the master. Next, the slave sends the least significant byte, which is acknowledged by the master upon receipt. The master terminates the data transfer by either sending a not-acknowledge after receiving any data byte or generating a start or stop condition.

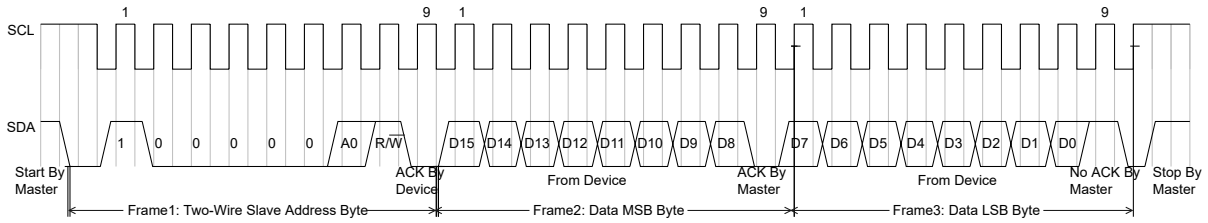
If multiple reads from the same register are desired, there's no need to continuously resend the register pointer bytes; the device retains the register pointer value until it's altered by the next write operation.

The following shows the write and read operation timing diagrams, respectively. Note that register bytes are sent most-significant byte first, followed by the least significant byte.



(1) The value of the slave address byte is determined by the A0 pin setting.

Figure 11. Timing Diagram for Write Word Format



(1) The value of the slave address byte is determined by the A0 pin setting
(2) Read data is from the last register pointer location. If a new register is desired, the register pointer must be updated.
(3) The master can also send an ACK.

Figure 12. Timing Diagram for Read Word Format

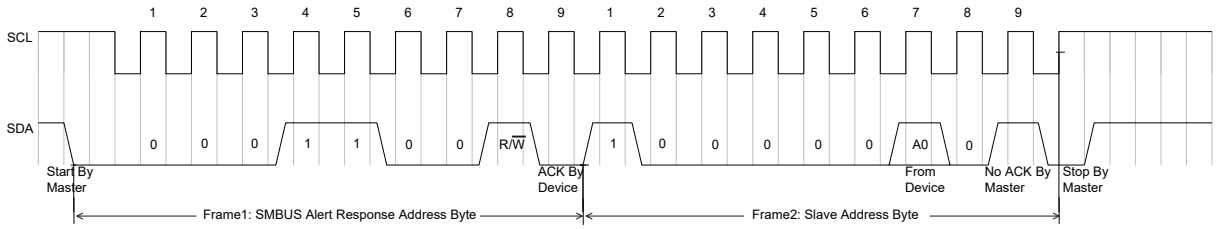


Figure 13.

(1) The value of the Slave Address Byte is determined by the A0 pin setting.

High-Speed I²C Mode

When the bus is inactive, the SDA and SCL lines are automatically raised to a high state by the pull-up resistors. To initiate communication, the master creates a start condition and proceeds to transmit a valid serial byte, which includes the high-speed (Hs) master code 00001XXX. This communication occurs in either fast (400 kHz) or standard (100 kHz) (F/S) mode, with a maximum transmission speed of 400 kHz. While the device does not provide an acknowledgment for the Hs master code, it recognizes it and adjusts its internal filters accordingly to support a 2.44-MHz operation. After establishing the initial communication, the master generates a repeated start condition, which follows the same timing as the initial start condition. From this point onward, the communication protocol remains the same as in F/S mode, with the exception that transmission speeds can now reach up to 2.44 MHz. Instead of employing a stop condition to terminate the communication, the master utilizes repeated start conditions to maintain the bus in Hs mode. A stop condition is required to exit Hs mode, at which point all internal filters in the device revert to supporting F/S mode.

Register Maps

The device uses a bank of registers for holding configuration settings, measurement results, minimum and maximum limits, and status information.

Table 5. Summary of Register Set

Pointer Address (Hex)	Register Name	Description	Power-on Reset		Type (1)
			Binary	Hex	
0	Configuration	All-register reset, shunt and bus voltage ADC conversion times and averaging, operating mode.	01110001 00100111	7127	R/$\overline{W}$
1	Channel-1 Shunt Voltage	Averaged shunt voltage value.	00000000 00000000	0000	R
2	Channel-1 Bus Voltage	Averaged bus voltage value.	00000000 00000000	0000	R
3	Channel-2 Shunt Voltage	Averaged shunt voltage value.	00000000 00000000	0000	R
4	Channel-2 Bus Voltage	Averaged bus voltage value.	00000000 00000000	0000	R
5	Channel-3 Shunt Voltage	Averaged shunt voltage value.	00000000 00000000	0000	R
6	Channel-3 Bus Voltage	Averaged bus voltage value.	00000000 00000000	0000	R
7	Channel-1 Critical Alert Limit	Contains limit value to compare each conversion value to determine if the corresponding limit has been exceeded.	01111111 11111000	7FF8	R/$\overline{W}$
8	Channel-1 Warning Alert Limit	Contains limit value to compare to averaged measurement to determine if the corresponding limit has been exceeded.	01111111 11111000	7FF8	R/$\overline{W}$
9	Channel-2 Critical Alert Limit	Contains limit value to compare each	01111111 11111000	7FF8	R/$\overline{W}$

Pointer Address (Hex)	Register Name	Description	Power-on Reset		Type (1)
			Binary	Hex	
		conversion value to determine if the corresponding limit has been exceeded.			
A	Channel-2 Warning Alert Limit	Contains limit value to compare to averaged measurement to determine if the corresponding limit has been exceeded.	01111111 11111000	7FF8	R/$\overline{W}$
B	Channel-3 Critical Alert Limit	Contains limit value to compare each conversion value to determine if the corresponding limit has been exceeded.	01111111 11111000	7FF8	R/$\overline{W}$
C	Channel-3 Warning Alert Limit	Contains limit value to compare to averaged measurement to determine if the corresponding limit has been exceeded.	01111111 11111000	7FF8	R/$\overline{W}$
D	Shunt-Voltage Sum	Contains the summed value of the each of the selected shunt voltage conversions.	00000000 00000000	0000	R
E	Shunt-Voltage Sum Limit	Contains limit value to compare to the Shunt Voltage Sum register to determine if the corresponding limit has been exceeded.	01111111 11111110	7FFE	R/$\overline{W}$

Pointer Address (Hex)	Register Name	Description	Power-on Reset		Type (1)
			Binary	Hex	
F	Mask/Enable	Alert configuration, alert status indication, summation control and status.	00000000 00000010	0002	R/$\overline{W}$
10	Power-Valid Upper Limit	Contains limit value to compare all bus voltage conversions to determine if the Power Valid level has been reached.	00100111 00010000	2710	R/$\overline{W}$
11	Power-Valid Lower Limit	Contains limit value to compare all bus voltage conversions to determine if the any voltage rail has dropped below the Power Valid range.	00100011 00101000	2328	R/$\overline{W}$
FE	Manufacturer ID	Contains unique manufacturer identification number.	01010101 01001001	5549	R
FF	Die ID	Contains unique die identification number.	00110010 00100000	3220	R

(1) Type: R = read-only, R/$\overline{W}$ = read/write.

Register Descriptions

All 16-bit registers are two 8-bit bytes via the I²C interface.

Table 6. Register Map

Register	ADDRESS (Hex)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Configuration	00	RST	$CH1_{en}$	$CH2_{en}$	$CH3_{en}$	AVG2	AVG1	AVG0	V_{BUS}CT2	V_{BUS}CT1	V_{BUS}CT0	V_{SH}CT2	V_{SH}CT1	V_{SH}CT0	MODE3	MODE2	MODE1

Register	ADDRESS (Hex)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Channel-1 Shunt Voltage	01	SIGN	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	—	—	—
Channel-1 Bus Voltage	02	SIGN	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	—	—
Channel-2 Shunt Voltage	03	SIGN	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	—	—	—
Channel-2 Bus Voltage	04	SIGN	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	—	—
Channel-3 Shunt Voltage	05	SIGN	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	—	—	—
Channel-3 Bus Voltage	06	SIGN	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	—	—
Channel-1 Critical-Alert Limit	07	C1L12	C1L11	C1L10	C1L9	C1L8	C1L7	C1L6	C1L5	C1L4	C1L3	C1L2	C1L1	C1L0	—	—	—
Channel-1 Warning-Alert Limit	08	W1L12	W1L11	W1L10	W1L9	W1L8	W1L7	W1L6	W1L5	W1L4	W1L3	W1L2	W1L1	W1L0	—	—	—
Channel-2 Critical-Alert Limit	09	C2L12	C2L11	C2L10	C2L9	C2L8	C2L7	C2L6	C2L5	C2L4	C2L3	C2L2	C2L1	C2L0	—	—	—
Channel-2 Warning-Alert Limit	0A	W2L12	W2L11	W2L10	W2L9	W2L8	W2L7	W2L6	W2L5	W2L4	W2L3	W2L2	W2L1	W2L0	—	—	—
Channel-3 Critical-Alert Limit	0B	C3L12	C3L11	C3L10	C3L9	C3L8	C3L7	C3L6	C3L5	C3L4	C3L3	C3L2	C3L1	C3L0	—	—	—
Channel-3 Warning-Alert Limit	0C	W3L12	W3L11	W3L10	W3L9	W3L8	W3L7	W3L6	W3L5	W3L4	W3L3	W3L2	W3L1	W3L0	—	—	—
Shunt-Voltage Sum	0D	SIGN	SV13	SV12	SV11	SV10	SV9	SV8	SV7	SV6	SV5	SV4	SV3	SV2	SV1	SV0	—
Shunt-Voltage Sum Limit	0E	SIGN	SVL13	SVL12	SVL11	SVL10	SVL9	SVL8	SVL7	SVL6	SVL5	SVL4	SVL3	SVL2	SVL1	SVL0	—
Mask/Enable	0F	—	SC C1	SC C2	SC C3	WEN	CEN	CF1	CF2	CF3	SF	WF1	WF2	WF3	PVF	TCF	CVRF
Power-Valid Upper Limit	10	PVU12	PVU11	PVU10	PVU9	PVU8	PVU7	PVU6	PVU5	PVU4	PVU3	PVU2	PVU1	PVU0	—	—	—

Register	ADDRESS (Hex)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Power-Valid Lower Limit	11	PVL12	PVL11	PVL10	PVL9	PVL8	PVL7	PVL6	PVL5	PVL4	PVL3	PVL2	PVL1	PVL0	—	—	—
Manufacturer ID	FE	0	1	0	1	0	1	0	1	0	1	0	0	1	0	0	1
Die ID	FF	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	0

Configuration Register (address = 00h) [reset = 7127h]

The Configuration register settings control the operating modes for the shunt- and bus-voltage measurements for the three input channels. This register controls the conversion time settings for both the shunt- and bus-voltage measurements and the averaging mode used. The Configuration register is used to independently enable or disable each channel, as well as select the operating mode that controls which signals are selected to be measured.

This register can be read from at any time without impacting or affecting either device settings or conversions in progress. Writing to this register halts any conversion in progress until the write sequence is completed, resulting in a new conversion starting, based on the new Configuration register contents. This architecture prevents any uncertainty in the conditions used for the next completed conversion.

Table 7. Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	$CH1_{en}$	$CH2_{en}$	$CH3_{en}$	AVG2	AVG1	AVG0	VBUSCT2	VBUSCT1	VBUSCT0	VSHCT2	VSHCT1	VSHCT0	MODE 3	MODE 2	MODE 1
RW-0	RW-1	RW-1	RW-1	RW-0	RW-0	RW-0	RW-1	RW-0	RW-0	RW-1	RW-0	RW-0	RW-1	RW-1	RW-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RST	R/W	0h	Reset bit. Set this bit = 1 to generate a system reset that is the same as a power-on reset (POR). This bit resets all registers to default values and self-clears.
14	$CH1_{en}$	R/W	7h	Channel enable mode. These bits allow each channel to be independently enabled or disabled. 0 = Channel disable 1 = Channel enable (default)
13	$CH2_{en}$			
12	$CH3_{en}$			
11-9	AVG2-0	R/W	0h	Averaging mode. These bits set the number of samples that are collected and averaged together. 000 = 1 (default) 001 = 4 010 = 16 011 = 64 100 = 128

Bit	Field	Type	Reset	Description
				101 = 256 110 = 512 111 = 1024
8-6	V_{BUS}CT2-0	R/W	4h	Bus-voltage conversion time. These bits set the conversion time for the bus-voltage measurement. 000 = 140 µs 001 = 204 µs 010 = 332 µs 011 = 588 µs 100 = 1.1 ms (default) 101 = 2.116 ms 110 = 4.156 ms 111 = 8.244 ms
5-3	V_{SH}CT2-0	R/W	4h	Shunt-voltage conversion time. These bits set the conversion time for the shunt-voltage measurement. The conversion-time bit settings for V_{SH}CT2-0 are the same as V_{BUS}CT2-0 (bits 8-6) listed in the previous row.
2-0	MODE3-1	R/W	7h	Operating mode. These bits select continuous, single-shot (triggered), or power-down mode of operation. These bits default to continuous shunt and bus mode. 000 = Power-down 001 = Shunt voltage, single-shot (triggered) 010 = Bus voltage, single-shot (triggered) 011 = Shunt and bus, single-shot (triggered) 100 = Power-down 101 = Shunt voltage, continuous 110 = Bus voltage, continuous 111 = Shunt and bus, continuous (default)

Channel-1 Shunt-Voltage Register (address = 01h), [reset = 00h]

This register contains the averaged shunt-voltage measurement for channel 1. This register stores the current shunt-voltage reading, V_{SHUNT}, for channel 1. Negative numbers are represented in twos complement format. Generate the twos complement of a negative number by complementing the absolute value binary number and adding 1. Extend the sign, denoting a negative number by setting MSB = 1.

Full-scale range = 163.8 mV (decimal = 7FF8); LSB (SD0): 40 µV. Example: For a value of V_{SHUNT} = –80 mV:

1. Take the absolute value: 80 mV
2. Translate this number to a whole decimal number (80 mV / 40 µV) = 2000
3. Convert this number to binary = 011 1110 1000 0_ _ _ (last three bits are set to 0)
4. Complement the binary result = 100 0001 0111 1111
5. Add 1 to the complement to create the twos complement result = 100 0001 1000 0000
6. Extend the sign and create the 16-bit word: 1100 0001 1000 0000 = C180h

Table 9. Channel-1 Shunt-Voltage Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	—	—	—

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. Channel-1 Shunt-Voltage Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit. 0 = positive number 1 = negative number in twos complement format
14-3	SD11-0	R	0h	Channel-1 shunt-voltage data bits
2-0	Reserved	R	0h	Reserved

Channel-1 Bus-Voltage Register (address = 02h) [reset = 00h]

This register stores the bus voltage reading, V_{BUS}, for channel 1. Full-scale range = 32.76 V (decimal = 7FF8); LSB (BD0) = 8 mV.

Table 11. Channel-1 Bus-Voltage Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	—	—
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. Channel-1 Bus-Voltage Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit. 0 = positive number 1 = negative number in twos complement format.
14-3	BD11-0	R	0h	Channel-1 bus-voltage data bits
2-0	Reserved	R	0h	Reserved

Channel-2 Shunt-Voltage Register (address = 03h) [reset = 00h]

This register contains the averaged shunt voltage measurement for channel 2. Full-scale range = 163.8 mV (decimal = 7FF8); LSB (SD0): 40 μV. The full-scale range of the ADC scaling is 32.76 V.

Table 13. Channel-2 Shunt-Voltage Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	—	—	—

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. Channel-2 Shunt-Voltage Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit. 0 = positive number 1 = negative number in twos complement format
14-3	SD11-0	R	0h	Channel-2 shunt-voltage data bits
2-0	Reserved	R	0h	Reserved

Channel-2 Bus-Voltage Register (address = 04h) [reset = 00h]

This register stores the bus voltage reading, V_{BUS}, for channel 2. Full-scale range = 32.76 V (decimal = 7FF8); LSB (BD0) = 8 mV. The full-scale range of the ADC scaling is 32.76 V.

Table 15. Channel-2 Bus-Voltage Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	—	—
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. Channel-2 Bus-Voltage Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit. 0 = positive number 1 = negative number in twos complement format
14-3	BD11-0	R	0h	Channel-2 bus-voltage data bits
2-0	Reserved	R	0h	Reserved

Channel-3 Shunt-Voltage Register (address = 05h) [reset = 00h]

This register contains the averaged shunt voltage measurement for channel 3. Full-scale range = 163.8 mV (decimal = 7FF8); LSB (SD0): 40 µV.

Table 17. Channel-3 Shunt-Voltage Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	—	—	—
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. Channel-3 Shunt-Voltage Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit. 0 = positive number 1 = negative number in twos complement format
14-3	SD11-0	R	0h	Channel-3 shunt-voltage data bits
2-0	Reserved	R	0h	Reserved

Channel-3 Bus-Voltage Register (address = 06h) [reset = 00h]

This register stores the bus voltage reading, V_{BUS}, for channel 3. Full-scale range = 32.76 V (decimal = 7FF8); LSB (BD0) = 8 mV. The full-scale range of the ADC scaling is 32.76 V.

Table 19. Channel-3 Bus-Voltage Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	—	—
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. Channel-3 Bus-Voltage Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit. 0 = positive number 1 = negative number in twos complement format
14-3	BD11-0	R	0h	Channel-3 bus-voltage data bits
2-0	Reserved	R	0h	Reserved

Channel-1 Critical-Alert Limit Register (address = 07h) [reset = 7FF8h]

This register contains the value used to compare to each shunt voltage conversion on channel 1 to detect fast overcurrent events.

Table 21. Channel-1 Critical-Alert Limit Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1L12	C1L11	C1L10	C1L9	C1L8	C1L7	C1L6	C1L5	C1L4	C1L3	C1L2	C1L1	C1L0	—	—	—
RW-0	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-0	RW-0	RW-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. Channel-1 Critical-Alert Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	C1L12-0	R/W	FFFh	Channel-1 critical-alert-limit data bits
2-0	Reserved	R/W	0h	Reserved

Warning-Alert Channel-1 Limit Register (address = 08h) [reset = 7FF8h]

This register contains the value used to compare to the averaged shunt voltage value of channel 1 to detect a longer duration overcurrent event.

Table 23. Channel-1 Warning-Alert Limit Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W1L12	W1L11	W1L10	W1L9	W1L8	W1L7	W1L6	W1L5	W1L4	W1L3	W1L2	W1L1	W1L0	—	—	—
RW-0	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-0	RW-0	RW-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. Channel-1 Warning-Alert Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	W1L12-0	R/W	FFFh	Channel-1 warning-alert-limit data bits
2-0	Reserved	R/W	0h	Reserved

Channel-2 Critical-Alert Limit Register (address = 09h) [reset = 7FF8h]

This register contains the value used to compare to each shunt voltage conversion on channel 2 to detect fast overcurrent events.

Table 25. Channel-2 Critical-Alert Limit Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2L12	C2L11	C2L10	C2L9	C2L8	C2L7	C2L6	C2L5	C2L4	C2L3	C2L2	C2L1	C2L0	—	—	—

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW-0	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-0	RW-0	RW-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. Channel-2 Critical-Alert Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	C2L12-0	R/W	FFFh	Channel-2 critical-alert-limit data bits
2-0	Reserved	R/W	0h	Reserved

Channel-2 Warning-Alert Limit Register (address = 0Ah) [reset = 7FF8h]

This register contains the value used to compare to the averaged shunt voltage value of channel 2 to detect a longer duration overcurrent event.

Table 27. Warning-Alert Limit Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W2L12	W2L11	W2L10	W2L9	W2L8	W2L7	W2L6	W2L5	W2L4	W2L3	W2L2	W2L1	W2L0	—	—	—
RW-0	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-0	RW-0	RW-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. Channel-2 Warning-Alert Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	W2L12-0	R/W	FFFh	Channel-2 warning-alert-limit data bits
2-0	Reserved	R/W	0h	Reserved

Channel-3 Critical-Alert Limit Register (address = 0Bh) [reset = 7FF8h]

This register contains the value used to compare to each shunt voltage conversion on channel 3 to detect fast overcurrent events.

Table 29. Channel-3 Critical-Alert Limit Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C3L12	C3L11	C3L10	C3L9	C3L8	C3L7	C3L6	C3L5	C3L4	C3L3	C3L2	C3L1	C3L0	—	—	—
RW-0	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-0	RW-0	RW-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 30. Channel-3 Critical-Alert Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	C3L12-0	R/W	FFFh	Channel-3 critical-alert-limit data bits
2-0	Reserved	R/W	0h	Reserved

Channel-3 Warning-Alert Limit Register (address = 0Ch) [reset = 7FF8h]

This register contains the value used to compare to the averaged shunt voltage value of channel 3 to detect a longer duration overcurrent event.

Table 31. Channel-3 Warning-Alert Limit Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W3L12	W3L11	W3L10	W3L9	W3L8	W3L7	W3L6	W3L5	W3L4	W3L3	W3L2	W3L1	W3L0	—	—	—
RW-0	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-0	RW-0	RW-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 32. Channel-3 Warning-Alert Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	W3L12-0	R/W	FFFh	Channel-3 warning-alert limit data bits
2-0	Reserved	R/W	0h	Reserved

Shunt-Voltage Sum Register (address = 0Dh) [reset = 00h]

This register contains the sum of the single conversion shunt voltages of the selected channels based on the summation control bits 12, 13, and 14 in the Mask/Enable register.

This register is updated with the most recent sum following each complete cycle of all selected channels. The Shunt-Voltage Sum register LSB value is 40 μV.

Table 33. Shunt-Voltage Sum Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	SV13	SV12	SV11	SV10	SV9	SV8	SV7	SV6	SV5	SV4	SV3	SV2	SV1	SV0	—
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. Shunt-Voltage Sum Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit.

Bit	Field	Type	Reset	Description
				0 = positive number 1 = negative number in twos complement format
14-1	SV13-0	R	0h	Shunt-voltage sum data bits
0	Reserved	R	0h	Reserved

Shunt-Voltage Sum-Limit Register (address = 0Eh) [reset = 7FFEh]

This register contains the value that is compared to the Shunt-Voltage Sum register value following each completed cycle of all selected channels to detect system overcurrent events. The Shunt-Voltage Sum-Limit register LSB value is 40 μV.

Table 35. Shunt-Voltage Sum-Limit Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	SVL13	SVL12	SVL11	SVL10	SVL9	SVL8	SVL7	SVL6	SVL5	SVL4	SVL3	SVL2	SVL1	SVL0	—
RW-0	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-1	RW-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 36. Shunt-Voltage Sum-Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit. 0 = positive number 1 = negative number in twos complement format
14-1	SVL13-0	R	0h	Shunt-voltage sum-limit data bits
0	Reserved	R	0h	Reserved

Mask/Enable Register (address = 0Fh) [reset = 0002h]

This register selects which function is enabled to control the Critical alert and Warning alert pins, and how each warning alert responds to the corresponding channel. Read the Mask/Enable register to clear any flag results present. Writing to this register does not clear the flag bit status. To make sure that there is no uncertainty in the warning function setting that resulted in a flag bit being set, the Mask/Enable register should be read from to clear the flag bit status before changing the warning function setting.

Table 37. Mask/Enable Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	SCC1	SCC2	SCC3	WEN	CEN	CF1	CF2	CF3	SF	WF1	WF2	WF3	PVF	TCF	CVRF
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-1	RW-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 38. Mask/Enable Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0h	Reserved
14-12	SCC1-3	R/W	0h	Summation channel control. These bits determine which shunt voltage measurement channels are enabled to fill the Shunt-Voltage Sum register. The selection of these bits does not impact the individual channel enable or disable status, or the corresponding channel measurements. The corresponding bit is used to select if the channel is used to fill the Shunt-Voltage Sum register. 0 = Disabled (default) 1 = Enabled
11	WEN	R/W	0h	Warning alert latch enable. These bits configure the latching feature of the Warning alert pin. 0 = Transparent (default) 1 = Latch enabled
10	CEN	R/W	0h	Critical alert latch enable. These bits configure the latching feature of the Critical alert pin. 0 = Transparent (default) 1 = Latch enabled
9-7	CF1-3	R/W	0h	Critical-alert flag indicator. These bits are asserted if the corresponding channel measurement has exceeded the critical alert limit resulting in the Critical alert pin being asserted. Read these bits to determine which channel caused the critical alert. The critical alert flag bits are cleared when the Mask/Enable register is read back.
6	SF	R/W	0h	Summation-alert flag indicator. This bit is asserted if the Shunt Voltage Sum register exceeds the Shunt Voltage Sum Limit register. If the summation alert flag is asserted, the Critical alert pin is also asserted. The Summation Alert Flag bit is cleared when the Mask/Enable register is read back.
5-3	WF1-3	R/W	0h	Warning-alert flag indicator. These bits are asserted if the corresponding channel averaged measurement has exceeded the warning alert limit, resulting in the Warning alert pin being asserted. Read these bits to determine which channel caused the warning alert. The Warning Alert Flag bits clear when the Mask/Enable register is read back.
2	PVF	R/W	0h	Power-valid-alert flag indicator. This bit can be used to be able to determine if the power valid (PV) alert pin has been asserted through software rather than hardware. The bit setting corresponds to the

Bit	Field	Type	Reset	Description
				status of the PV pin. This bit does not clear until the condition that caused the alert is removed, and the PV pin has cleared.
1	TCF	R/W	11h	Timing-control-alert flag indicator. Use this bit to determine if the timing control (TC) alert pin has been asserted through software rather than hardware. The bit setting corresponds to the status of the TC pin. This bit does not clear after it has been asserted unless the power is recycled or a software reset is issued. The default state for the timing control alert flag is high.
0	CVRF	R/W	0h	Conversion-ready flag. Although the device can be read at any time, and the data from the last conversion is available, the conversion-ready bit is provided to help coordinate single-shot conversions. The conversion bit is set after all conversions are complete. Conversion ready clears under the following conditions: 1. Writing the Configuration register (except for power-down or disable-mode selections). 2. Reading the Mask/Enable register.

Power-Valid Upper-Limit Register (address = 10h) [reset = 2710h]

This register contains the value used to determine if the power-valid conditions are met. The power-valid condition is reached when all bus-voltage channels exceed the value set in this limit register. When the power-valid condition is met, the PV alert pin asserts high to indicate that the device has confirmed all bus voltage channels are above the power-valid upper-limit value. In order for the power-valid conditions to be monitored, the bus measurements must be enabled through one of the corresponding MODE bits set in the Configuration register. The power-valid upper-limit LSB value is 8 mV. Power-on reset value is 2710h = 10.000 V.

Table 39. Power-Valid Upper-Limit Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	PVU11	PVU10	PVU9	PVU8	PVU7	PVU6	PVU5	PVU4	PVU3	PVU2	PVU1	PVU0	—	—	—
RW-0	RW-0	RW-1	RW-0	RW-0	RW-1	RW-1	RW-1	RW-0	RW-0	RW-0	RW-1	RW-0	RW-0	RW-0	RW-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 40. Power-Valid Upper-Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R/W	0h	Sign bit. 0 = positive number 1 = negative number in twos complement format
14-3	PVU11-0	R/W	4E2h	Power-valid upper-limit data bits

Bit	Field	Type	Reset	Description
2-0	Reserved	R/W	0h	Reserved

Power-Valid Lower-Limit Register (address = 11h) [reset = 2328h]

This register contains the value used to determine if any of the bus-voltage channels drops below the power-valid lower-limit when the power-valid conditions are met. This limit contains the value used to compare all bus- channel readings to make sure that all channels remain above the power-valid lower-limit, thus maintaining the power-valid condition. If any bus-voltage channel drops below the power-valid lower-limit, the PV alert pin pulls low to indicate that the device detects a bus voltage reading below the power-valid lower-limit. In order for the power-valid condition to be monitored, the bus measurements must be enabled through the mode (MODE3-1) bits set in the Configuration register. The power-valid lower-limit LSB value is 8 mV. Power-on reset value is 2328h = 9.000 V.

Table 41. Power-Valid Lower-Limit Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	PVL11	PVL10	PVL9	PVL8	PVL7	PVL6	PVL5	PVL4	PVL3	PVL2	PVL1	PVL0	—	—	—
RW-0	RW-0	RW-1	RW-0	RW-0	RW-0	RW-1	RW-1	RW-0	RW-0	RW-1	RW-0	RW-1	RW-0	RW-0	RW-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 42. Power-Valid Lower-Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R/W	0h	Sign bit. 0 = positive number 1 = negative number in twos complement format
14-3	PVL11-0	R/W	465h	Power-valid lower-limit data bits
2-0	Reserved	R/W	0h	Reserved

Manufacturer ID Register (address = FEh) [reset = 5549h]

This register contains a factory-programmable identification value that identifies this device as being manufactured by Texas Instruments. This register distinguishes this device from other devices that are on the same I²C bus. The contents of this register are 5549h.

Table 43. Manufacturer ID Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R-0	R-1	R-0	R-1	R-0	R-1	R-0	R-1	R-0	R-1	R-0	R-0	R-1	R-0	R-0	R-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 44. Manufacturer ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	D15-0	R	5549h	Manufacturer ID bits

Die ID Register (address = FFh) [reset = 3220]

This register contains a factory-programmable identification value that identifies this device as a device. This register distinguishes this device from other devices that are on the same I²C bus. The Die ID for the device is 3220h.

Table 45. Die ID Register

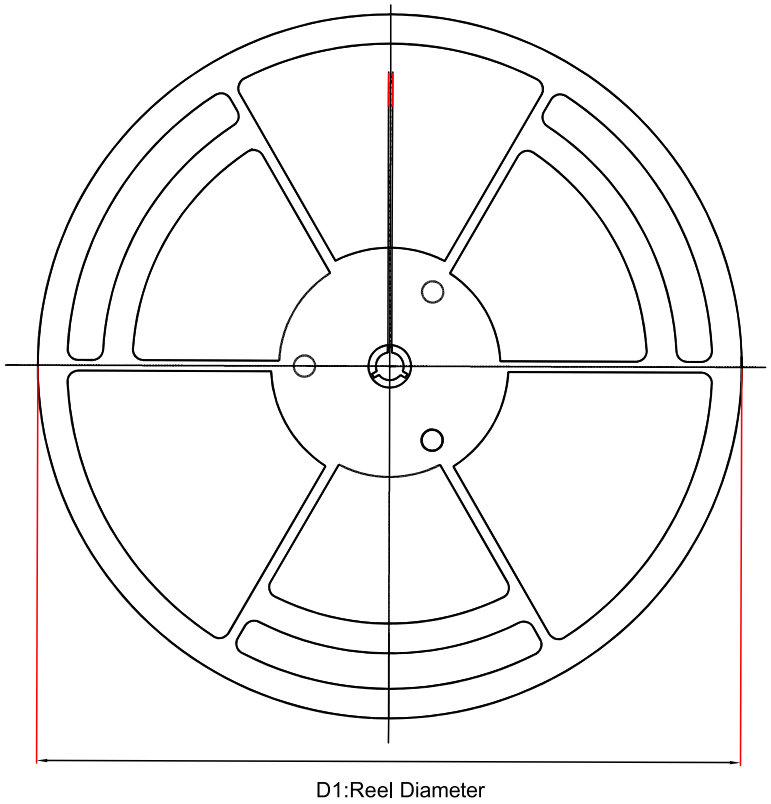
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R-0	R-0	R-1	R-1	R-0	R-0	R-1	R-0	R-0	R-0	R-1	R-0	R-0	R-0	R-0	R-0

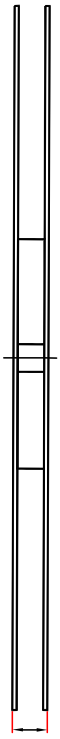
LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

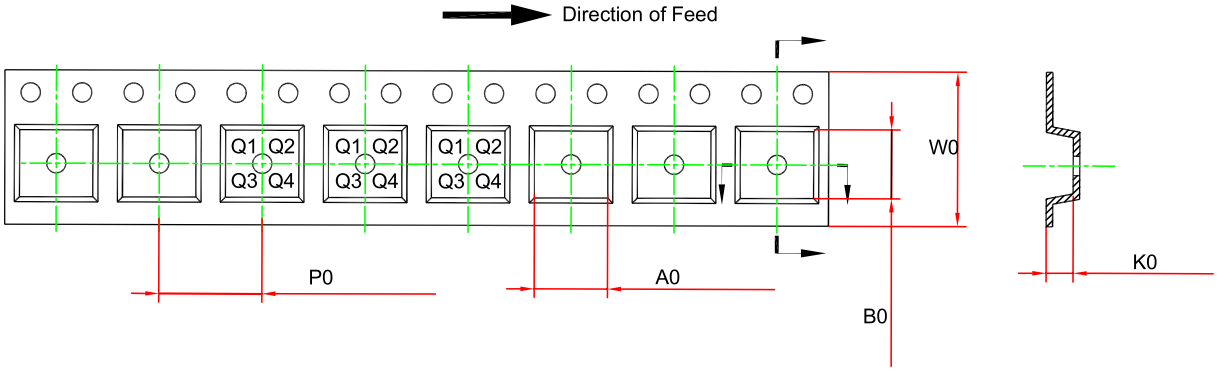
Table 46. Die ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	D15-0	R	3220h	Die ID bits

Tape and Reel Information





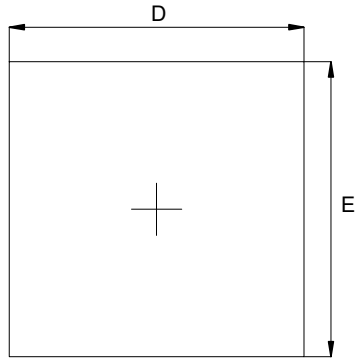


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPA6290-QFPR	QFN4X4-16	330	17.6	4.3	4.3	1.1	8	12	Q2

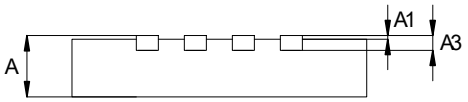
Package Outline Dimensions

QFN4X4-16

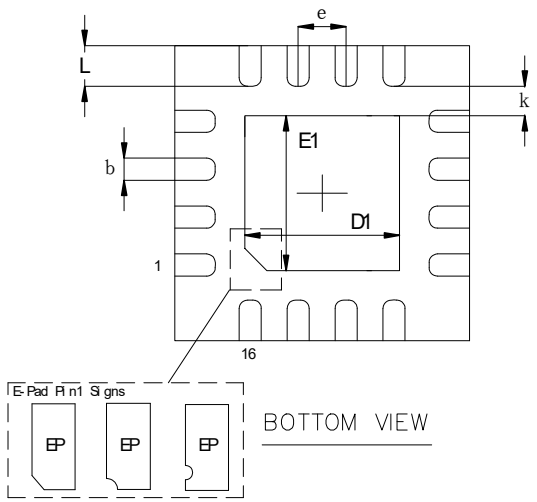
Package Outline Dimensions QFP(QFN4X4-16-D)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203 REF		0.008 REF	
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
e	0.650 BSC		0.030 BSC	
b	0.250	0.350	0.010	0.013
L	0.450	0.650	0.018	0.026
D1	2.000	2.200	0.079	0.087
E1	2.000	2.200	0.079	0.087
K	0.200 MIN		0.008 MIN	

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPA6290-QFPR	−40 to 125°C	QFN4X4-16	6290	2	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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