Bi-Directional Current and Power Monitor

Features

- Senses Bus Voltages from 0 V to 36 V
- High-Side or Low-Side Sensing
- Reports Current, Voltage, and Power
- High Accuracy
- Configurable Averaging Options
- 16 Programmable Addresses
- Operates from 2.7-V to 5.5-V Power Supply
- MSOP10 Package

Applications

- Power Management
- Servers
- Telecom Equipment
- Computing
- Test Equipment

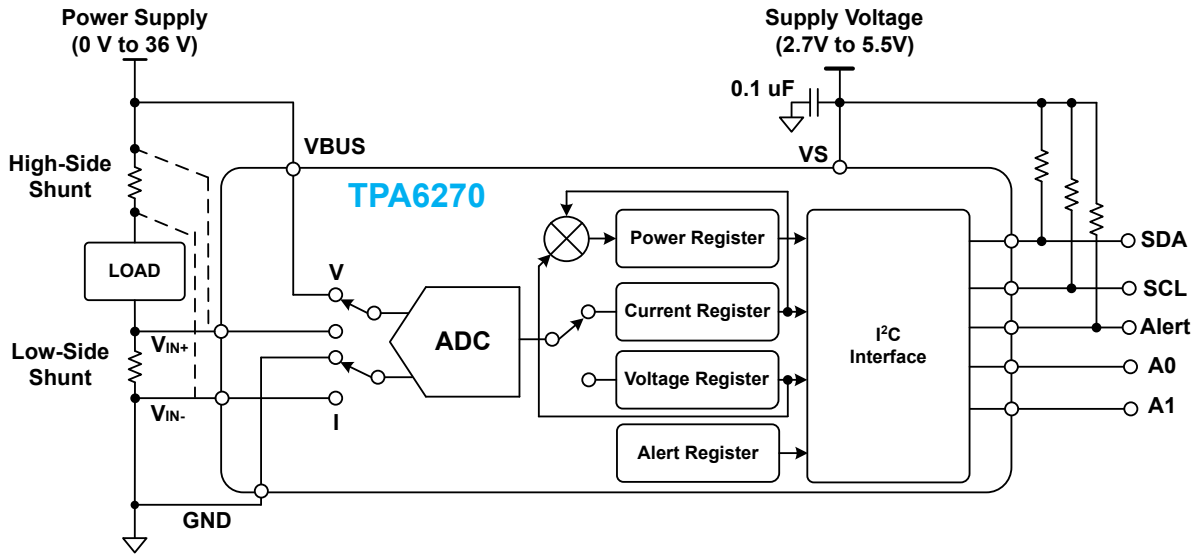
Description

The TPA6270X is a current and power monitor, with I^2C or SMBUS-compatible interface. The device monitors both a shunt voltage drop and bus supply voltage.

The TPA6270X input voltage can vary from 0 V to 36 V.

The TPA6270X features up to 16 programmable addresses on the I^2C-compatible interface.

Typical Application Circuit



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Revision History

Date	Revision	Notes
2024-02-20	Rev.A.0	Initial version.
2024-11-12	Rev.A.1	Corrected Die ID information, and added Timing Characteristics and Timing Diagram.
2025-09-16	Rev.A.2	Added Feature Description, Device Functional Modes, Programming, Power Supply Recommendations and Layout. The actual product remains unchanged.

Pin Configuration and Functions

TPA6270X
MSOP10 Package
Top View

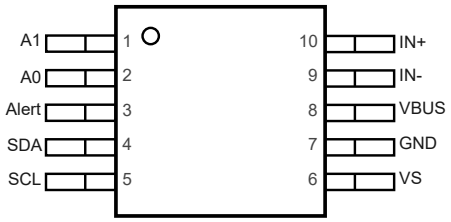


Table 1. Pin Functions: TPA6270X

Pin No.	Name	I/O	Description
2	A0	Digital input	Address pin. Connect to GND, SCL, SDA, or VS.
1	A1	Digital input	Address pin. Connect to GND, SCL, SDA, or VS.
3	Alert	Digital output	Multi-functional alert, open-drain output.
7	GND	Analog	Ground.
10	IN+	Analog input	Connect to the supply side of the shunt resistor.
9	IN–	Analog input	Connect to the load side of the shunt resistor.
5	SCL	Digital input	Serial bus clock line, open-drain input.
4	SDA	Digital I/O	Serial bus data line, open-drain input/output.
8	VBUS	Analog input	Bus voltage input.
6	VS	Analog	Power supply, 2.7 V to 5.5 V.

Specifications

Absolute Maximum Ratings

Cover operating free-air temperature range (unless otherwise noted) (1)

Parameter		Min	Max	Unit
V_{VS}	Supply Voltage		6	V
Analog Inputs, IN+, IN–	Differential (VIN+ – VIN-) (2)	–40	40	V
	Common-Mode (VIN+ + VIN-) / 2	–0.3	40	
V_{VBUS}		–0.3	40	V
V_{SDA}		GND – 0.3	6	V
V_{SCL}		GND – 0.3	VVS + 0.3	V
I_{IN}	Input Current into any Pin		5	mA
I_{OUT}	Open-Drain Digital Output Current		10	mA
T_J	Junction Temperature		150	°C
T_{stg}	Storage Temperature Range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) IN+ and IN– may have a differential voltage between –40 V and 40 V. However, the voltage at these pins must not exceed the range from −0.3 V to 40 V.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1), all pins	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2), all pins	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions (1)

Parameter		Min	Typ	Max	Unit
V_{CM}	Common Mode Input Voltage		12		V
V_{VS}	Operating Supply Voltage		3.3		V
T_A	Operating Free-Air Temperature	−40		125	℃

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
MSOP10	171	42.9	°C/W

Electrical Characteristics

All test conditions: T_A = 25°C, V_{VS} = 3.3 V, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0 mV, and V_{VBUS} = 12 V, unless otherwise noted.

Parameter		Test conditions	Min	Typ	Max	Unit
INPUT						
	Shunt Voltage Input Range		–81.9175		81.92	mV
	Bus Voltage Input Range (1)		0		36	V
CMRR	Common-Mode Rejection	0 V ≤ VIN+ ≤ 36 V	120	140		dB
V_{OS}	Shunt Offset Voltage, RTI (2)			±2.5	±10	μV
	Shunt Offset Voltage, RTI (2) vs. Temperature	–40°C ≤ TA ≤ 125°C		0.025		μV/°C
PSRR	Shunt Offset Voltage, RTI (2) vs. Power Supply	2.7 V ≤ VS ≤ 5.5 V		5		μV/V
V_{OS}	Bus Offset Voltage, RTI (2)			±1.25	±5	mV
	Bus Offset Voltage, RTI (2) vs. Temperature	–40°C ≤ TA ≤ 125°C		5		μV/°C
PSRR	Bus Offset Voltage, RTI (2) vs. Power Supply	2.7 V ≤ VS ≤ 5.5 V		0.1		mV/V
I_B	Input Bias Current			10		μA
	VBUS Input Impedance			830		kΩ
	Input Leakage (3)	(IN+ pin) + (IN– pin), Power-down mode		1		μA
DC ACCURACY						
	ADC Native Resolution			16		Bits
	1 LSB Step Size	Shunt voltage		2.5		μV
		Bus voltage		1.25		mV
	Shunt Voltage Gain Error			0.02%	0.15%	
	Shunt Voltage Gain Error Vs Temperature	–40°C ≤ TA ≤ 125°C		10		ppm/°C
	Shunt Voltage Linearity			1		LSB
	Bus Voltage Gain Error			0.02%	0.15%	
	Bus Voltage Gain Error vs Temperature	–40°C ≤ TA ≤ 125°C		10		ppm/°C
	Bus Voltage Linearity			1		LSB
t_{CT}	ADC Conversion Time	CT bit = 000		140		μs
		CT bit = 001		204		
		CT bit = 010		332		
		CT bit = 011		588		

Parameter		Test conditions	Min	Typ	Max	Unit
		CT bit = 100		1100		µs
		CT bit = 101		2116		
		CT bit = 110		4156		
		CT bit = 111		8244		
SMBus						
	SMBus Timeout (4)			28		ms

Digital Input/Output						
	Input Capacitance			3		pF
	Leakage Input Current	0 V ≤ VSCL ≤ VVS , 0 V ≤ VSDA ≤ VVS, 0 V ≤ VAlert ≤ VVS , 0 V ≤ VA0 ≤ VVS , 0 V ≤ VA1 ≤ VVS		0.1		µA
V_{IH}	High-Level Input Voltage		0.7×VVS			V
V_{IL}	Low-Level Input Voltage				0.3×VVS	V
V_{OL}	Low-Level Output Voltage, SDA, Alert		0		0.4	V
	Hysteresis			150		mV
Power Supply						
	Operating Supply Range		2.7		5.5	V
IQ	Quiescent Current			600	950	µA
	Quiescent Current, Power-Down (Shutdown) Mode			2	20	µA
V_{POR}	Operating Supply Range			2.2		V

(1) While the input range is 36 V, the full-scale range of the ADC scaling is 40.96 V.
(2) RTI = Referred-to-input.
(3) Input leakage is positive (current flowing into the pin) for the conditions shown at the top of this table. Negative leakage currents can occur under different input conditions.
(4) SMBus timeout in the TPA6270X resets the interface any time SCL is low for more than 28 ms.
(5) Test Levels: (A) Tested at final test. Over-temperature limits are set by characterization and simulation. (B) Set by characterization and simulation. (C) Typical value only for information, provided by design simulation.

Timing Characteristics

All test conditions: T_A = 25°C, V_{VS} = 3.3 V unless otherwise noted.

Symbol	Parameter	Fast Mode		High-Speed Mode		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency	0.001	0.4	0.001	2.94	MHz
t_{LOW}	SCL Low Period	1300		200		ns
t_{HIGH}	SCL High Period	600		60		ns
t_R	SCL Rise Time		300		40	ns
	SCL/SDA Rise Time for SCLK ≤ 100 kHz		1000		40	
t_F	SCL Fall Time		300		40	ns
	SDA Fall Time		300		80	
t_{SU_DAT}	Data Setup Time	100		20		ns
t_{HD_DAT}	Data Hold Time	10	900	10	100	ns
t_{SU_STA}	Setup Time for a Repeated START Condition	100		100		ns
t_{HD_STA}	Hold Time for a (Repeated) START Condition	100		100		ns
t_{SU_STO}	Setup Time for a STOP Condition	100		100		ns
t_{BUF}	Bus Free Time (Time between the STOP and START Conditions)	600		160		ns

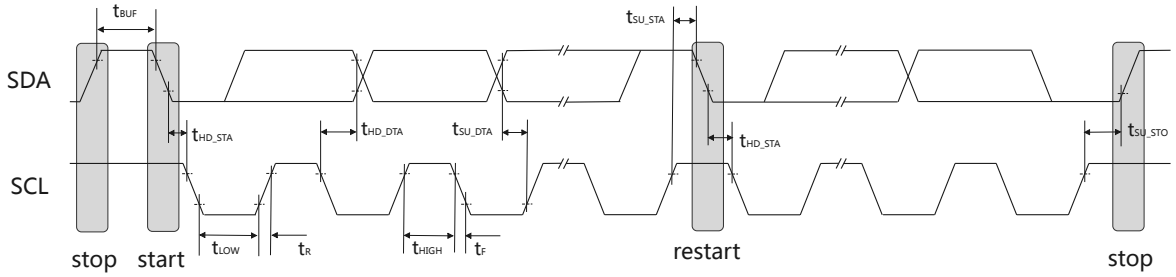


Figure 1. Timing Diagram

Typical Performance Characteristics

All test conditions: T_A = 25°C, V_{VS} = 3.3 V, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0 mV and V_{VBUS} = 12 V, unless otherwise noted.

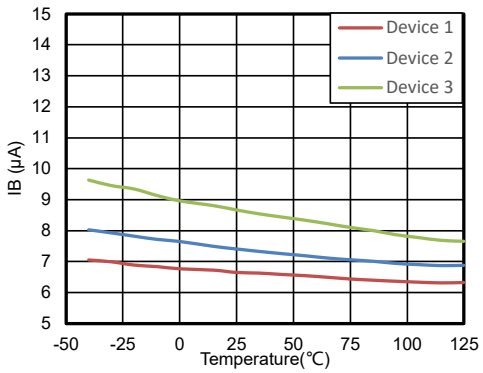


Figure 2. Ib vs. Temp

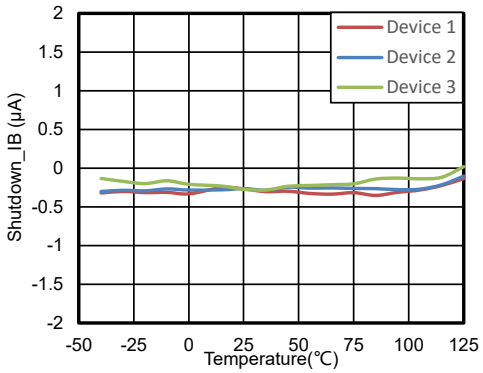


Figure 3. Shutdown Ib vs. Temp

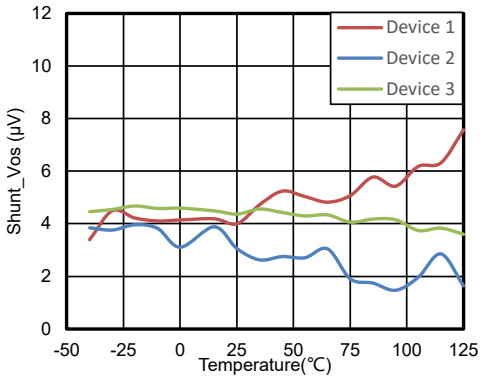


Figure 4. Shunt Vos vs. Temp

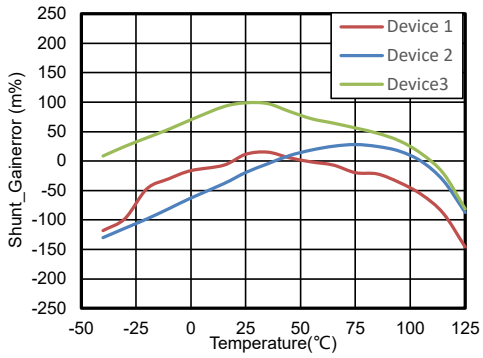


Figure 5. Shunt Gain vs. Temp

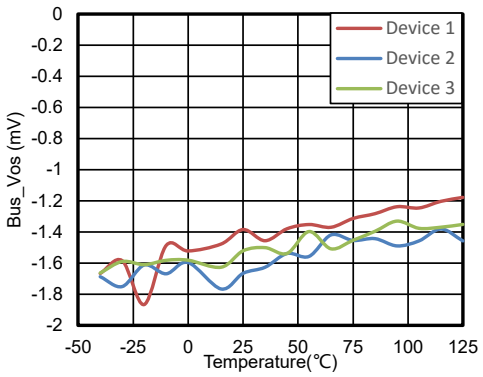


Figure 6. Bus Vos vs. Temp

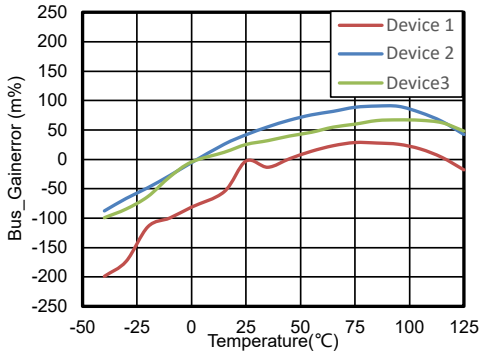


Figure 7. Bus Gain vs. Temp

Detailed Description

Overview

The TPA6270X is a digital current sense amplifier with an I^2C- and SMBus-compatible interface. It performs two measurements on the power-supply bus: The differential shunt voltage created by load current flowing through a shunt resistor measured at the IN+ and IN– pins. The power supply bus voltage is measured at the VBUS pin.

There is no special requirement for power supply sequencing since power supply and input voltages are independent of each other.

Functional Block Diagram

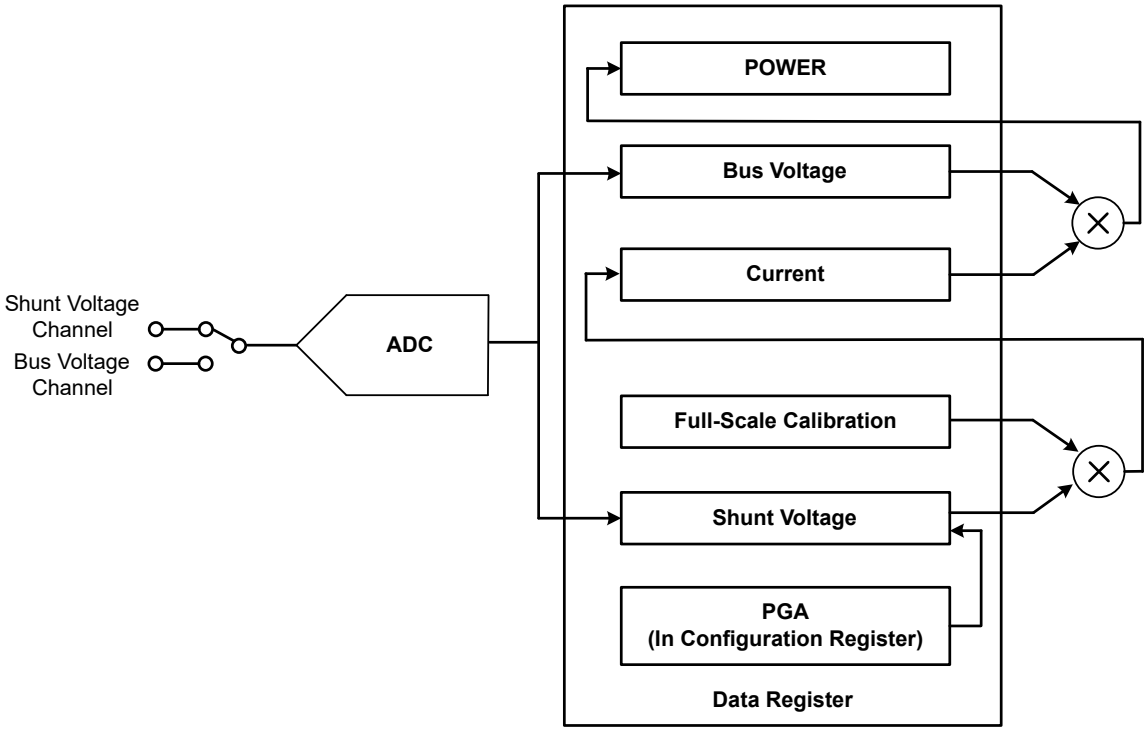


Figure 8. Functional Block Diagram

Feature Description

Basic ADC Functions

The TPA6270X performs two measurements on the target power-supply bus. The load current flowing through a shunt resistor develops a voltage, which forms a shunt voltage measured at the IN+ and IN– pins. Additionally, the device can measure the power-supply bus voltage by connecting this voltage to the VBUS pin. Specifically, the differential shunt voltage is measured relative to the IN– pin, while the bus voltage is measured relative to ground (GND).

The TPA6270X is typically powered by a separate supply, with a voltage range of 2.7 V to 5.5 V. The monitored bus voltage can range from 0 V to 36 V.

The device performs two measurements: shunt voltage and bus voltage. It then converts these measurements into current based on the value of the Calibration Register, and then calculates the power.

The device has two operating modes, continuous and triggered, that determine how the ADC operates following these conversions.

When in normal operating mode (i.e., the MODE bits of the Configuration Register (00h) are set to '111'), the device continuously converts a shunt voltage reading followed by a bus voltage reading. After the shunt voltage is read, a current value is calculated (using Equation 3), and this current value is then used to compute the power result (using Equation 4). These values are stored in an accumulator, and the measurement/calculation sequence repeats until the number of averages set in the Configuration Register (00h) is achieved. After each sequence, the currently measured and calculated values are appended to previously collected data. Once all averaging is completed, the final values for shunt voltage, bus voltage, current, and power are updated in their respective registers, which can then be read. These values remain in the data output registers until replaced by the next fully completed conversion results. Reading the data output registers does not interfere with an ongoing conversion.

The mode control in the Conversion Register (00h) also permits selecting modes to convert only the shunt voltage or the bus voltage to further allow the user to configure the monitoring function to fit the specific application requirements.

All current and power calculations are performed in the background and do not consume conversion time.

In triggered mode, writing any triggered conversion mode into the Configuration Register (00h) (i.e., the MODE bits of the Configuration Register (00h) are set to ‘001’, ‘010’, or ‘011’) triggers a single-shot conversion. This action generates one set of measurement data; therefore, to trigger another single-shot conversion, the Configuration Register (00h) must be written to a second time—even if the mode remains unchanged.

In addition to the two operating modes (continuous and triggered), the device also includes a power-down mode. This mode reduces quiescent current and turns off current into the device inputs, minimizing the impact of power drain when the device is not in use. The registers of the device can still be read from and written to while in power-down mode. The device remains in power-down mode until one of the active mode settings is written into the Configuration Register (00h).

Although the device can be read at any time and data from the last conversion remains available, a Conversion Ready flag bit (Mask/Enable Register, CVRF bit) is provided to assist in coordinating single-shot or triggered conversions. The Conversion Ready flag (CVRF) bit is set high once all conversions, averaging, and multiplication operations are completed.

The Conversion Ready flag (CVRF) bit clears under these conditions:

- Writing to the Configuration Register(00h), except when configuring the MODE bits for power-down mode
- Reading the Mask/Enable Register(06h)

Power Calculation

Current and power are calculated after measuring the shunt voltage and bus voltage, as illustrated in Figure 9. Specifically, current is computed following a shunt voltage measurement, based on the value set in the Calibration Register. If no value is loaded into the Calibration Register, the stored current value will be zero. Power is calculated after a bus voltage measurement, using the previously computed current value and the currently measured bus voltage value. Similarly, if no

value is loaded into the Calibration Register, the stored power value will also be zero. It should be noted again that these calculations are performed in the background and do not increase the overall conversion time. These current and power values are regarded as intermediate results (unless the number of averages is set to 1) and are stored in an internal accumulation register rather than the corresponding output registers. After each sample is measured, the newly calculated current and power values are appended to this accumulation register. This process continues until all samples have been measured and averaged in accordance with the number of averages set in the Configuration Register (00h).

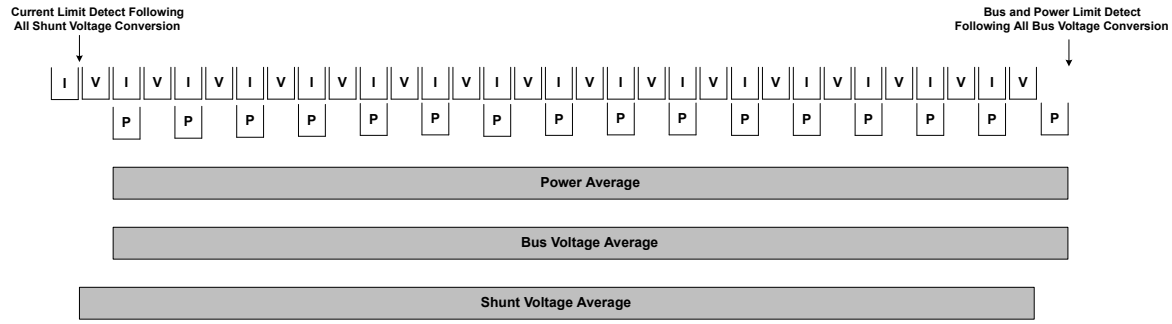


Figure 9. Power Calculation Scheme

In addition to the current and power accumulating after every sample, the shunt and bus voltage measurements are also collected. After all of the samples have been measured and the corresponding current and power calculations have been made, the accumulated average for each of these parameters is then loaded to the corresponding output registers, where the average can then be read.

Alert Pin

The TPA6270X is equipped with a single Alert Limit Register (07h), which enables programming of the Alert pin to respond to either a single user-defined event or a Conversion Ready notification, depending on the user's needs. The Mask/Enable Register allows the user to select one of the five available functions for monitoring and/or set the Conversion Ready bit to control how the Alert pin responds. Based on the function being monitored, the user then inputs a value into the Alert Limit Register to set the corresponding threshold—once this threshold is reached, the Alert pin is asserted.

The Alert pin allows for one of several available alert functions to be monitored to determine if a user-defined threshold has been exceeded. The five alert functions that can be monitored are:

- Shunt Voltage Over-Limit (SOL)
- Shunt Voltage Under-Limit (SUL)
- Bus Voltage Over-Limit (BOL)
- Bus Voltage Under-Limit (BUL)
- Power Over-Limit (POL)

The Alert pin is an open-drain output. This pin is asserted when the alert function selected in the Mask/Enable Register exceeds the value programmed into the Alert Limit Register. Only one of these alert functions can be enabled and monitored simultaneously. If multiple alert functions are enabled, the function selected at the highest significant bit position takes priority and is the only one that responds to the value in the Alert Limit Register. For example, if both the Shunt Voltage Over-Limit function and the Shunt Voltage Under-Limit function are selected, the Alert pin is asserted when the value in the Shunt Voltage Register exceeds the value stored in the Alert Limit Register.

The device's Conversion Ready state can also be monitored via the Alert pin to notify the user when the device has completed the previous conversion and is ready to start a new one. The Conversion Ready state can be monitored through the Alert pin alongside any one of the alert functions. If both an alert function and the Conversion Ready state are configured to be monitored via the Alert pin, after the Alert pin is asserted, the Mask/Enable Register must be read post-alert to identify the source of the alert. The alert source can be determined by reading the Conversion Ready Flag (CVRF, bit 3) and the Alert

Function Flag (AFF, bit 4) in the Mask/Enable Register. If the Conversion Ready feature is not required and the CNVR bit is not set, the Alert pin only responds to the exceeded limit condition associated with the enabled alert function.

If the alert function is not in use, the Alert pin can be left floating.

Refer to Figure 9 to get the relative timing of the comparison between the value in the Alert Limit Register and the corresponding converted value. For example, if the enabled alert function is Shunt Voltage Over-Limit (SOL), after each shunt voltage conversion with average, the value in the Alert Limit Register is compared with the measured shunt voltage to check if the measured value exceeds the programmed limit. Whenever the measured voltage exceeds the value programmed into the Alert Limit Register, bit 4 (the AFF bit) of the Mask/Enable Register is set high. In addition to the assertion of the AFF bit, whether the Alert pin is asserted depends on the setting of the Alert Polarity Bit (APOL, bit 1 of the Mask/Enable Register). If the Alert Latch feature is enabled, the AFF bit and the Alert pin remain asserted until data is written to the Configuration Register (00h) or the Mask/Enable Register is read.

The Bus Voltage-related alert functions compare the measured bus voltage with the value in the Alert Limit Register after each bus voltage conversion with average. If the limit threshold is exceeded, the AFF bit is set and the Alert pin is asserted.

The Power Over-Limit alert function compares the calculated power value with the value in the Alert Limit Register after each bus voltage measurement conversion with average. If the limit threshold is exceeded, the AFF bit is set and the Alert pin is asserted.

Device Functional Modes

Averaging and Conversion Time Considerations

The TPA6270X provides programmable conversion times (t_{CT}) for both shunt voltage and bus voltage measurements. When combined with the programmable averaging mode, the conversion time settings allow the device to be configured to optimize the available timing requirements in a specific application. Additionally, the device can be configured with different conversion time settings for shunt voltage and bus voltage measurements—a common approach in applications where the bus voltage remains relatively stable. In such cases, the time allocated to bus voltage measurement can be reduced compared to that for shunt voltage measurement.

There are trade-offs between the conversion time settings and the averaging mode used. The averaging feature can significantly enhance measurement accuracy by effectively filtering the signal, which helps reduce measurement noise caused by noise coupling into the signal. A higher number of averages enables the device to more effectively suppress the noise component in the measurement.

The selected conversion times also have an impact on measurement accuracy.

Filtering and Input Considerations

Measuring current is often noisy, and such noise can be difficult to define. The TPA6270X provides multiple filtering options through the selection of resolution and averaging modes in the Configuration Register. These filtering options can be configured independently for either voltage measurement or current measurement.

The internal ADC is based on a delta-sigma (ΔΣ) front-end with a 1 MHz (±30%) typical sampling rate. This architecture has good inherent noise rejection; however, transients that occur at or very close to the sampling rate harmonics can cause problems. Since these interfering signals operate at frequencies of 1 MHz and above, they can be mitigated by integrating filtering circuitry at the input of the TPA6270X. The high frequency enables the use of low-value series resistors on the filter for negligible effects on measurement accuracy. Filter using the lowest possible series resistance and ceramic capacitor. Recommended values are 0.1 to 1 μF. Figure 10 shows the TPA6270X with an additional filter added at the input.

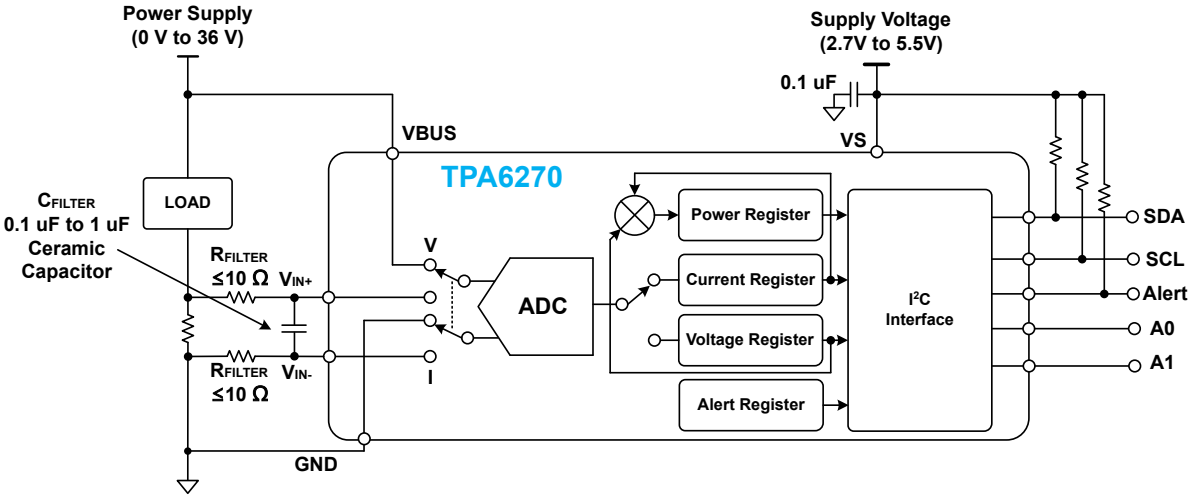


Figure 10. Input Filtering

Overload conditions represent an additional consideration for the TPA6270X inputs. A large differential scenario might be a short to ground on the load side of the shunt. This type of event can result in full power-supply voltage across the shunt (as long the power supply or energy storage capacitors support it). It must be remembered that removing a short to ground can result in inductive kickbacks that could exceed the differential and common-mode rating of the TPA6270X. The most effective approach to mitigating inductive kickback voltages involves the use of zener-type transient-absorbing devices, combined with energy storage capacitors of sufficient capacitance.

In applications that do not have large energy storage electrolytics on one or both sides of the shunt, an input overstress condition may result from an excessive dV/dt of the voltage applied to the input. A hard physical short circuit is the most probable cause of this issue—especially in setups that lack large electrolytic capacitors, where the problem becomes more noticeable. This problem occurs because an excessive dV/dt can activate the ESD protection in the TPA6270X in systems where large currents are available. Tests have shown that connecting a 10 Ω resistor in series with each input terminal of the TPA6270X provides sufficient protection for its input terminals against voltage slew rate (dV/dt) failure. These resistors have no significant impact on measurement accuracy.

Programming

An important feature of the TPA6270X device is that it can perform current or power measurement if programmed according to system requirements. The device measures both the differential voltage applied between the IN+ and IN- input pins and the voltage applied to the VBUS pin. For the device to report both current and power values, the user must program the resolution of the Current Register (04h) and the value of the shunt resistor present in the application to develop the differential voltage applied between the input pins. The Power Register (03h) is internally set to be 25 times the programmed Current_LSB. Both the Current_LSB and shunt resistor value are used in the calculation of the Calibration Register value that the device uses to calculate the corresponding current and power values based on the measured shunt and bus voltages.

After programming the Calibration Register, the Current Register (04h) and Power Register (03h) update accordingly based on the corresponding shunt voltage and bus voltage measurements. Until the Calibration Register is programmed, the Current Register (04h) and Power Register (03h) remain at zero.

Programming the Calibration Register

The Calibration Register is calculated based on Equation 1. This equation includes the term Current_LSB, which is the programmed value for the LSB for the Current Register (04h). The user uses this value to convert the value in the Current Register (04h) to the actual current in amperes. The highest resolution for the Current Register (04h) can be obtained by using the smallest allowable Current_LSB based on the maximum expected current as shown in Equation 2. While this value yields the highest resolution, it is common to select a value for the Current_LSB to the nearest round number above this

value to simplify the conversion of the Current Register (04h) and Power Register (03h) to amperes and watts respectively. The R_{SHUNT} term is the value of the external shunt used to develop the differential voltage across the input pins.

$$Cal = trunc\left(\frac{0.00512}{Current\_LSB \times R_{SHUNT}}\right) \quad (1)$$

where

- 0.00512 is an internal fixed value used to ensure scaling is maintained properly

$$Current\_LSB = \frac{Maximum\ Expected\ Current}{2^{15}} \quad (2)$$

The value of the Current Register (04h) is calculated by multiplying the decimal value of the content in the Shunt Voltage Register (01h) by the decimal value of the Calibration Register, then dividing the product by 2048—this calculation is detailed in Equation 3.

$$Current = \frac{Shunt\ Voltage \times Calibration\ Register}{2048} \quad (3)$$

The LSB for the Bus Voltage Register (02h) is a fixed 1.25 mV/bit. Note that the MSB of the Bus Voltage Register (02h) is always zero because the VBUS pin is only able to measure positive voltages.

The value expected in the Power register (03h) can be calculated by multiplying the Current register value by the Bus Voltage register value and then dividing by 20000 as shown in Equation 4.

$$Power = \frac{Current \times Bus\ Voltage}{20000} \quad (4)$$

Table 2 lists the steps for configuring, measuring, and calculating the values for current and power for this device.

Table 2. Calculating Current and Power

Step	Register name	Address	Contents	Dec	Lsb	Value
Step 1	Configuration Register	00h	4127h	—	—	—
Step 2	Shunt Register	01h	1F40h	8000	2.5 µV	20 mV
Step 3	Bus Voltage Register	02h	2570h	9584	1.25 mV	11.98 V
Step 4	Calibration Register	05h	A00h	2560	—	—
Step 5	Current Register	04h	2710	10000	1 mA	10 A
Step 6	Power Register	03h	12B8h	4792	25 mW	119.82 W

(1) Conditions: Load = 10 A, V_{CM} = 12 V, R_{SHUNT} = 2 mΩ, and V_{VBUS} = 12 V.

Calibration Register and Scaling

The Calibration Register enables the user to scale the Current Register (04h) and Power Register (03h) to the most useful value for a given application. For example, set the Calibration Register such that the largest possible number is generated in the Current Register (04h) or Power Register (03h) at the expected full-scale point. This approach yields the highest resolution using the previously calculated minimum Current_LSB in the equation for the Calibration Register. The Calibration Register can also be selected to provide values in the Current Register (04h) and Power Register (03h) that either provide direct decimal equivalents of the values being measured, or yield a round LSB value for each corresponding register. After

these choices have been made, the Calibration Register also offers possibilities for end-user system-level calibration. After determining the exact current by using an external ammeter, the value of the Calibration Register can then be adjusted based on the measured current result of the TPA6270X to cancel the total system error as shown in Equation 5.

$$\text{Corrected\_Full\_Scale\_Cal} = \text{trunc}\left(\frac{\text{Cal} \times \text{MeasShuntCurrent}}{\text{Device\_Current}}\right) \quad (5)$$

Simple Current Shunt Monitor Usage (No Programming Necessary)

The TPA6270X can be used without any programming if it is only necessary to read a shunt voltage drop and bus voltage with the default power-on reset configuration and continuous conversion of shunt and bus voltage.

The Current register and Power register are only available if the Calibration register contains a programmed value.

Default Settings

The default power-up states of the registers are shown in the Register Details section of this data sheet. These registers are volatile, and if programmed to other than default values, must be re-programmed at every device power-up. Detailed information on programming the Calibration register specifically is given in the section, Programming the Calibration Register.

Bus Overview

The TPA6270X offers compatibility with both I^2C and SMBus interfaces. The I^2C and SMBus protocols are essentially compatible with one another.

The I^2C interface is used throughout this data sheet as the primary example, with SMBus protocol specified only when a difference between the two systems is being addressed. Two bidirectional lines, SCL and SDA, connect the TPA6270X to the bus. Both SCL and SDA are open-drain connections.

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates START and STOP conditions.

To address a specific device, the master initiates a START condition by pulling the data signal line (SDA) from a HIGH to a LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and eight bits of data are sent, followed by an Acknowledge bit. During data transfer, SDA must remain stable while SCL is HIGH. Any change in SDA while SCL is HIGH is interpreted as a START or STOP condition.

Once all data has been transferred, the master generates a STOP condition, indicated by pulling SDA from LOW to HIGH while SCL is HIGH. The TPA6270X includes a 28-ms timeout on its interface to prevent locking up a bus.

Serial Bus Address

The device has two address pins, A0 and A1. The device samples the state of pins A0 and A1 on every bus communication. The following table lists the pin logic levels for each of the 16 possible addresses.

Table 3. Address Pins and Slave Address

A1	A0	Slave Address
GND	GND	1000000
GND	V_S	1000001
GND	SDA	1000010
GND	SCL	1000011

A1	A0	Slave Address
V_S	GND	1000100
V_S	V_S	1000101
V_S	SDA	1000110
V_S	SCL	1000111
SDA	GND	1001000
SDA	V_S	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V_S	1001101
SCL	SDA	1001110
SCL	SCL	1001111

Serial Interface

The TPA6270X operates only as a slave device on the I^2C bus and SMBus. Connections to the bus are made through the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. Although the device incorporates spike suppression into its digital I/O lines, proper layout techniques help minimize the amount of interference coupled into the communication lines. This noise injection can stem from two sources: capacitive coupling of signal edges between the two communication lines themselves, or other switching noise sources present in the system. Routing traces in parallel with ground planes between layers of a printed circuit board (PCB) typically mitigates the effects of coupling between the communication lines. Using shielded communication lines reduces the likelihood of unintended noise coupling into the digital I/O lines—such coupled noise could be misinterpreted as start or stop commands.

The TPA6270X supports the transmission protocol for fast (1- to 400-kHz) and high-speed (1-kHz to 2.94-MHz) modes. All data bytes are transmitted most significant byte first.

SMBus Alert Response

The TPA6270X is designed to respond to the SMBus Alert Response address. The SMBus Alert Response feature enables rapid fault identification for simple slave devices. When an alert occurs, the master device can broadcast the Alert Response slave address (0001100) with the Read/Write bit set high. After this Alert Response operation, any slave device that has generated an alert will identify itself by acknowledging the Alert Response and transmitting its own address on the bus. The Alert Response can activate multiple distinct slave devices simultaneously, similar to the General Call function of the I^2C bus. If more than one slave device attempts to respond, the bus arbitration rules shall apply. The device that loses the arbitration will not generate an acknowledge signal and will keep the Alert line low until the interrupt is cleared.

Writing to and Reading from the TPA6270X

Accessing a particular register on the TPA6270X is accomplished by writing the appropriate value to the register pointer. Refer to Table 4 for a complete list of registers and corresponding addresses. The value for the register pointer as shown in Figure 14. Writing to and Reading from the TPA6270X is the first byte transferred after the slave address byte with the R/W bit LOW. Every write operation to the device requires a value for the register pointer.

Writing to a register begins with the first byte transmitted by the master. This byte is the slave address, with the R/W bit LOW. The TPA6270X then acknowledges receipt of a valid address. The next byte transmitted by the master is the address of the register to which data will be written. This register address value updates the register pointer to the desired register. The next

two bytes are written to the register addressed by the register pointer. The TPA6270X acknowledges receipt of each data byte. The master may terminate data transfer by generating a START or STOP condition.

When reading from the TPA6270X, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a slave address byte with the R/W bit LOW, followed by the register pointer byte. No additional data are required. The master then generates a START condition and sends the slave address byte with the R/W bit HIGH to initiate the read command. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register pointer. This byte is followed by an Acknowledge from the master; then the slave transmits the least significant byte. The master acknowledges receipt of the data byte. The master may terminate data transfer by generating a *Not-Acknowledge* after receiving any data byte, or generating a START or STOP condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the TPA6270X retains the register pointer value until it is changed by the next write operation.

Figure 11 and Figure 12 show write and read operation timing diagrams, respectively. Note that register bytes are sent most-significant byte first, followed by the least significant byte. Figure 13 shows the timing diagram for the SMBus Alert response operation. Figure 14 shows a typical register pointer configuration.

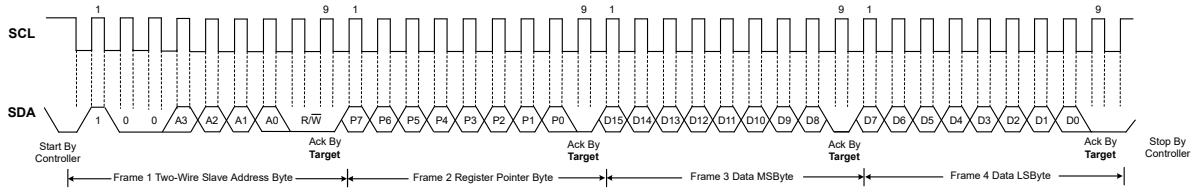


Figure 11. Timing Diagram for Write Word Format

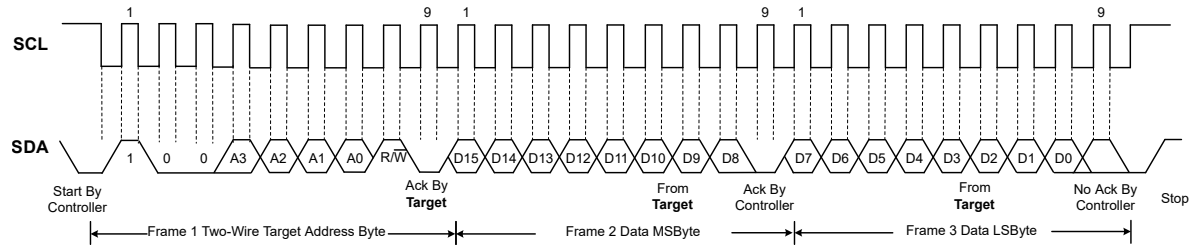


Figure 12. Timing Diagram for Read Word Format

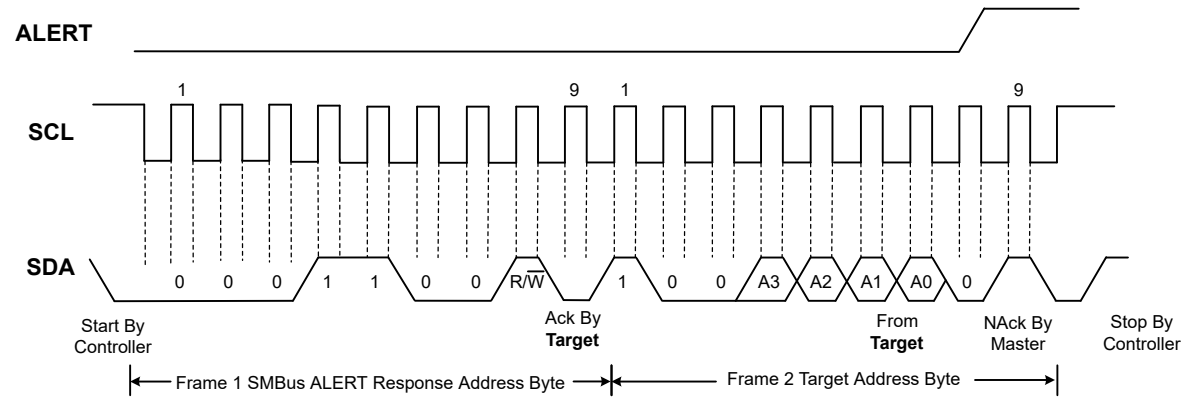


Figure 13. Timing Diagram for SMBus Alert

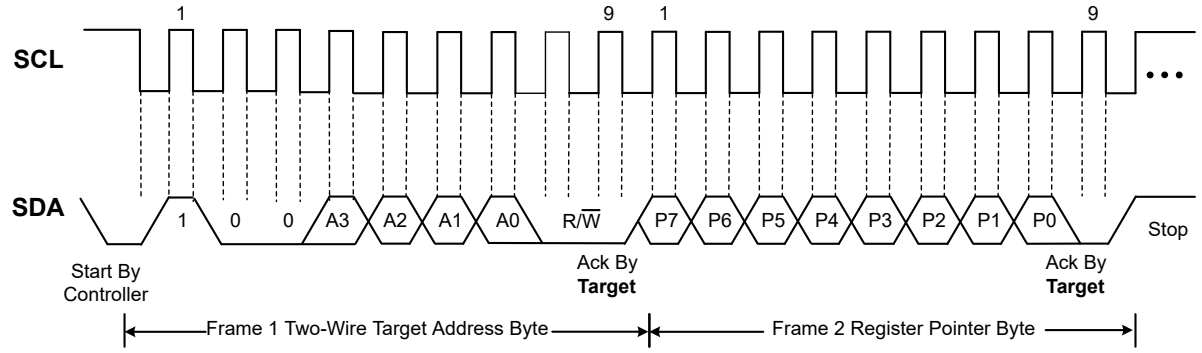


Figure 14. Typical Register Pointer Set

High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pull-up devices. The master generates a start condition followed by a valid serial byte containing high-speed (HS) master code *00001XXX*. This transmission is made in fast (400 kHz) or standard (100 kHz) (F/S) mode at no more than 400 kHz. The TPA6270X does not acknowledge the HS master code, but does recognize it and switches its internal filters to support 2.94 MHz operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 2.94 MHz are allowed. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS-mode. A stop condition ends the HS-mode and switches all the internal filters of the device to support the F/S mode.

Registers

Register Maps

The TPA6270X uses a bank of registers for holding configuration settings, measurement results, minimum/ maximum limits, and status information. Register Maps summarizes the device registers.

All 16-bit device registers are two 8-bit bytes via the I²C interface.

Table 4. Register Set Summary

Pointer Address	Register Name	Function	Power-on Reset		Type (1)
Hex			Binary	Hex	
00h	Configuration Register	All-register reset, shunt voltage and bus voltage ADC conversion times and averaging, operating mode.	01000001 00100111	4127	R/W
01h	Shunt Voltage Register	Shunt voltage measurement data.	00000000 00000000	0000	R
02h	Bus Voltage Register	Bus voltage measurement data.	00000000 00000000	0000	R
03h	Power Register (2)	Contains the value of the calculated power being delivered to the load.	00000000 00000000	0000	R
04h	Current Register (2)	Contains the value of the calculated current flowing through the shunt resistor.	00000000 00000000	0000	R
05h	Calibration Register	Sets full-scale range and LSB of current and power measurements. Overall system calibration.	00000000 00000000	0000	R/W

06h	Mask/Enable Register	Alert configuration and Conversion Ready flag.	00000000 00000000	0000	R/W
07h	Alert Limit Register	Contains the limit value to compare to the selected Alert function.	00000000 00000000	0000	R/W
FEh	Manufacturer ID Register	Contains unique manufacturer identification number.	0101010001001001	5449	R
FFh	Die ID Register	Contains unique die identification number.	0010001001100000	2260	R

(1) Type: R = Read-Only, R/ W = Read/Write.
(2) The Current Register (04h) and Power Register (03h) default to '0' because the Calibration register defaults to '0', yielding zero current and power values until the Calibration register is programmed.

Configuration Register (00h) (Read/Write)

Table 5. Configuration Register (00h) (Read/Write) Descriptions

Bit No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RST	—	—	—	AVG2	AVG1	AVG0	VBUSCT2	VBUSCT1	VBUSCT0	VSHCT2	VSHCT1	VSHCT0	MODE3	MODE2	MODE1
Por Value	0	1	0	0	0	0	0	1	0	0	1	0	0	1	1	1

The parameter settings of the Configuration Register dictate the operating modes of the device. This register not only governs the conversion time configurations for both shunt voltage and bus voltage measurements, but also controls the averaging mode employed. In addition, the operating mode that selects the signals to be measured is also programmed and configured within the Configuration Register.

The Configuration Register is readable at any time, with no impact on the existing device settings or any ongoing conversion process. Writing data to the Configuration Register will suspend all in-progress conversions immediately until the entire write sequence is finalized. After that, a new conversion cycle will be initiated based on the updated parameters stored in the Configuration Register (address 00h). This suspension mechanism ensures that the execution conditions for the next complete conversion are unambiguous and fully deterministic.

RST: Reset Bit

Bit 15

Setting this bit to '1' generates a system reset that is the same as power-on reset. Resets all registers to default values; this bit self-clears.

AVG: Averaging Mode

Bits 9–11

Determines the number of samples that are collected and averaged. Table 6 shows all the AVG bit settings and related number of averages for each bit setting.

Table 6. AVG Bit Settings [11:9] Combinations

AVG2 D11	AVG1 D10	AVG0 D9	Number of Averages (1)
0	0	0	1
0	0	1	4
0	1	0	16

AVG2 D11	AVG1 D10	AVG0 D9	Number of Averages (1)
0	1	1	64
1	0	0	128
1	0	1	256
1	1	0	512
1	1	1	1024

(1) Shaded values are default.

VBUSCT: Bus Voltage Conversion Time

Bits 6-8

Sets the conversion time for the bus voltage measurement. Table 7 shows the VBUSCT bit options and related conversion times for each bit setting.

Table 7. VBUSCT Bit Settings [8:6] Combinations

VBUSCT2 D8	VBUSCT1 D7	VBUSCT0 D6	Conversion Time (μS)
0	0	0	66
0	0	1	134
0	1	0	269
0	1	1	542
1	0	0	1085
1	0	1	2170
1	1	0	4341
1	1	1	8682

(1) Shaded values are default.

VSHCT: Shunt Voltage Conversion Time

Bits 3-5

Sets the conversion time for the shunt voltage measurement. Table 8 shows the VSHCT bit options and related conversion times for each bit setting.

Table 8. VSHCT Bit Settings [5:3] Combinations

VSHCT2 D5	VSHCT1 D4	VSHCT0 D3	Conversion Time (1)
0	0	0	66
0	0	1	134
0	1	0	269
0	1	1	542
1	0	0	1085
1	0	1	2170
1	1	0	4341
1	1	1	8682

(1) Shaded values are default.

MODE: Operating Mode

Bits 0-2

Selects continuous, triggered, or power-down mode of operation. These bits default to continuous shunt and bus measurement mode. The mode settings are shown in Table 9.

Table 9. Mode Settings [2:0] Combinations

Mode3 D2	Mode2 D1	Mode1 D0	Mode (1)
0	0	0	Power-Down (or Shutdown)
0	0	1	Shunt Voltage, Triggered
0	1	0	Bus Voltage, Triggered
0	1	1	Shunt and Bus, Triggered
1	0	0	Power-Down (or Shutdown)
1	0	1	Shunt Voltage, Continuous
1	1	0	Bus Voltage, Continuous
1	1	1	Shunt and Bus, Continuous

(1) Shaded values are default.

Shunt Voltage Register (01h) (Read-Only)

The Shunt Voltage Register holds the real-time measured value of the shunt voltage, designated as VSHUNT. Negative values are represented in the two's complement binary format. To generate the two's complement of a negative number, first invert all the bits of the binary number corresponding to its absolute value, then add 1 to the resulting value. A value of '1' in the MSB indicates that the number is negative.

Example: For a value of VSHUNT = –80 mV:

1. Take the absolute value: 80 mV
2. Translate this number to a whole decimal number (80 mV ÷ 2.5 μV) = 32000
3. Convert this number to binary = 0111 1101 0000 0000
4. Complement the binary result = 1000 0010 1111 1111
5. Add '1' to the complement to create the two's complement result = 1000 0011 0000 0000 = 8300h

When the averaging function is activated, the register will output the averaged result.

Full-scale range = 81.92 mV (decimal = 7FFF); LSB: 2.5 μV.

Table 10. Shunt Voltage Register (01h) (Read-Only) Description

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	SIGN	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Por Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bus Voltage Register (02h) (Read-Only)(1)

The Bus Voltage Register holds the latest measurement data of the bus voltage, denoted as VBUS.

Full-scale range = 40.96 V (decimal = 7FFF); LSB = 1.25 mV.

Table 11. Bus Voltage Register (02h) (Read-Only) Description

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	—	BD14	BD13	BD12	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
Por Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) D15 is always zero because bus voltage can only be positive.

Power Register (03h) (Read-Only)

When the averaging function is activated, the register will output the averaged result.

The LSB of the Power Register is internally calibrated to be equivalent to 25 times the programmed value of the Current_LSB.

In accordance with Equation 4, the Power Register calculates and logs power in Watts by multiplying the decimal value of the Current Register by that of the Bus Voltage Register.

Table 12. Power Register (03h) (Read-Only) Description

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Por Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Current Register (04h) (Read-Only)

When the averaging function is activated, the register will output the averaged result.

In accordance with Equation 3, the value of the Current Register is derived by multiplying the decimal value stored in the Shunt Voltage Register by that stored in the Calibration Register.

Table 13. Current Register (04h) (Read-Only) Register Description

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	CSIGN	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
Por Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Calibration Register (05h) (Read/Write)

This register supplies the device with the parameter value of the shunt resistor, which the device leverages to generate the measured differential voltage. Meanwhile, it also configures the resolution of the Current Register. Programming this register determines the values of both the Current_LSB and the Power_LSB. In addition, this register is applicable for overall system calibration.

Table 14. Calibration Register (05h) (Read/Write) Description

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	—	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0
Por Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mask/Enable Register (06h) (Read/Write)

The Mask/Enable Register designates the enabled functions that govern the operational mode and logical behavior of the Alert pin. In the event that multiple functions are activated simultaneously, the highest priority shall be assigned to the most significant bit position of the Alert Function (D15–D11), which will respond to the configuration parameters of the Alert Limit Register.

Table 15. Mask/Enable Register (06h) (Read/Write)

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	SOL	SUL	BOL	BUL	POL	CNVR	—	—	—	—	—	AFF	CVRF	OVF	APOL	LEN
Por Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SOL: Shunt Voltage Over-Voltage

Bit 15

Setting this bit high configures the alert pin to be asserted if the shunt voltage measurement following a conversion exceeds the value programmed in the alert limit register.

SUL: Shunt Voltage Under-Voltage

Bit 14

Setting this bit high configures the alert pin to be asserted if the shunt voltage measurement following a conversion drops below the value programmed in the alert limit register.

BOL: Bus Voltage Over-Voltage

Bit 13

Setting this bit high configures the alert pin to be asserted if the bus voltage measurement following a conversion exceeds the value programmed in the alert limit register.

BUL: Bus Voltage Under-Voltage

Bit 12

Setting this bit high configures the alert pin to be asserted if the bus voltage measurement following a conversion drops below the value programmed in the alert limit register.

POL: Power Over-Limit

Bit 11

Setting this bit high configures the alert pin to be asserted if the Power calculation made following a bus voltage measurement exceeds the value programmed in the alert limit register.

CNVR: Conversion Ready

Bit 10

Setting this bit high configures the alert pin to be asserted when the conversion ready flag, Bit 3, is asserted indicating that the device is ready for the next conversion.

AFF: Alert Function Flag

Bit 4

While only one alert function can be monitored at the alert pin at a time, the conversion ready can also be enabled to assert the alert pin. Reading the alert function flag following an alert allows the user to determine if the alert function is the source of the alert.

When the alert latch enable bit is set to latch mode, the alert function flag bit clears only when the mask/enable register is read. When the alert latch enable bit is set to transparent mode, the alert function flag bit is cleared following the next conversion that does not result in an alert condition.

CVRF: Conversion Ready Flag

Bit 3

Although the device can be read at any time, and the data from the last conversion is available, the conversion ready flag bit is provided to help coordinate one-shot or triggered conversions. The conversion ready flag bit is set after all conversions, averaging, and multiplications are complete. The conversion ready flag bit clears under the following conditions:

1. Writing to the configuration register (except for the power-down selection).
2. Reading the mask/enable register.

OVF: Math Overflow Flag

Bit 2

This bit is set to '1' if an arithmetic operation results in an overflow error. It indicates that current and power data may be invalid.

APOL: Alert Polarity bit; sets the Alert pin polarity.

Bit 1

1 = inverted (active-high open collector)

0 = normal (active-low open collector) (default)

LEN: Alert Latch Enable; configures the latching feature of the Alert pin and Alert Flag bits.

Bit 0

1 = latch enabled

0 = transparent (default)

When the alert latch enable bit is set to transparent mode, the alert pin and flag bit resets to the idle states when the fault is cleared. When the alert latch enable bit is set to latch mode, the alert pin and alert flag bit remain active following a fault until the Mask/Enable register is read.

Alert Limit Register (07h) (Read/Write)

The Alert Limit Register contains the value used to compare to the register selected in the Mask/Enable Register to determine if a limit has been exceeded.

Table 16. Alert Limit Register (07h) (Read/Write) Description

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	AUL15	AUL14	AUL13	AUL12	AUL11	AUL10	AUL9	AUL8	AUL7	AUL6	AUL5	AUL4	AUL3	AUL2	AUL1	AUL0
Por Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Manufacturer ID Register (FEh) (Read-Only)

The Manufacturer ID Register stores a unique identification number for the manufacturer.

Table 17. Manufacturer ID Register (FEh) (Read-Only) Description

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Por Value	0	1	0	1	0	1	0	0	0	1	0	0	1	0	0	1

ID: Manufacturer ID Bits

Bits 0-15

Stores the manufacturer identification bits.

Die ID Register (FFh) (Read-Only)

The Die ID Register stores a unique identification number and the revision ID for the die.

Table 18. Die ID Register (FFh) (Read-Only) Description

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	DID11	DID10	DID9	DID8	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0	RID3	RID2	RID1	RID0
Por Value	0	0	1	0	0	0	1	0	0	1	1	0	0	0	0	0

DID: Device ID Bits

Bits 4-15

Stores the device identification bits

RID: Die Revision ID Bits

Bits 0-3

Stores the device revision identification bits

Power Supply Recommendations

The input circuitry of the device is capable of accurately measuring signals with common-mode voltages that exceed the power supply voltage, VVS. For instance, while the voltage applied to the V_{VS} power supply terminal may be 5 V, the load

power-supply voltage under monitoring (i.e., the common-mode voltage) can reach up to 36 V. It should also be noted that the device can withstand the full 0 V to 36 V range at its input terminals, regardless of whether the device is powered or not.

For optimal stability, place the required power-supply bypass capacitors as close as possible to the device's power and ground pins. A typical value for this bypass capacitor is 0.1 µF. In applications with noisy or high-impedance power supplies, additional decoupling capacitors may be necessary to effectively suppress power-supply noise

Layout

Connect the input pins (IN+ and IN-) to the sensing resistor using a Kelvin connection or a 4-wire connection. These connection techniques verify that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current-sensing resistor, any additional high-current carrying impedance causes significant measurement errors. Place the power-supply bypass capacitor as close as possible to the supply and ground pins.

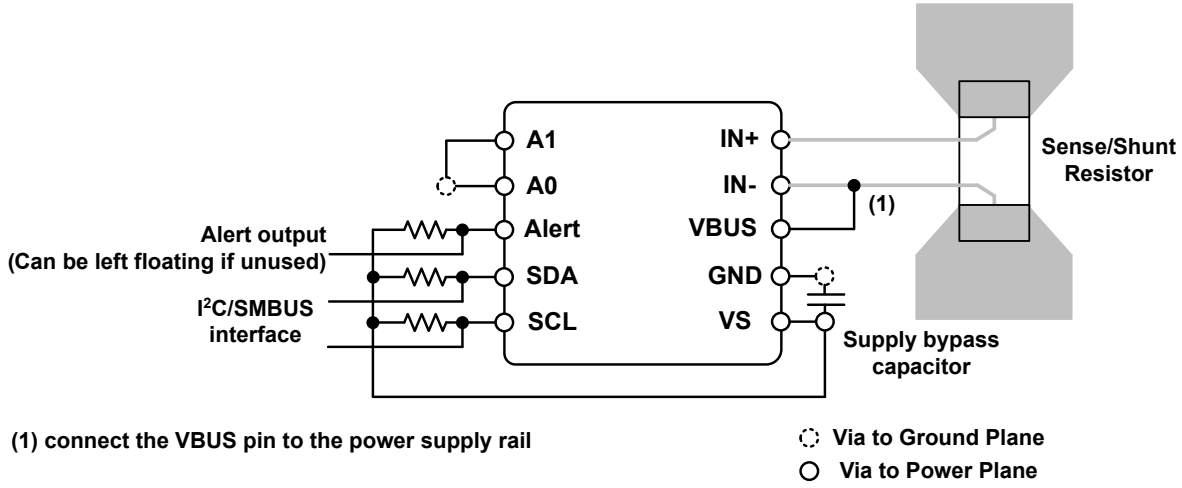
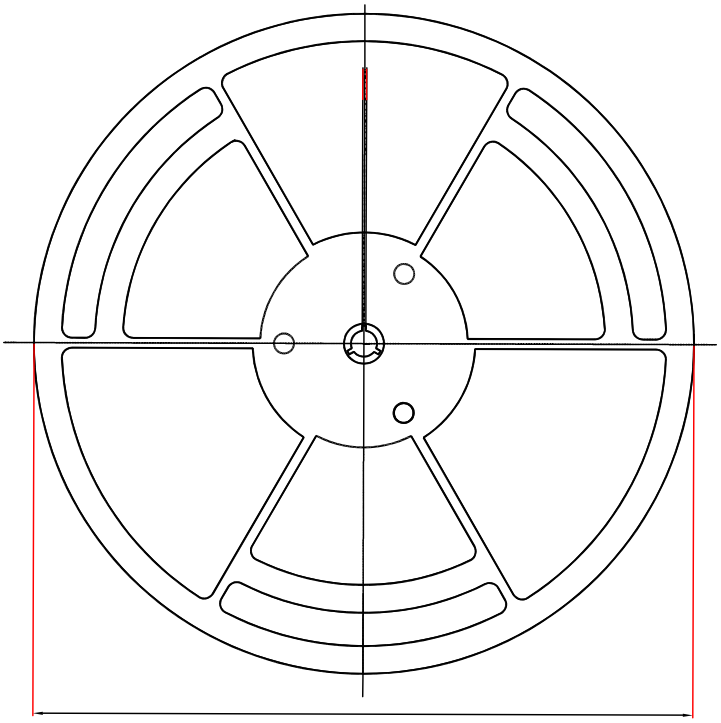
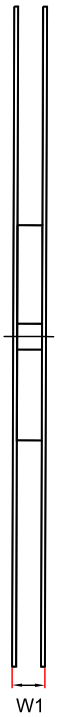
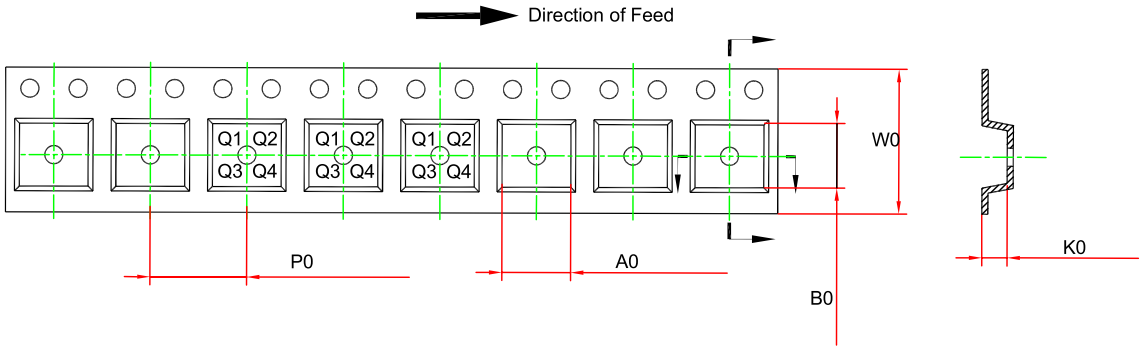


Figure 15. Layout Example

Tape and Reel Information





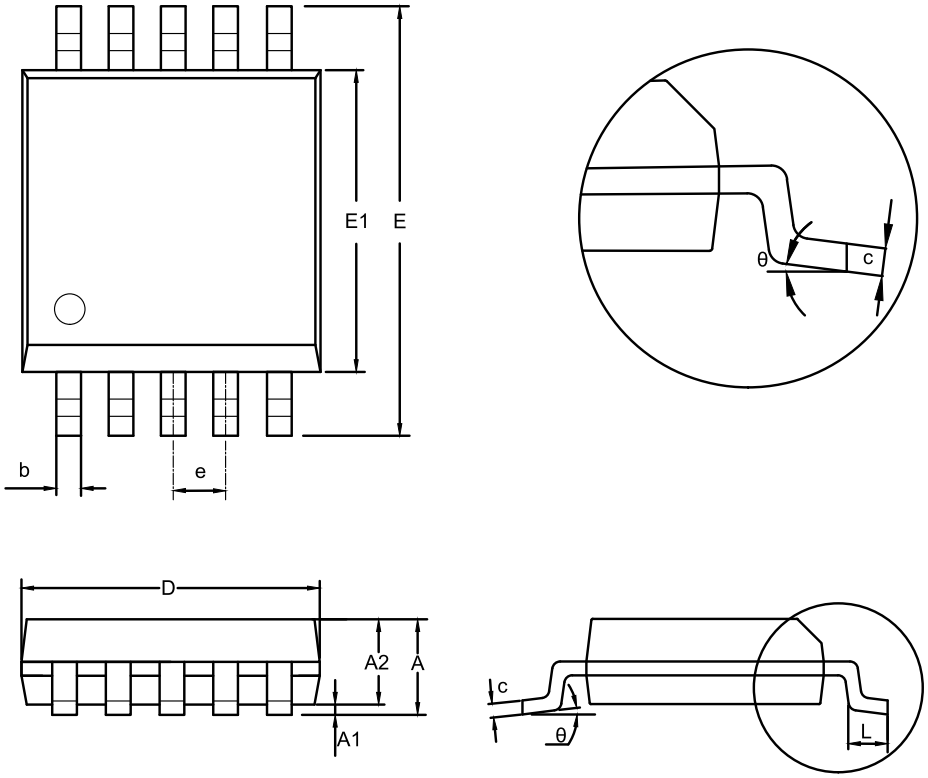


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPA6270X-VS2R-S	MSOP10	330.0	17.6	5.30	3.30	1.40	8.0	12.0	Q1

Package Outline Dimensions

MSOP10

Package Outline Dimensions VS2(MSOP-10-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
e	0.500 BSC		0.020 BSC	
L	0.400	0.800	0.016	0.031
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPA6270X-VS2R-S	−40 to 125°C	MSOP10	6270	MSL2	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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