Femtoampere Input Bias Current Amplifier

Features

- Ultra-Low Input Bias Current:
  - ±100 fA (Max) at T_A = 25°C (Lab Test Limit)
  - ±800 fA (Max) at −40°C < T_A < +125°C (Lab Test Limit)
- Low Input Offset Voltage: ±150 μV (Max)
- Integrated Guard Buffer with 120-μV Maximum Offset
- Low Voltage Noise Density: 18 nV/√Hz at 1 kHz
- Wide Bandwidth: 2.1 MHz
- Supply Voltage: 4.5 V to 16 V (±2.25 V to ±8 V)
- Rail-to-Rail Output Swing
- ESD Rating: Robust 3-kV HBM, 1.5-kV CDM

Applications

- Photodiode Sensor Interface
- Industrial Sensors and Instrumentation
- A.T.E. Leakage Testing

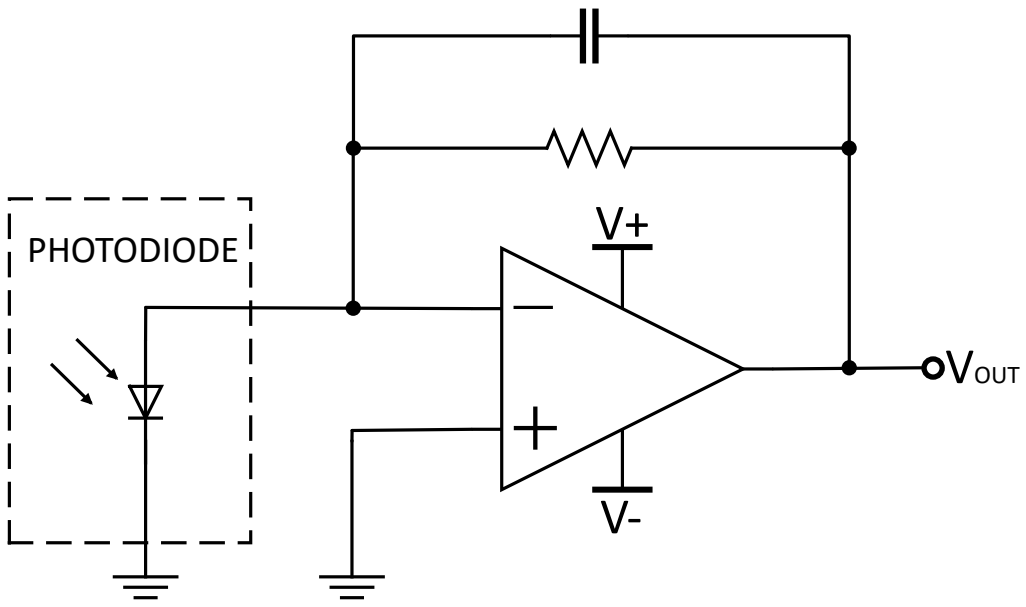
Description

The TPA3530 operational amplifier features a femtoampere-level input bias current. It operates from 4.5 V to 16 V (±2.25 V to ±8 V), and features rail-to-rail output swing in addition to an input common-mode range that includes ground. The integrated guard buffer isolates the input pins from leakage in the printed circuit board. It minimizes board component counts and enables easy system design.

The TPA3530 is ideal for portable medical and industrial applications that require low-bias current analog front-end performance, such as photodiode trans-impedance and chemical sensor interface circuits.

The TPA3530 is available in the SOP8 package, and is specified over the industrial temperature range from –40°C to +125°C. The unique pinout is optimized to prevent signals from coupling among the sensitive input pins, power supplies, and output pins while enabling easy routing of the guard ring traces.

Typical Application Circuit



Trans-Impedance Amplifier with Photodiode

Table of Contents

Product Family Table

Order Number	Package	Mark Information	MSL	Transport Media, Quantity
TPA3530-SO1R	SOP8	A3530	2	Tape and Reel, 4000

Revision History

Date	Revision	Notes
2022-09-10	Rev.Pre.0	Pre-released version.
2023-05-15	Rev.A.0	Initial release.
2024-12-18	Rev.A.1	The following updates are all about the new datasheet formats or typos, and the actual product remains unchanged. • Updated the Tape and Reel Information.

Pin Configuration and Functions

TPA3530
SOP8
Top View

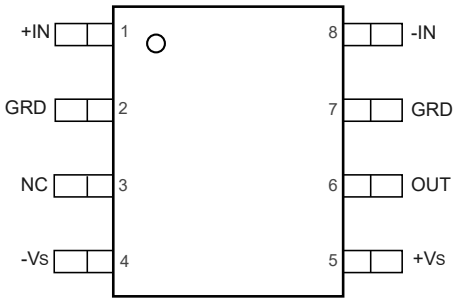


Table 1. Pin Functions: TPA3530

Pin	Name	I/O	Description
SOP8			
1	+IN	I	Non-inverting input.
2	GRD	O	Guard.
3	NC	–	No internal connection.
4	$-V_S$	–	Negative power supply.
5	$+V_S$	–	Positive power supply.
6	OUT	O	Output.
7	GRD	O	Guard.
8	−IN	I	Inverting input.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Supply Voltage	$(+V_S) - (-V_S)$		17	V
Signal Input Pins (2)	Voltage	$(-V_S) - 0.3$	$(+V_S) + 0.3$	V
	Current	−10	10	mA
Differential Input Voltage	Differential ($V_{+IN} - V_{-IN}$)	−7	7	V
Output Short Current	Short Circuit to Ground	Indefinite		
T_A	Operating Temperature Range	−40	125	°C
T_J	Junction Temperature Range		150	°C
T_{stg}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The input pins are diode-clamped to the power-supply rails. The input signal current that can swing more than 0.3 V beyond the supply rails must be limited to 10 mA or less.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	3	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_S	Supply Voltage	4.5 (±2.25)		16 (±8)	V
V_{IN}	Signal Input Pins	$-V_S$		$(+V_S) - 1.5$	V
T_A	Operating Ambient Temperature	−40		125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOP8	158	43	°C/W

Electrical Characteristics

All test conditions: V_S = (+V_S) – (−V_S) = 4.5 V, T = 25°C, V_{CM} = V_S / 2, R_L = 10 KΩ, C_L = 10 pF, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supply						
I_Q	Quiescent Current per Amplifier	I_{OUT} = 0 mA		0.9	1.4	mA
		−40°C < T_A < +125°C			1.5	
PSRR	Power Supply Rejection Ratio	V_S = 4.5 V to 16 V	115	127		dB
		−40°C < T_A < +125°C	110			
Input Characteristics						
I_B (1)	Input Bias Current	RH < 50%	−100		100	fA
		−40°C < T_A < +80°C, RH < 50%	−300		300	
		−40°C < T_A < +125°C, RH < 50%	−800		800	
I_{OS} (1)	Input Offset Current	RH < 50%	−50		50	fA
		−40°C < T_A < +125°C, RH < 50%	−200		200	
V_{OS}	Input Offset Voltage	V_{CM} = 0 V to 1.5 V	−100		100	μV
		V_{CM} = 1.5 V to 3 V	−150		150	
		V_{CM} = 0 V to 3 V, −40°C < T_A < 125°C	−600		600	
V_{OS} TC	Input Offset Voltage Drift	−40°C < T_A < 125°C		2		μV/°C
V_{CM}	Input Common-Mode Voltage		0		3	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 1.5 V to 3 V	92			dB
		V_{CM} = 1.5 V to 3 V, −40°C < T_A < +125°C	90			
		V_{CM} = 0 V to 3 V	75			
A_{OL}	Open-Loop Gain	R_L = 2 kΩ to V_{CM}, V_{OUT} = 0.2 V to 4.3 V	122			dB
		−40°C < T_A < +125°C	120			
R_{IN}	Input Resistance	−40°C < T_A < +125°C		>100		TΩ
C_{IN}	Input Capacitance			10		pF
Output Characteristics						
V_{OH}	Output Voltage High	R_L = 10 kΩ to V_{CM}, −40°C < T_A < +125°C	4.46			V
		R_L = 2 kΩ to V_{CM}, −40°C < T_A < +125°C	4.38			
V_{OL}	Output Voltage Low	R_L = 10 kΩ to V_{CM}, −40°C < T_A < +125°C			40	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		R_L = 2 kΩ to V_{CM}, −40°C < T_A < +125°C			120	
I_{SC}	Short-Circuit Current	Source current		31		mA
		Sink current		19		
AC Electrical Characteristics						
GBW	Gain Bandwidth			2.1		MHz
SR	Slew Rate			1.4		V/μs
V_N	Input Voltage-Noise Density	f = 1 kHz		18		nV/√Hz
V_{NP-P}	Input Voltage Noise	f = 0.1 Hz to 10 Hz		4		$μV_{P-P}$
C_{LOAD}	Capacitive Loading	No sustained oscillations		100		pF
Guard Buffer						
V_{GOS}	Guard Offset Voltage	V_{SUPPLY} = 5 V, V_{CM} = V_{SUPPLY} / 2	−120		120	μV

(1) Guaranteed by design. +IN and −IN are internally connected to the gates of the CMOS transistors. CMOS GATE leakage is so small that it is impractical to test in production. Devices are screened during production testing to eliminate defective units.

Electrical Characteristics (Continued)

All test conditions: V_S = (+V_S) – (–V_S) = 16 V, T = 25°C, V_{CM} = V_S / 2, R_L = 10 KΩ, C_L = 10 pF, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supply						
I_Q	Quiescent Current per Amplifier	I_{OUT} = 0 mA		0.9	1.4	mA
		−40°C < T_A < +125°C			1.5	
PSRR	Power Supply Rejection Ratio	V_S = 4.5 V to 16 V	115	127		dB
		−40°C < T_A < +125°C	110			
Input Characteristics						
I_B (1)	Input Bias Current	RH < 50%	−100		100	fA
		−40°C < T_A < +80°C, RH < 50%	−300		300	
		−40°C < T_A < +125°C, RH < 50%	−800		800	
I_{OS} (1)	Input Offset Current	RH < 50%	−50		50	fA
		−40°C < T_A < +125°C, RH < 50%	−200		200	
V_{OS}	Input Offset Voltage	V_{CM} = 0 V to 1.5 V	−100		100	μV
		V_{CM} = 1.5 V to 14.5 V	−150		150	
		V_{CM} = 0 V to 14.5 V, −40°C < T_A < 125°C	−600		600	
V_{OS} TC	Input Offset Voltage Drift	−40°C < T_A < 125°C		2		μV/°C
V_{CM}	Input Common-Mode Voltage		0		14.5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 1.5 V to 14.5 V	107			dB
		V_{CM} = 1.5 V to 14.5 V, −40°C < T_A < +125°C	105			
		V_{CM} = 0 V to 14.5 V	95			
A_{OL}	Open-Loop Gain	R_L = 2 kΩ to V_{CM}, V_{OUT} = 0.2 V to 4.3 V	127			dB
		−40°C < T_A < +125°C	125			
R_{IN}	Input Resistance	−40°C < T_A < +125°C		>100		TΩ
C_{IN}	Input Capacitance			10		pF
Output Characteristics						
V_{OH}	Output Voltage High	R_L = 10 kΩ to V_{CM}, −40°C < T_A < +125°C	15.9			V
		R_L = 2 kΩ to V_{CM}, −40°C < T_A < +125°C	15.58			
V_{OL}	Output Voltage Low	R_L = 10 kΩ to V_{CM}, −40°C < T_A < +125°C			100	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		R_L = 2 kΩ to V_{CM}, −40°C < T_A < +125°C			420	
I_{SC}	Short-Circuit Current	Source current		33		mA
		Sink current		21		
AC Electrical Characteristics						
GBW	Gain Bandwidth			2.1		MHz
SR	Slew Rate			1.4		V/μs
V_N	Input Voltage-Noise Density	f = 1 kHz		18		nV/√Hz
V_{NP-P}	Input Voltage Noise	f = 0.1 Hz to 10 Hz		4		$μV_{P-P}$
C_{LOAD}	Capacitive Loading	No sustained oscillations		100		pF
Guard Buffer						
V_{GOS}	Guard Offset Voltage	V_{SUPPLY} = 5 V, V_{CM} = V_{SUPPLY} / 2	−120		120	μV

(1) Guaranteed by design. +IN and −IN are internally connected to the gates of the CMOS transistors. CMOS GATE leakage is so small that it is impractical to test in production. Devices are screened during production testing to eliminate defective units.

Typical Performance Characteristics

All test conditions: V_S = (+V_S) – (–V_S) = 4.5 V, T = 25°C, V_{CM} = V_S / 2, R_L = 10 kΩ, C_L = 10 pF, unless otherwise noted.

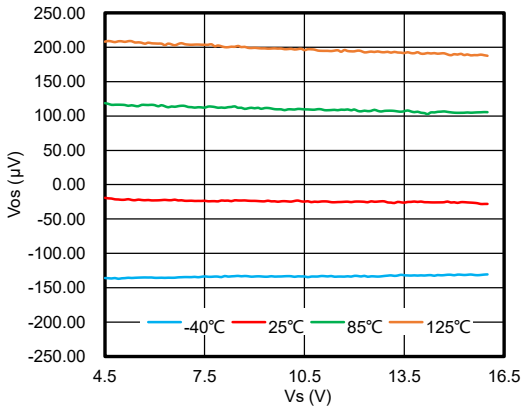


Figure 1. Input Offset Voltage vs. Supply Voltage

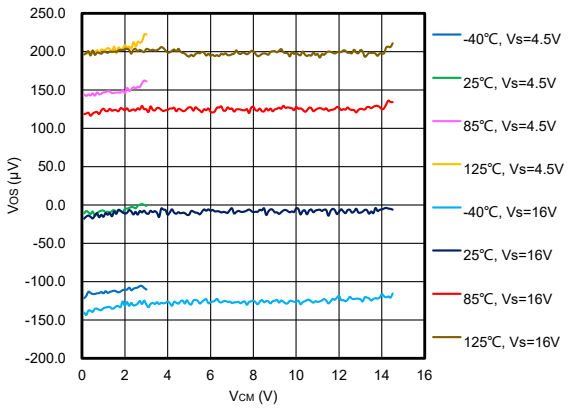


Figure 2. Input Offset Voltage vs. Common-Mode Voltage

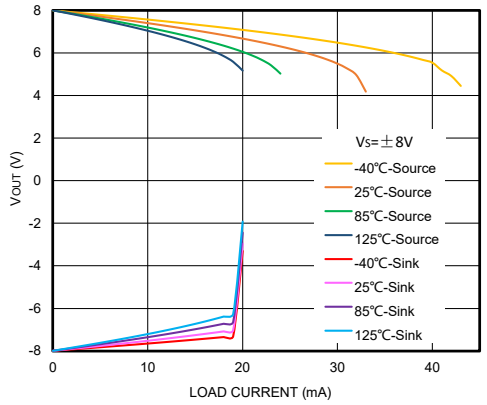


Figure 3. Output Voltage vs. Load Current

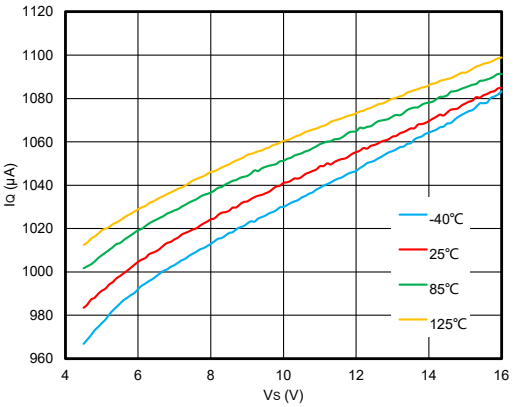


Figure 4. Quiescent Current vs. Supply Voltage

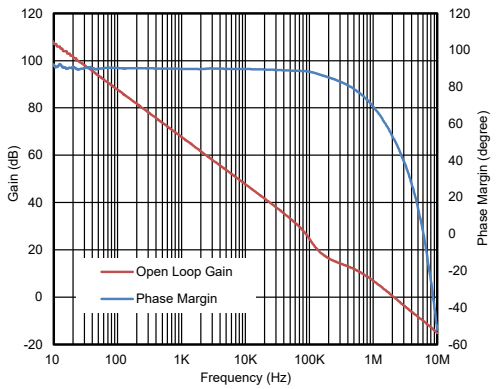


Figure 5. Open-Loop Gain and Phase Margin vs. Frequency

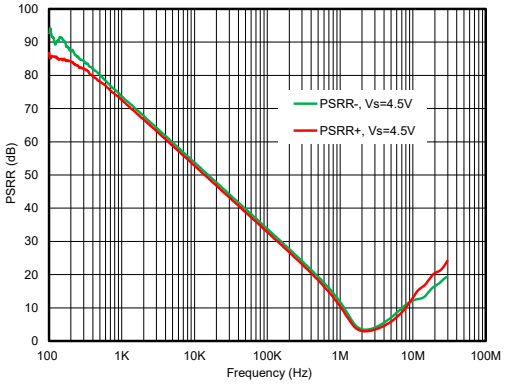


Figure 6. PSRR vs. Frequency, V_S = 4.5 V

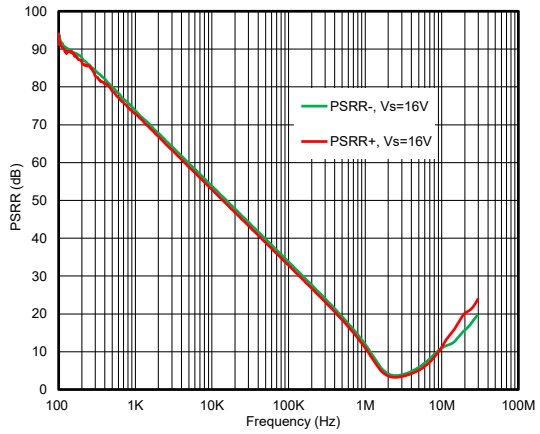


Figure 7. PSRR vs. Frequency, V_S = 16 V

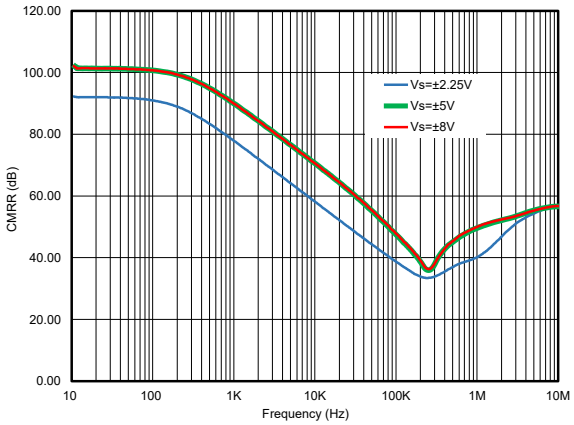


Figure 8. CMRR vs. Frequency

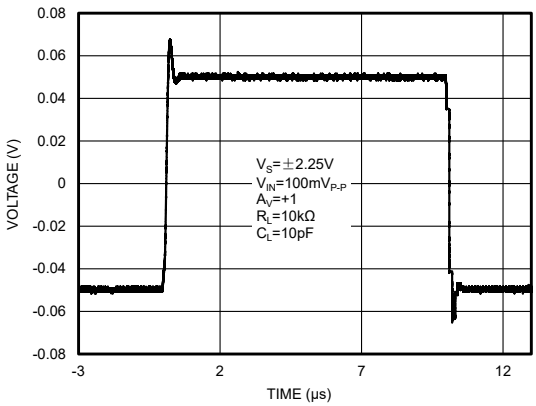


Figure 9. Small-Signal Transient Response, V_S = ±2.25 V

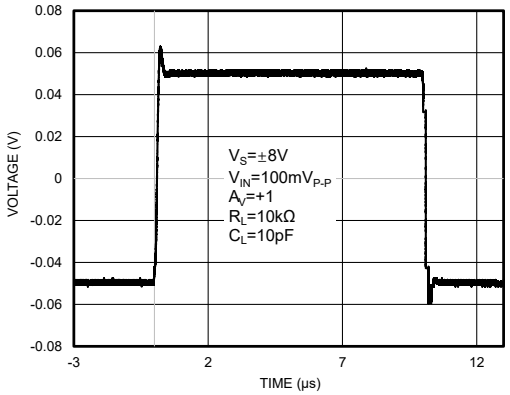


Figure 10. Small-Signal Transient Response, V_S = ±8 V

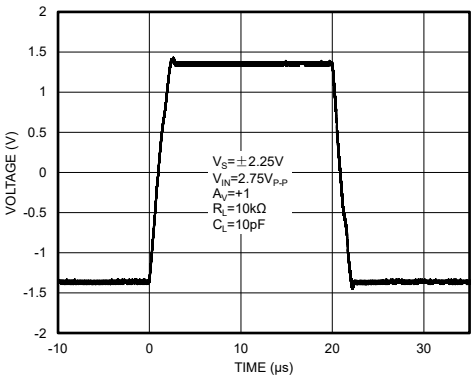


Figure 11. Large-Signal Transient Response, V_S = ±2.25 V

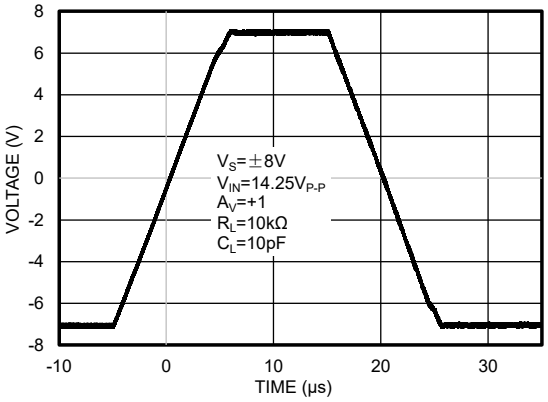


Figure 12. Large-Signal Transient Response, V_S = ±8 V

Detailed Description

Overview

The TPA3530 can interface with small signals from either current sources or high-output impedance voltage sources. Applications include photodiode pulse oximeters, pH sensors, capacitive pressure sensors, chemical analysis equipment, smoke detectors, and humidity sensors. The TPA3530 features a combination of low-input current, rail-to-rail output voltage swing, wide-supply voltage range, and low-power operation.

Functional Block Diagram

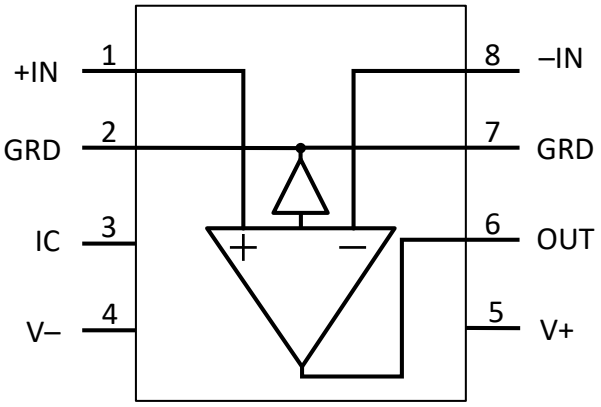


Figure 13. Functional Block Diagram

Feature Description

Input Bias and Guard Buffer

The TPA3530 features a MOS-input stage with only 100 fA (max) of input bias current. The unique input diode structure provides ESD protection, and allows the diodes to be guarded to minimize leakage currents at the input pins. The TPA3530 integrates a precision buffer that guards internal ESD diode leakage paths. The buffer input is connected to the non-inverting input (+IN) which is approximately equal to the input common-mode voltage when the main amplifier feedback loop is settled.

The output of this guard buffer is also connected to external pins (GRD), allowing users to guard external components against leakage currents. The input bias current is determined by the accuracy of the guard voltage applied across the ESD diodes.

Input Common-Mode Voltage

The TPA3530 is a rail-to-rail output amplifier with an input voltage range from ($-V_S$) to ($+V_S$) − 1.5 V. The input guard buffer supports rail-to-rail output that allows the guard voltage to swing within 100 mV of the supply rails. Because the guard buffer output follows the input common-mode voltage, this output range limits the effectiveness of the guard buffer at low-input common-mode voltages. For this reason, it is not recommended to operate the circuit with an input common-mode voltage of less than 100 mV from the $-V_S$ supply rail.

Rail-to-Rail Output Stage

The TPA3530 output stage swings to within 30 mV (typ) of either power-supply rail with a 100-kΩ load, and provides a 2.1-MHz GBW with a 1.4-V/μs slew rate. The device is also unity-gain stable.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPA3530 is a single CMOS operational amplifier with femtoampere input bias current and ultra-low offset voltage. It is suited for a wide variety of current output transducers (such as photodiodes and photomultiplier tubes), spectrometry, chromatography, and high-impedance buffering for chemical sensors.

Power Supply

The TPA3530 operates from +4.5 V to +16 V (±2.25 V to ±8 V). Bypass the power-supply inputs, $+V_S$ and $-V_S$, to a quiet copper ground plane, with a 0.1-μF IC capacitor in parallel with a 4.7-μF electrolytic capacitor, placed close to the pins.

High-Impedance Sensor Front Ends

The TPA3530 interfaces include photodiodes and potentiostat sensors, and high-impedance voltage sources, such as pH sensors. It is designed to maximize the performance of high-impedance circuits.

Typical Application

Figure 14 shows the TPA3530 configured in a trans-impedance amplifier interfacing with a photodiode.

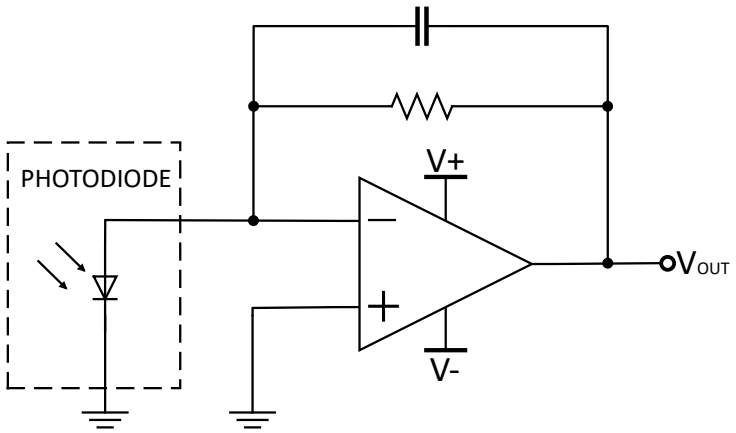


Figure 14. Trans-Impedance Amplifier with Photodiode

TIA Application Recommendations

It is essential to take into account various noise sources. Op amp noise voltage, feedback resistor thermal noise, input noise current, and photodiode noise current do not operate across the same frequency range when analyzing the noise at the output of the TIA. The op amp noise voltage is gained up within the range between the noise gain zero and its pole. The higher the values of RF and C_{IN} are (C_{IN} is the total capacitance at the inverting terminal of the op amp, including the photodiode capacitance and input capacitance), the sooner the noise gain peaking starts, and the larger its contribution to

the total output noise is. An equivalent total-noise voltage is calculated by taking the square root of the sum of squared contributing noise voltages at the output of TIA.

Layout

Layout Guideline

A good layout is critical to obtaining high performance especially when interfacing with high-impedance sensors. Use shielding techniques to guard against parasitic leakage paths. The goal of guarding is to completely surround the insulation of the high-impedance node with another conductor that is driven to the guard voltage. The guard rail isolates sensitive nodes, such as the inverting input and the traces connecting to it, from varying or large-voltage differentials that otherwise occur in the rest of the circuit board. This reduces leakage and noise effects, allowing accurate sensitive measurements.

Be careful when decreasing the amount of stray capacitance at the inputs of op amp to improve stability. To achieve this, minimize trace lengths and resistor leads by placing external components as close as possible to the package. If the sensor is inherently capacitive or is connected to the amplifier through a long cable, use a low-value feedback capacitor to control high-frequency gain and peaking to stabilize the feedback loop.

Layout Example

Figure 15 shows the implementation of a guard ring in the TIA circuit. The guard ring shape is extended around these passive components to ensure that the entire high-impedance node is surrounded by guard. The guard ring is directly driven from the internal guard buffer.

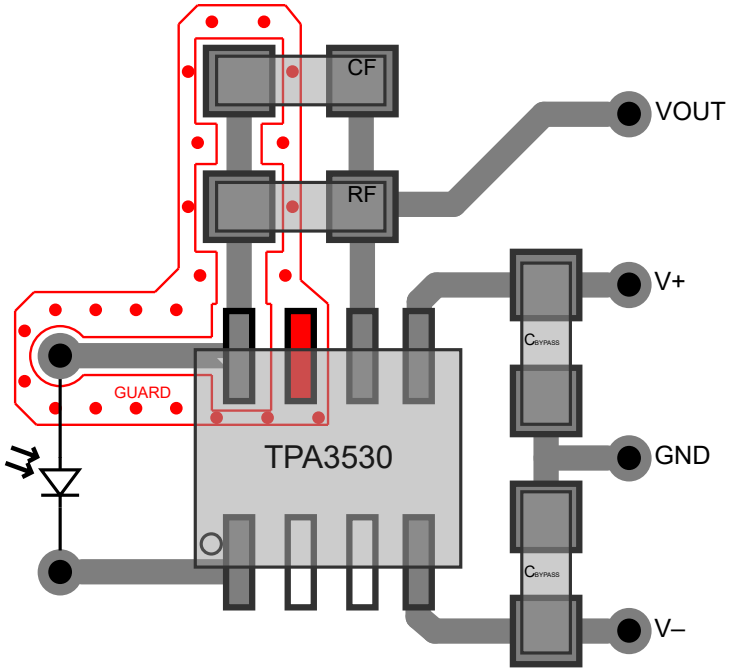
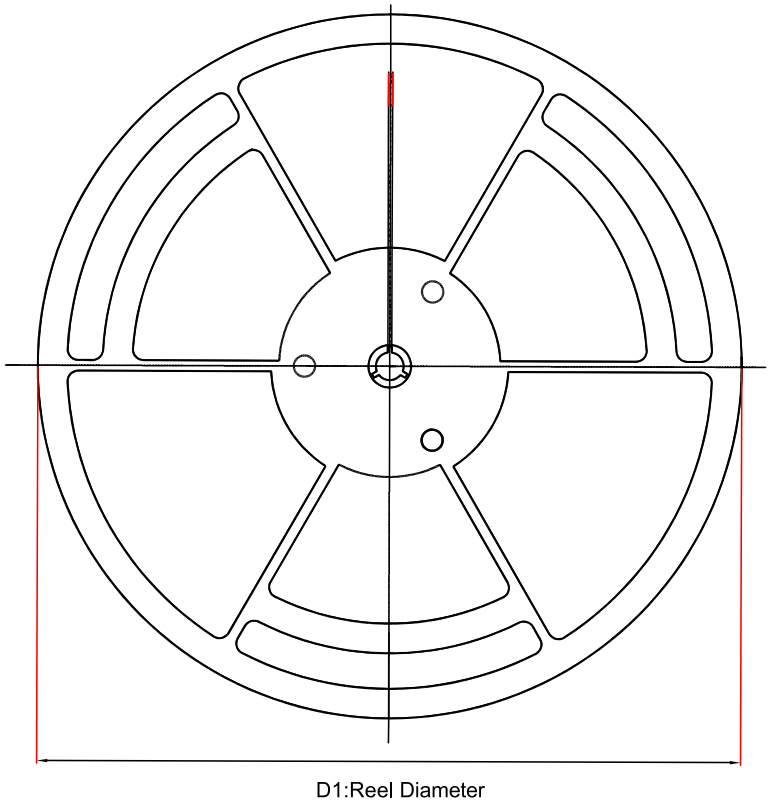
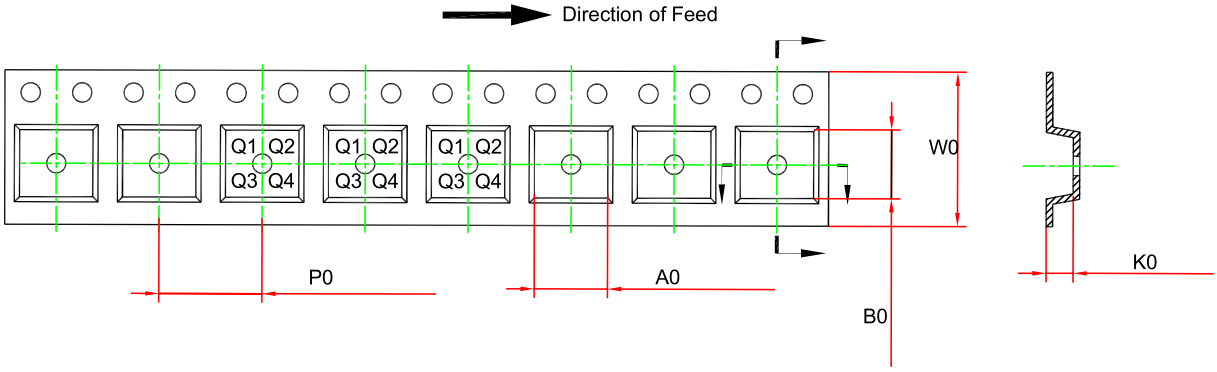


Figure 15. TIA Circuit Layout

Tape and Reel Information





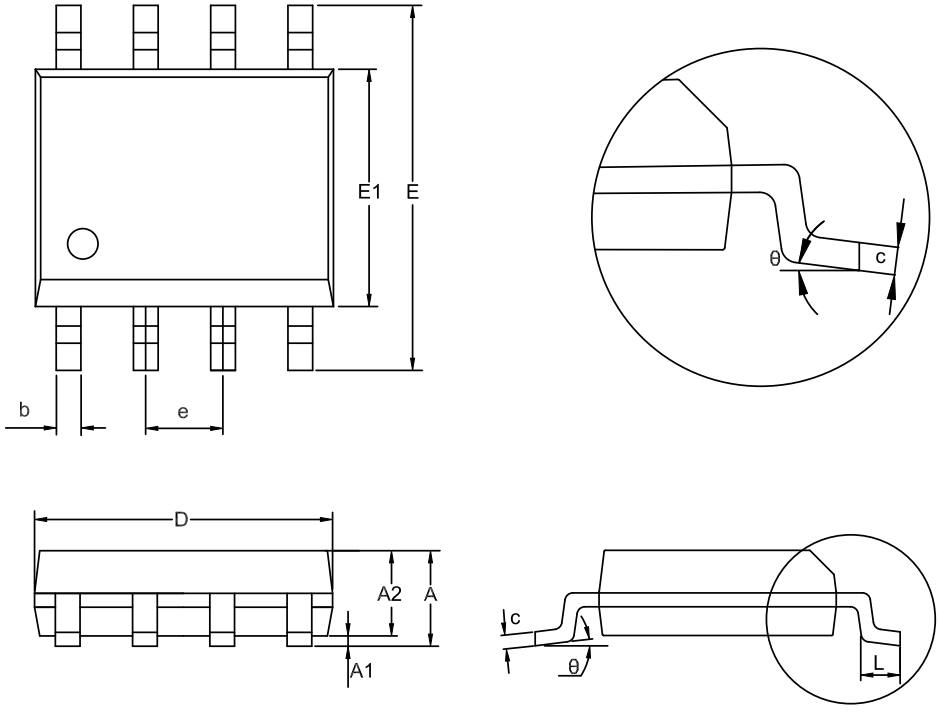
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm) (1)	B0 (mm) (1)	K0 (mm) (1)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPA3530-SO1R	SOP8	330	17.6	6.5	5.4	2	8	12	Q1

(1) The value is for reference only. Contact the 3PEAK factory for more information.

Package Outline Dimensions

SOP8

Package Outline Dimensions SO1(SOP-8-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPA3530-SO1R	−40 to 125°C	SOP8	A3530	2	Tape and Reel, 4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

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