±12K ESD Protection, Dedicated RS-485 Driver or Receiver

Features

- **Exceeds Requirements of EIA-485 Standard**
- **Hot Plug Circuitry - Tx and Rx Outputs Remain Three-State During Power-up/Power-down**
- **TP8481 is a pure RS485 Driver (Tx); TP8480 is a pure RS485 Receiver (Rx)**
- **Data Rate: Up to 250 kbps**
- **Full Fail-safe (Open, Short, Terminated) Receivers**
- **Up to 256 Nodes on a Bus (1/8 unit load)**
- **Wide Supply Voltage 3V to 5.5V**
- **SOP8 Package for Backward Compatibility**
- **Bus-Pin Protection:**
  - **±12 kV HBM protection**

Applications

- Industrial Automation
- HVAC Systems
- Process Control
- DMX512-Networks
- Battery-Powered Applications

Description

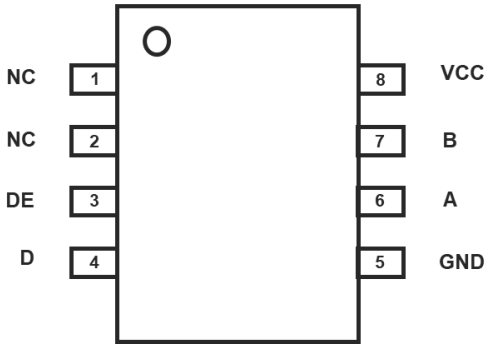
The TP8481/0 is 3V~5.5V powered transceivers that meet the RS-485 and RS-422 standards for balanced communication. Driver outputs and receiver inputs are protected against ±12kV ESD strikes without latch-up.

Transmitters in this family deliver exceptional differential output voltages (2.5V min/5Vcc), into the RS-485 required 54Ω load, for better noise immunity, or to allow up to eight 120Ω terminations in “star” topologies. These devices have very low bus currents so they present a true “1/8 unit load” to the RS-485 bus. This allows up to 256 transceivers on the network without using repeaters. Receiver (Rx) inputs feature a “Full Fail-Safe” design, which ensures a logic high Rx output if Rx inputs are floating, shorted, or on a terminated but undriven bus. Rx outputs feature high drive levels - typically 25mA @ VOL = 1V (to ease the design of optocoupled isolated interfaces).

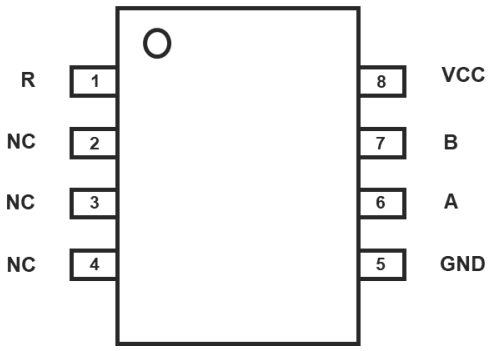
The TP8481/0 is available in an SOP8 package, and is characterized from –40°C to 125°C.

Pin Configuration (Top View)

TP8481
SOP8



TP8480
SOP8



Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
TP8481	TP8481-SR	8-Pin SOIC	Tape and Reel, 4,000	TP8481
TP8480	TP8480-SR	8-Pin SOIC	Tape and Reel, 4,000	TP8480

DRIVER PIN FUNCTIONS

INPUT	ENABLE	OUTPUTS		DESCRIPTION
D	DE	A	B	
NORMAL MODE				
H	H	H	L	Actively drives bus High
L	H	L	H	Actively drives bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drives bus High

RECEIVER PIN FUNCTIONS

DIFFERENTIAL INPUT	ENABLE	OUTPUT	DESCRIPTION
$V_{ID} = V_A - V_B$	/RE	R	
NORMAL MODE			
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled
Open, short, idle Bus	L	H	Indeterminate bus state

TP8481 pinout definition

Pin No.	Pin Name	I/O	Description
1	NC		
2	NC		
3	DE	Digital input	Driver Output Enable.
4	D	Digital input	Driver Input.
5	GND	Ground	Ground.
6	A	Bus input/output	Noninverting Receiver Input A and Noninverting Driver Output A.
7	B	Bus input/output	Inverting Receiver Input B and Inverted Driver Output B.
8	V_{CC}	Power	Power Supply.

TP8480 pinout definition

Pin No.	Pin Name	I/O	Description
1	R	Digital output	Receiver Output.
2	NC		
3	NC		
4	NC		
5	GND	Ground	Ground.
6	A	Bus input/output	Noninverting Receiver Input A and Noninverting Driver Output A.
7	B	Bus input/output	Inverting Receiver Input B and Inverted Driver Output B.
8	V_{CC}	Power	Power Supply.

Absolute Maximum Ratings

V_{DD} to GND.....-0.3V to +7V

Input Voltages DI, DE, RE .....-0.3V to (VCC + 0.3V)

Input/Output Voltages A, B..... -9V to +14V

A/Y, B/Z, A, B (Transient Pulse through 100Ω, Note 1) ..... ±100V

RO..... -0.3V to (VCC +0.3V)

Short Circuit Duration A,B.....Continuous

ESD Rating..... See Specification Table

Recommended Operating Conditions Note 2

Supply Voltage.....3V~5.5V

Temperature Range.....-40°C to +125°C

Bus Pin Common Mode Voltage Range ..... -8V to +13V

Thermal Resistance, ΘJA (Typical)

8-Pin SOIC Package .....158°C/W

Maximum Junction Temperature (Plastic Package) .....+150°C

Maximum Storage Temperature Range ..... -65°C to +150°C

Note 1: Tested according to TIA/EIA-485-A, Section 4.2.6 (±100V for 15μs at a 1% duty cycle).

Note 2: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Electrical Characteristics

Test Conditions: VCC = 5V, Over operating free-air temperature range(unless otherwise noted)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$\|V_{OD}\|$	Driver differential-output voltage magnitude	RL = 60 Ω	See Figure 1B		2.6		V
		RL = 54 Ω with V_A or V_B from –7 to +12 V, V_{CC} = 5V (RS-485)	See Figure 1A	2.1	2.5		
		RL = 54 Ω with V_A or V_B from –7 to +12 V, V_{CC} = 3V (RS-485)		1	1.5		
		RL = 100 Ω(RS-422)			3		
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential-output voltage	RL = 54 Ω, CL=50 pF, V_{CC} = 5V	See Figure 1A	-0.2	-0.002	0.2	V
$V_{OC(SS)}$	Steady-stage common-mode output voltage	Center of two 27 Ω load resistors	See Figure 1A		V_{CC}/2		V
ΔV_{OC}	Change in differential driver common-mode output voltage				0.05		V
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage				0.5		
C_{OD}	Differential output capacitance				8		pF
V_{IT+}	Positive-going receiver differential-input voltage threshold					-40	mV
V_{IT-}	Negative-going receiver differential-input voltage threshold			-200			mV
V_{HYS}(1)	Receiver differential-input voltage threshold hysteresis ($V_{IT+} – V_{IT–}$)				110		mV
V_{IH}	Logic Input High Voltage	DI, DE, $\overline{RE}$		2			V
V_{IL}	Logic Input Low Voltage	DI, DE, $\overline{RE}$				0.4	V
V_{OH}	Receiver high-level output voltage	I_{OH}= -8 mA		4	4.5		V
V_{OL}	Receiver low-level output voltage	I_{OL}= 8 mA			0.2	0.4	V
I_I	Driver input, driver enable and receiver enable input current			-2	0.01	2	μA
I_{OZ}	Receiver high-impedance output current	VO = 0 V or VCC, /RE at VCC		-2	0.01	2	μA
$\|I_{OS}\|$	Driver short-circuit output current	$\|I_{OS}\|$ with V_A or V_B from –7 to +12 V		75	80	115	mA
I_I	Bus input current(driver disabled)	V_{CC} = 4.5 to 5.5 V or V_{CC} = 0 V, DE at 0 V	VI= 12 V		100	150	μA
			VI= -7 V	-150	-80		
I_{CC}	Supply current(quiescent)	Driver and receiver enabled	DE = V_{CC}, /RE = GND, No LOAD		695	900	μA
		Driver enabled, receiver disabled	DE = V_{CC}, /RE = V_{CC}, No LOAD		270	350	
		Driver disabled, receiver enabled	DE = GND, /RE = V_{CC}, No LOAD		480	600	

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
		Driver and receiver disabled	DE = GND, /RE = V_{CC}, D= V_{cc} No LOAD		1.4	5	

Switching CHARACTERISTICS

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER							
t_r, t_f	Driver differential-output rise and fall times	RL = 54 Ω, CL=50pF	See Figure 2		620		ns
t_{PHL}, t_{PLH}	Driver propagation delay				340		
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$				23		
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 3		250		ns
t_{PHZ}, t_{PLZ}	Driver enable time	Receiver enabled			562		ns
		Receiver disabled			562		
RECEIVER							
t_r, t_f	Receiver output rise and fall times	CL=15 pF	See Figure 5		12.4		ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				960		
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$				40		
t_{PHZ}, t_{PLZ}	Receiver disable time				7		ns
t_{PZL}, t_{PZH}	Receiver enable time	Driver enabled	See Figure 6		70		ns
		Driver disabled	See Figure 6		989		
ESD							
RS-485 Pins (A, B)		Human Body Model, From Bus Pins to GND			±12		kV
All Other Pins		Human Body Model, per MIL-STD-883			±2		kV

Test Circuits and Waveforms

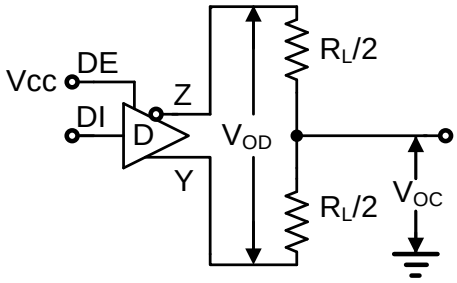


FIGURE 1A. VOD AND VOC

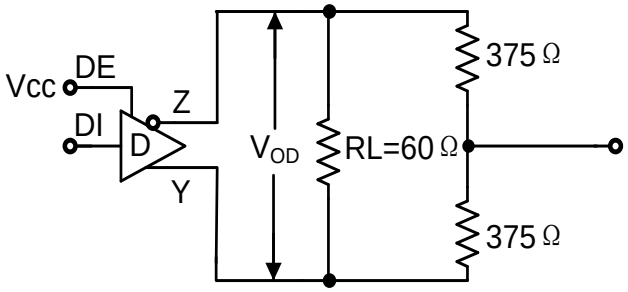


FIGURE 1B. VOD WITH COMMON MODE LOAD

FIGURE 1. DC DRIVER TEST CIRCUITS

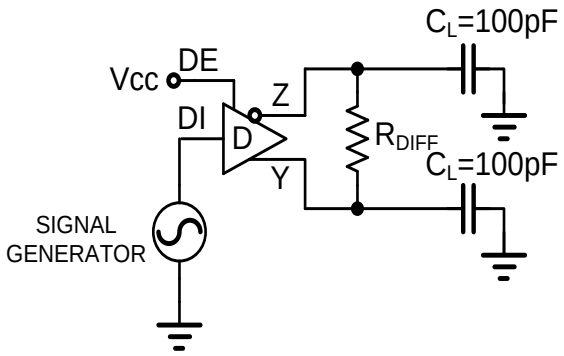


FIGURE 2A. TEST CIRCUIT

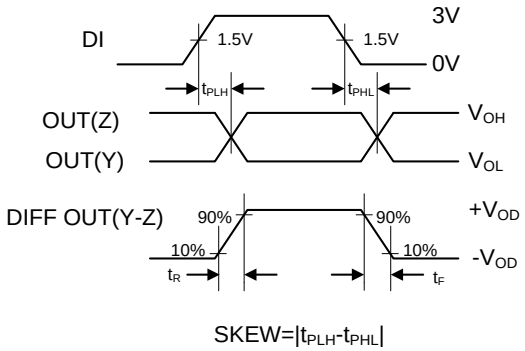
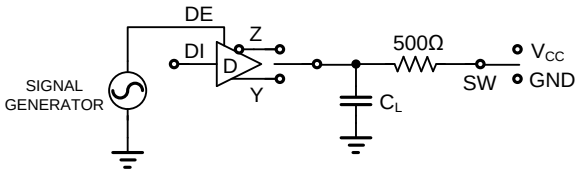


FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES



PARAMETER	OUTPUT	RE	DI	SW	CL (pF)
tHZ	Y/Z	X	1/0	GND	15
tLZ	Y/Z	X	0/1	VCC	15
tZH	Y/Z	0	1/0	GND	100
tZL	Y/Z	0	0/1	VCC	100
tZH(SHDN)	Y/Z	1	1/0	GND	100
tZL(SHDN)	Y/Z	1	0/1	VCC	100

FIGURE 3A. TEST CIRCUIT

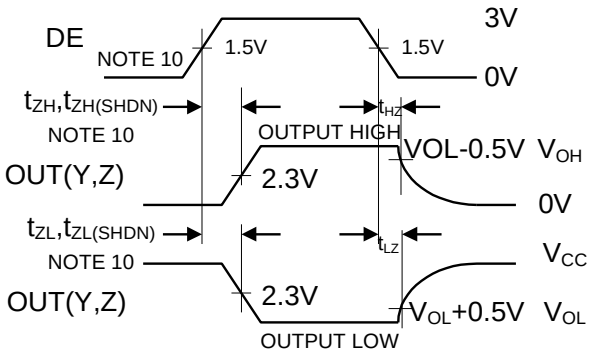


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. DRIVER ENABLE AND DISABLE TIMES

Test Circuits and Waveforms(continue)

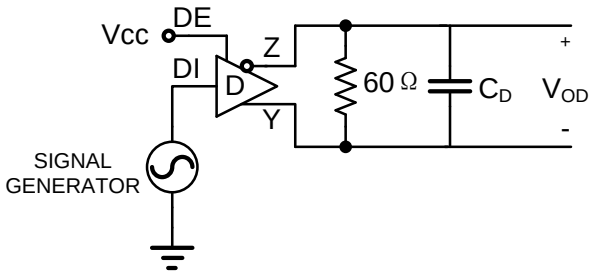


FIGURE 4A. TEST CIRCUIT

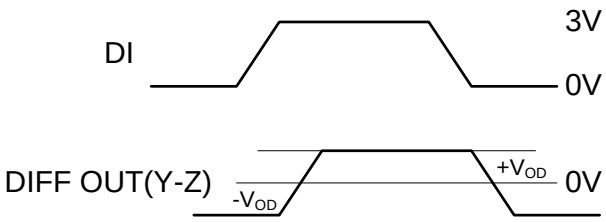


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. DRIVER DATA RATE

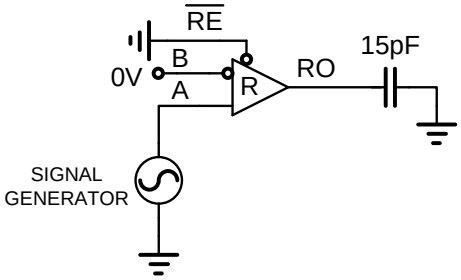


FIGURE 5A. TEST CIRCUIT

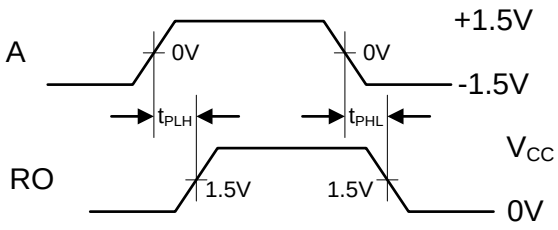
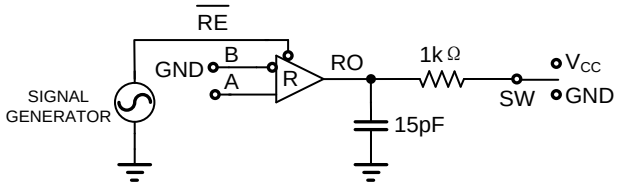


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. RECEIVER PROPAGATION DELAY AND DATA RATE



PARAMETER	DE	A	SW
tHZ	1	+1.5V	GND
tLZ	1	-1.5V	VCC
tZH	1	+1.5V	GND
tZL	1	-1.5V	VCC
tZH(SHDN)	0	+1.5V	GND
tZL(SHDN)	0	-1.5V	VCC

FIGURE 6A. TEST CIRCUIT

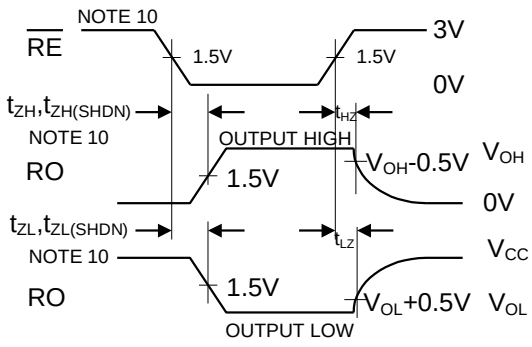
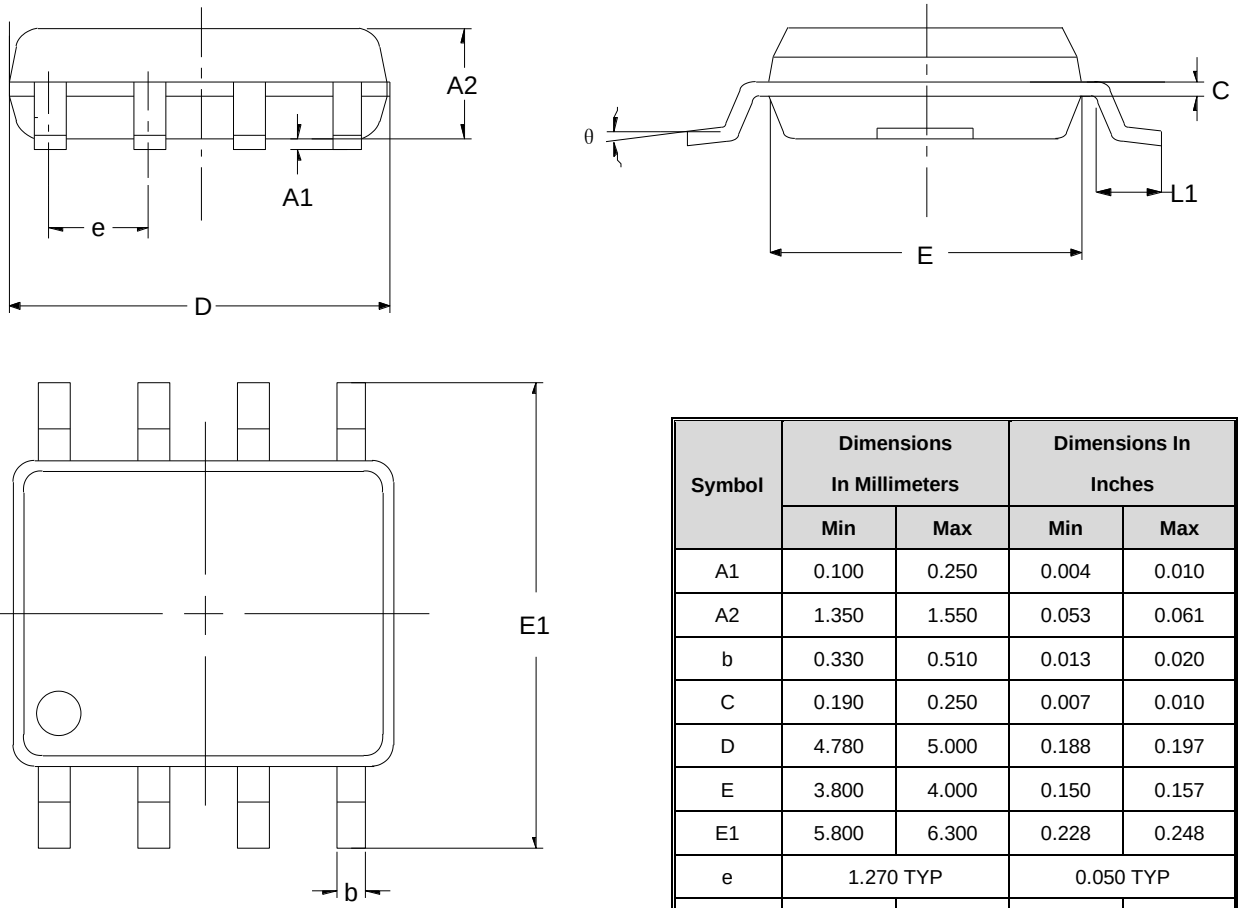


FIGURE 6B. MEASUREMENT POINTS

FIGURE 6. RECEIVER ENABLE AND DISABLE TIMES

Package Outline Dimensions

SR(SOP8)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270 TYP		0.050 TYP	
L1	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°