



Features

- Low Offset Voltage: 20 µV (Max)
- Zero Drift: 0.01 µV/°C
- Ultra-Low Noise:
 - Input Noise Voltage: 17 nV/√Hz at 1 kHz
 - 0.1-Hz to 10-Hz Noise Voltage: 370 nV_{PP}
 - 1/f Noise Corner down to 0.1 Hz
- 3.3-MHz Bandwidth, 2.5-V/µs Slew Rate
- Low Supply Current: 470 µA per Amplifier
- Single-Supply Operation down to +1.8 V
- Low Input Bias Current: 60 pA
- High-Gain, 127-dB High CMRR and PSRR
- Overload Recovery Time: 35 µs
- Rail-to-Rail Input and Output Swing
- Operating Temperature Range: -40°C to 125°C

Applications

- Medical Instrumentation
- Temperature Measurements
- Precision Current Sensing
- Precision Low-Drift, Low-Frequency ADC Drivers
- Process Control Systems
- Precision Voltage Reference Buffers

Description

The TP5591/TP5592/TP5594 is a series of single, dual and quad chopper-stabilized zero-drift operational amplifiers optimized for single or dual supply operation from 1.8 V to 5.5 V or ± 0.9 V to ± 2.75 V. The TP559x series features a very low input offset voltage and low noise with the 1/f noise corner down to 0.1 Hz. The series is designed to have a low offset voltage and offset temperature drift, a wide gain bandwidth, and a rail-to-rail input and output swing while minimizing power consumption.

The TP559x series can provide a low offset voltage (20 μV max) and a near-zero drift over time and temperature with excellent CMRR and PSRR.

The TP5591 (single version) is available in the SOT353 (SC70-5), SOT23-5, and SOP8 packages. The TP5592 (dual version) is offered in the MSOP8 and SOP8 packages. The TP5594 (quad version) is available in the TSSOP14 and SOP14 packages. All versions are specified for operation from -40° C to 125° C.



TP5591/TP5592/TP5594

Low-Noise, 1.8-V, 3.3-MHz, RRIO, Zero-Drift Operational Amplifier

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Revision History

Date	Revision	Notes
2022-04-30	Rev.A.3	Updated Order Information.
2025-01-04	Rev.A.4	Added the Tape and Reel Information. The following updates are all about the new datasheet formats or typo, the actual product remains unchanged. Updated to a new datasheet format. Updated the Package Outline Dimensions.



Pin Configuration and Functions

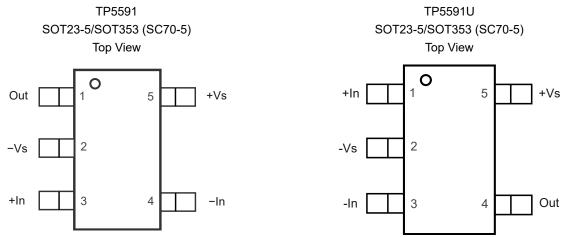


Table 1. Pin Functions: TP5591, TP5591U

Pin	No.	N		Description	
TP5591	TP5591U	Name	I/O	Description	
1	4	Out	0	Amplifier output. The voltage range extends to within mV of each supply rail.	
2	2	-Vs	Power Supply		
3	1	+In	I	Non-inverting input of the amplifier.	
4	3	-In	I	Inverting input of the amplifier.	
5	5	+Vs	Power Supply	Positive power supply. Typically, the voltage is from 1.8 V to 5.5 V. Split supplies are possible when the voltage between +V _S and $-V_S$ is between 1.8 V and 5.5 V. A bypass capacitor of 0.1 μ F as close to the part as possible should be used between the power supply pins or between supply pins and GND.	



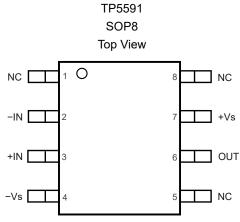
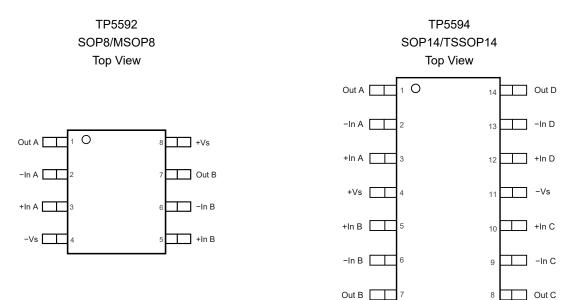


Table 2. Pin Functions: TP5591

Pin No.	Name	I/O	Description
1	NC		Not connected.
2	-IN	I	Inverting input of the amplifier.
3	+IN	I	Non-inverting input of the amplifier.
4	-Vs	Power Supply	Negative power supply. It is normally tied to GND. It can also be tied to a voltage other than GND when the voltage between +V _S and –V _S is from 1.8 V to 5.5 V. If it is not connected to GND, bypass it with a capacitor of 0.1 μ F as close to the part as possible.
5	NC		Not connected.
6	Out	0	Amplifier Output. The voltage range extends to within mV of each supply rail.
7	+Vs	Power Supply	Positive power supply. Typically, the voltage is from 1.8 V to 5.5 V. Split supplies are possible when the voltage between +V _S and $-V_S$ is between 1.8 V and 5.5 V. A bypass capacitor of 0.1 μ F as close to the part as possible should be used between the power supply pins or between supply pins and GND.
8	NC		Not connected.







Pin	No.	N		Description	
TP5592	TP5594	Name	I/O	Description	
1	1	Out A	0	Amplifier output. The voltage range extends to within mV of each supply rail.	
2	2	−In A	I	Inverting input of the amplifier.	
3	3	+In A	Ι	Non-inverting input of the amplifier.	
4	11	-Vs	Power Supply	Negative power supply. It is normally tied to GND. It can also be tied to a voltage other than GND when the voltage between +V _S and $-V_S$ is from 1.8 V to 5.5 V. If it is not connected to GND, bypass it with a capacitor of 0.1 μ F as close to the part as possible.	
5	5	+In B	I	Non-inverting input of the amplifier.	
6	6	–In B	I	Inverting input of the amplifier.	
7	7	Out B	0	Amplifier output. The voltage range extends to within mV of each supply rail.	
8	4	+Vs	Power Supply	Positive power supply. Typically, the voltage is from 1.8 V to 5.5 V. Split supplies are possible when the voltage between $+V_S$ and $-V_S$ is between 1.8 V and 5.5 V. A bypass capacitor of 0.1 μ F as close to the part as possible should be used between the power supply pins or between supply pins and GND.	
	8	Out C	0	Amplifier output. The voltage range extends to within mV of each supply rail.	
	9	−In C	I	Inverting input of the amplifier.	
	10	+In C	I	Non-inverting input of the amplifier.	
	12	+In D	I	Non-inverting input of the amplifier.	
	13	-In D	I	Inverting input of the amplifier.	
	14	Out D	0	Amplifier output. The voltage range extends to within mV of each supply rail.	



Specifications

Absolute Maximum Ratings (1)

	Parameter	Min	Max	Unit
	Supply Voltage		6	V
	Input Voltage	(-V _S) - 0.1	(+V _S) + 0.1	V
	Input Current: +IN, -IN ⁽²⁾	-20	+20	mA
	Output Current: OUT	-60	+60	mA
	Output Short-Circuit Duration ⁽³⁾		Indefinite	
	Current at Supply Pins	-50	+50	mA
TJ	Maximum Junction Temperature		150	°C
TA	Operating Temperature Range	-40	125	°C
T _{STG}	Storage Temperature Range	-65	150	°C
TL	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500 mV beyond the power supply, the input current should be limited to less than 10 mA.

(3) A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. The thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
НВМ	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	7	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information

Package Type	θιΑ	θις	Unit
SOT23-5	200		°C/W
MSOP8	210		°C/W
SOP8	158		°C/W
SOT353 (SC70-5)	250		°C/W
SOP14	83		°C/W
TSSOP14	100		°C/W

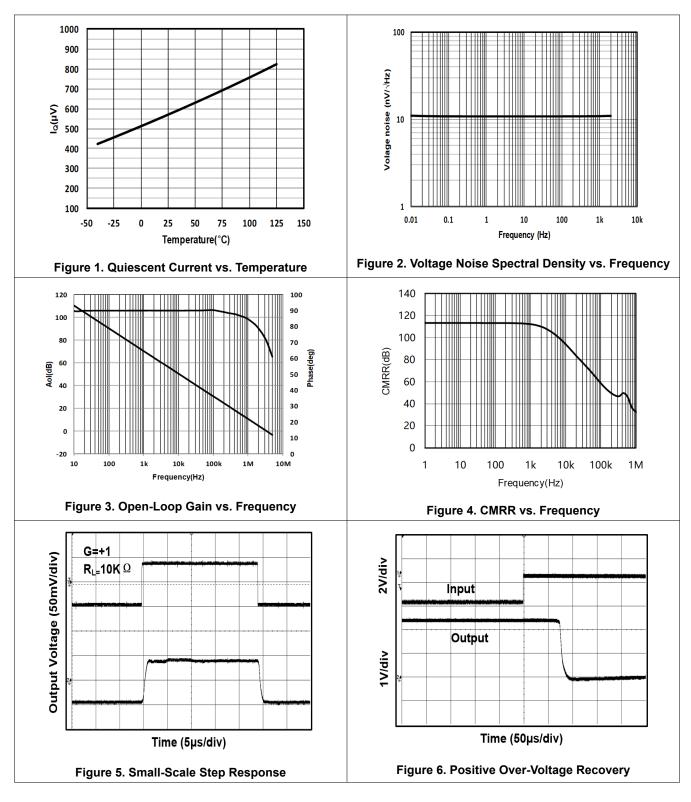


Electrical Characteristics

All test conditions: V_S = 5 V, T_A = 27°C, R_L = 10 k Ω , V_{CM} = V_{DD} / 2, unless otherwise noted.

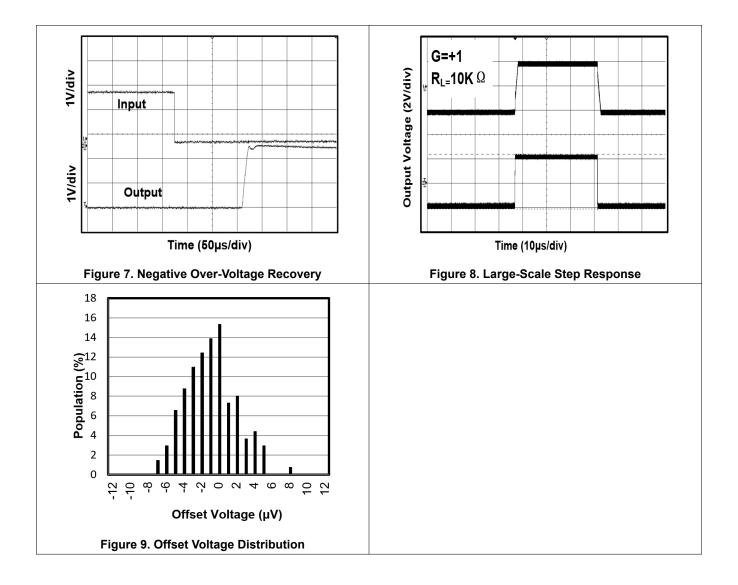
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Vs	Supply Voltage Range		1.8		5.5	V
		TP5591		1200	1400	μA
	Quiescent Current per Amplifier	TP5592/TP5594		550	950	μA
		V _{CM} = 0.05 V to 4.95 V		±5	±20	μV
Vos	Input Offset Voltage	V _S = 1.8 V, V _{CM} = 0.9 V		±5	±20	μV
dVOS/dT	Vs Temperature			0.01		μV/°C
PSRR	V _S Power Supply	$V_{\rm S}$ = 3 V to 5 V	95	130		dB
		f = 0.01 Hz to 1 Hz		0.1		μV _{pp}
Vn	Input Voltage Noise	f = 0.1 Hz to 10 Hz		0.37		μV _{pp}
en	Input Voltage Noise Density	f = 1 kHz		17		nV/√Hz
C _{IN} Input Capacito		Differential mode		3		pF
	Input Capacitor	Common mode		2		pF
	Input Bias Current			±60	±200	pА
IB	Over Temperature			±800		pА
los	Input Offset Current			±100	±400	pА
V _{CM}	Common-Mode Voltage Range		(-V _S) - 0.1		(+V _S) +0.1	V
CMRR	Common-Mode Rejection Ratio	V _{CM} = 0.5 V to 4.5 V	110	127		dB
Vo	Output Voltage Swing from Rail	R _L = 10 kΩ		5	25	mV
I _{SC}	Short-Circuit Current			±60		mA
GBWP	Unity Gain Bandwidth	C _L = 100 pF		3.3		MHz
SR	Slew Rate	G = +1, C _L = 100 pF		2.5		V/µs
t _{OR}	Overload Recovery Time	G = -10		35		μs
ts	Settling Time, 0.01%	C _L = 100 pF		20		μs
Avol	Open-Loop Voltage Gain	(−V _S) + 100 mV < V ₀ < (+V _S) − 100 mV, R _L = 100 kΩ	100	130		dB





Typical Performance Characteristics







TP5591/TP5592/TP5594

Low-Noise, 1.8-V, 3.3-MHz, RRIO, Zero-Drift Operational Amplifier

Detailed Description

Overview

The TP559x is a series of zero-drift, rail-to-rail operation amplifiers that can be run from a single-supply voltage. The TP559x series uses an auto-calibration technique with a time-continuous 3.3-MHz operational amplifier in the signal path while consuming a supply current of only 470 μ A per channel. The amplifier is zero-corrected with an ~550-kHz clock. Upon power-up, the amplifier requires approximately 100 μ s to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.



Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

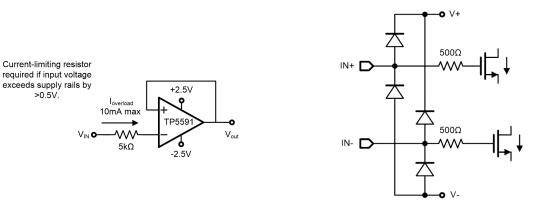
Application Information

Rail-to-Rail Input and Output

The TP559x series features rail-to-rail inputs and outputs with a supply voltage from 1.8 V to 5.5 V. This allows the inputs of the amplifier to have a wide common-mode range (50 mV beyond supply rails) while maintaining high CMRR (127 dB) and maximizes the signal to noise ratio of the amplifier by having the V_{OH} and V_{OL} levels at the +V_S and -V_S rails, respectively.

Input Protection

The TP559x series has internal ESD protection diodes that are connected between the inputs and supply rails. When either input exceeds one of the supply rails by more than 300 mV, the ESD diodes become forward-biased and large amounts of current begin to flow through them. Without current limiting, this excessive fault current causes permanent damage to the device. Thus an external series resistor must be used to ensure the input currents never exceed 10 mA.



INPUT ESD DIODE CURRENT LIMITING- UNITY GAIN

Figure 10. Input Protection

Low Input Referred Noise

The flicker noise, as known as the 1/f noise, is inherent in semiconductor devices, and increases as the frequency decreases. So at lower frequency, the flicker noise dominates, causing higher degrees of error for sub-Hertz frequencies or DC precision applications.

The TP559x is a series of chopper-stabilized amplifiers, and the flicker noise is reduced greatly because of this technique. This reduction in the 1/f noise allows the TP559x series to have much lower noise at DC and low frequency compared to standard low-noise amplifiers.



Residual Voltage Ripple

The chopping technique can be used in the design of the amplifier due to the internal notch filter. Although the choppingrelated voltage ripple is suppressed, a higher-noise spectrum exists at the chopping frequency and its harmonics due to the residual ripple.

So if the frequency of the input signal is near the chopping frequency, the signal may be interfered by the residue ripple. To suppress the noise at the chopping frequency, it is recommended that a post filter be placed at the output of the amplifier.

Broad Band and External Resistor Noise Considerations

The total broadband noise output from any amplifier is primarily a function of three types of noise: the input voltage noise from the amplifier, the input current noise from the amplifier, and the thermal (Johnson) noise from the external resistors used around the amplifier. These noise sources are not correlated with each other and their combined noise can be summed in a root sum squared manner. The full equation is given as:

$$e_{n}$$
total = $\left[e_{n}^{2} + 4kTR_{S} + (i_{n} \times R_{S})^{2}\right]^{1/2}$ (1)

Where:

en = the input voltage noise density of the amplifier;

in = the input current noise of the amplifier;

 R_{S} = the source resistance connected to the noninverting terminal;

k = the Boltzmann's constant (1.38 × 10^{-23} J/K).

T= the ambient temperature in Kelvin (K).

The total equivalent rms noise over a specific bandwidth is expressed as:

$$e_{n.rms} = e_n total \times \sqrt{BW}$$

The input voltage noise density (e_n) of the TP559x series is 17 nV/ \sqrt{Hz} , and the input current noise can be neglected. When the source resistance is 190 k Ω , the voltage noise contribution from the source resistor and the amplifier are equal. With a source resistance greater than 190 k Ω , the overall noise of the system is dominated by the Johnson noise of the resistor itself.

High Source Impedance Application

The TP559x series uses switches at the input of the chopper amplifier, and the input signal is chopped at 125 kHz to reduce the input offset voltage down to 20 μ V. The dynamic behavior of these switches induces a charge injection current to the input terminals of the amplifier. The charge injection current has a DC path to ground through the resistances seen at the input terminals of the amplifier. Higher input impedance causes an apparent shift in the input bias current of the amplifier.

Because the chopper amplifier has charge injection currents at each terminal, the input offset current is larger than that of standard amplifiers. The I_{OS} of the TP559x series are 150 pA under the typical condition. So the input impedance should be balanced across each input. The input impedance of the amplifier should be matched between the IN+ and IN- terminals to minimize the total input offset current. Input offset currents show up as an additional output offset voltage, as shown in the following equation:

$$v_{OS, \text{ total}} = v_{OS} - R_f \times I_{OS}$$
(3)

For a gain configure using a 1-M Ω feedback resistor, a 150-pA total input offset current has an additional output offset voltage of 0.15 mV. By keeping the input impedance low and balanced across the amplifier inputs, the input offset current effect can be suppressed efficiently.

(2)



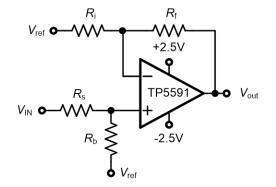


Figure 11. Circuit Implication for Reducing Input Offset Current Effect

PCB Surface Leakage

In applications where the low input bias current is critical, the Printed Circuit Board (PCB) surface leakage effects need to be considered. The surface leakage is caused by humidity, dust, or other contamination on the board. It is recommended to use the multi-layer PCB layout and route the –IN and +IN signal of the device under the PCB surface.

An effective way to reduce surface leakage is to use a guard ring around the sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 12 for inverting gain applications.

- 1. For noninverting gain and unity-gain buffers:
 - a. Connect the noninverting pin (V_{IN+}) to the input with a wire that does not touch the PCB surface.
 - b. Connect the guard ring to the inverting input pin (V_{IN-}). This biases the guard ring to the common-mode input voltage.
- 2. For inverting gain and transimpedance gain amplifiers (convert current to voltage, such as photo detectors):
 - a. Connect the guard ring to the noninverting input pin (V_{IN+}). This biases the guard ring to the same reference voltage as the operational amplifier (e.g., V_{DD} / 2 or ground).
 - b. Connect the inverting pin (V_{IN-}) to the input with a wire that does not touch the PCB surface.

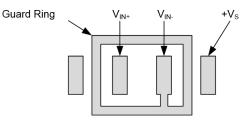


Figure 12. The Layout of Guard Ring



Typical Application

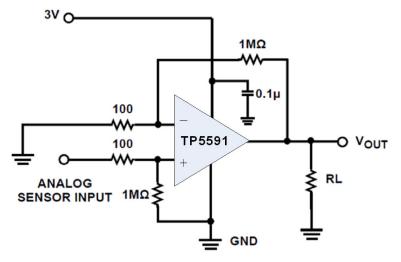


Figure 13. Single-Supply, High-Gain Amplifier, Av = 10,000 V/V

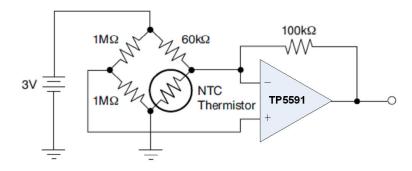
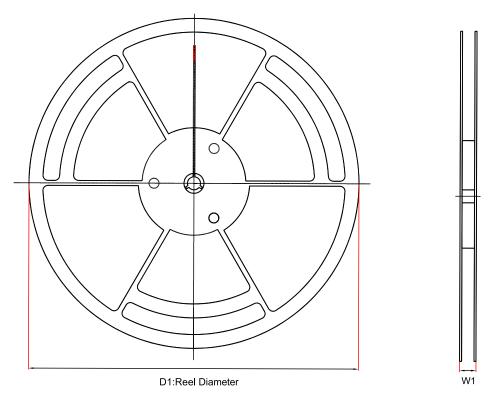
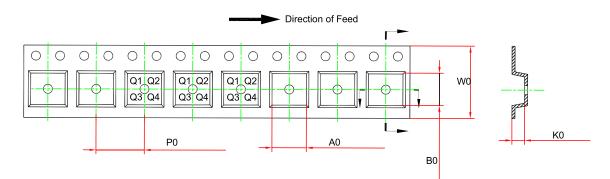


Figure 14. Thermistor Measurement



Tape and Reel Information





Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm) ⁽¹⁾	B0 (mm) ⁽¹⁾	K0 (mm) ⁽¹⁾	P0 (mm)	W0 (mm)	Pin1 Quadrant
TP5591U-CR	SOT353	178	12.1	2.4	2.5	1.2	4	8	Q3
TP5591-TR	SOT23-5	180	12	3.3	3.25	1.4	4	8	Q3
TP5591-SR	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TP5592-SR	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TP5592-VR	MSOP8	330	17.6	5.3	3.4	1.3	8	12	Q1
TP5594-SR	SOP14	330	21.6	6.5	9.3	2.1	8	16	Q1
TP5594-TR	TSSOP14	330	17.6	6.8	5.5	1.5	8	12	Q1



TP5591/TP5592/TP5594

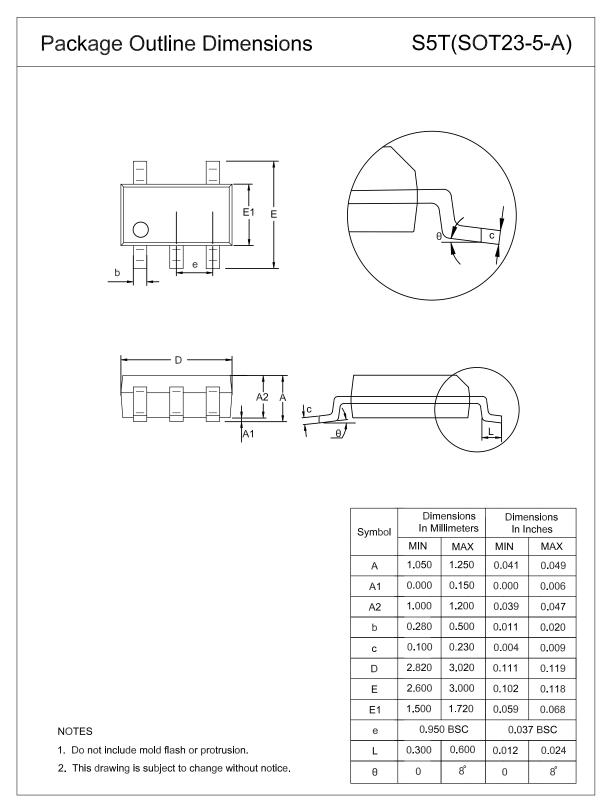
Low-Noise, 1.8-V, 3.3-MHz, RRIO, Zero-Drift Operational Amplifier

(1) The value is for reference only. Contact the 3PEAK factory for more information.



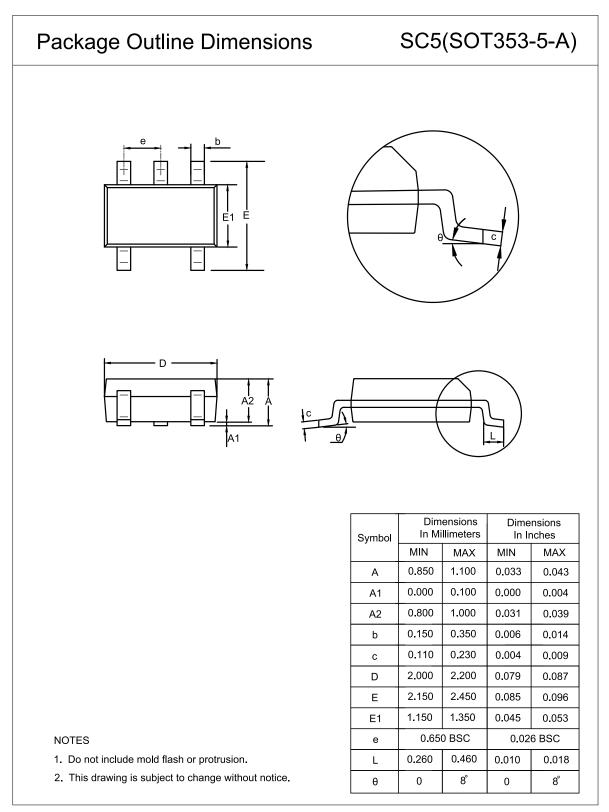
Package Outline Dimensions

SOT23-5



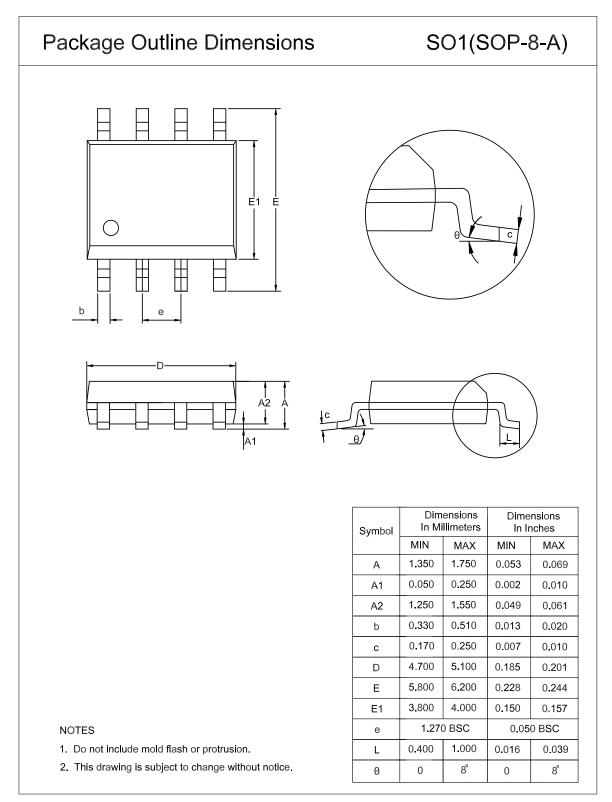


SOT353 (SC70-5)



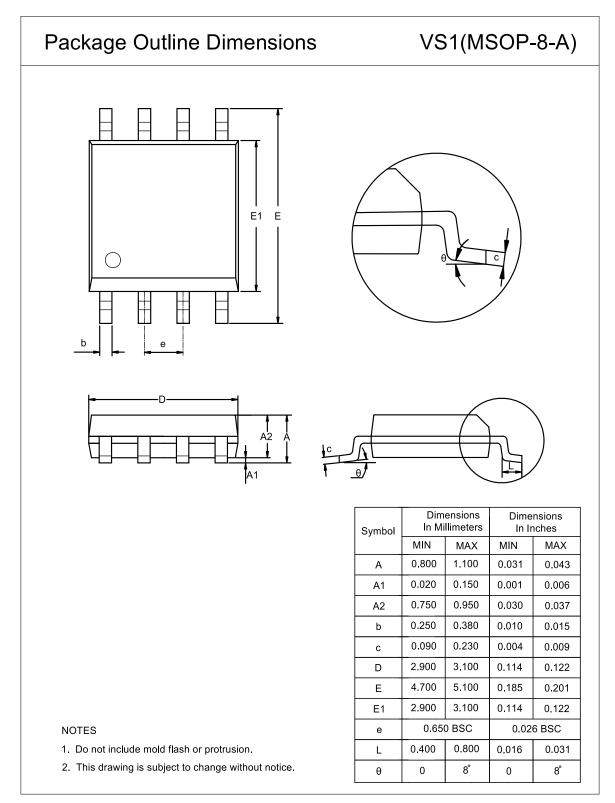


SOP8



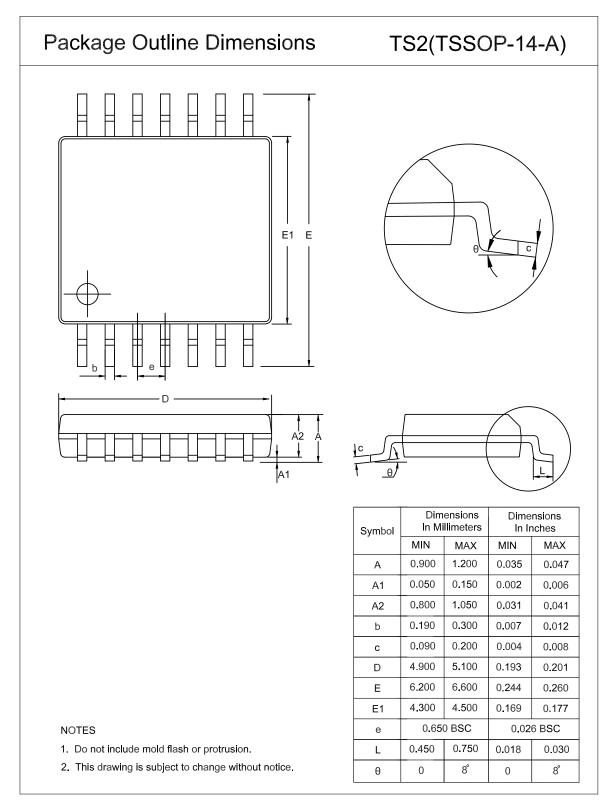


MSOP8



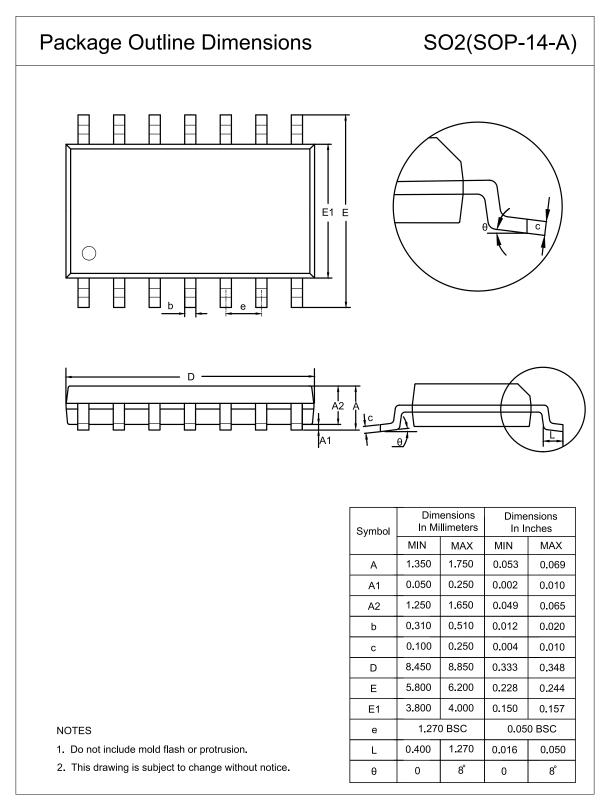


TSSOP14





SOP14





Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TP5591-TR	−40 to 125°C	SOT23-5	E91T	3	Tape and Reel, 3,000	Green
TP5591-SR	−40 to 125°C	SOP8	TP5591	3	Tape and Reel, 4,000	Green
TP5591U-CR	−40 to 125°C	SOT353 (SC70-5)	91V	3	Tape and Reel, 3,000	Green
TP5592-SR	−40 to 125°C	SOP8	TP5592	3	Tape and Reel, 4,000	Green
TP5592-VR	−40 to 125°C	MSOP8	TP5592	3	Tape and Reel, 3,000	Green
TP5594-SR	−40 to 125°C	SOP14	TP5594	3	Tape and Reel, 2,500	Green
TP5594-TR	-40 to 125°C	TSSOP14	TP5594	3	Tape and Reel, 3,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.



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TP5591/TP5592/TP5594

Low-Noise, 1.8-V, 3.3-MHz, RRIO, Zero-Drift Operational Amplifier

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