68-ns, 1.8-V, Ultra-Low-Power, RRI, Push-Pull Output Comparator

Features

- Fast Response Time: 68-ns Propagation Delay
- Ultra-Low Supply Current: 46 μA per Channel
- Offset Voltage: ± 3.0 mV Maximum
- Offset Voltage Temperature Drift: 0.3 μV/°C
- Input Bias Current: 6 pA Typical
- Internal Hysteresis Ensures Clean Switching
- Input Common-Mode Range Extends 200 mV
- No Phase Reversal for Overdriven Inputs
- Push-Pull, CMOS/TTL Compatible Output
- Shut-down Function (TP1941N Only)
- Output Latch (TP1941NU Only)
- Down to 1.8-V Supply Voltage: 1.75 V to 5.5 V
- Green, Space-Saving SC70 Package Available

Applications

- High-Speed Line or Digital Line Receivers
- High Speed Sampling Circuits
- Peak and Zero-Crossing Detectors
- Threshold Detectors/Discriminators
- Sensing at Ground or Supply Line
- Logic Level Shifting or Translation
- Window Comparators
- IR Receivers
- Clock and Data Signal Restoration
- Telecom, Portable Communications
- Portable and Battery Powered Systems

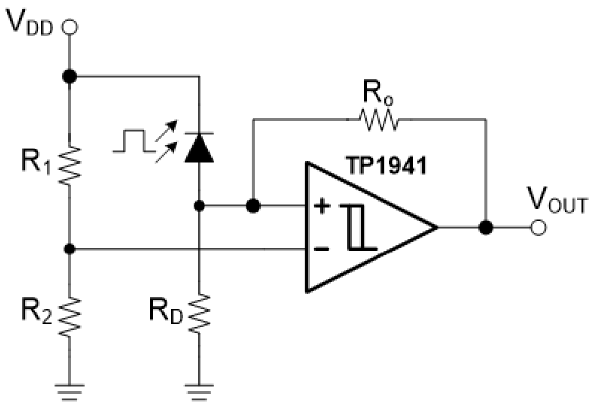
Description

The 3PEAK INCORPORATED TP194x CMOS/TTL compatible comparators are offered in single, dual, and quad configurations, and is exceptionally versatile and easy to use.

The TP194x series incorporates proprietary and patented design techniques of the 3PEAK to achieve the ultimate combination of high-speed (a 68-ns propagation delay under a 1.75~5.5-V wide supply range) and low power consuming (a 46-μA quiescent current per comparator). These comparators are optimized for 1.75-V low-power, single-supply applications with greater than rail-to-rail input operation, and also operate with ±0.9-V to ±2.75-V dual supplies. The input common-mode voltage range extends 200 mV below ground and 200 mV above supply, allowing both ground and supply sensing. The internal input hysteresis eliminates the output switching due to the internal input noise voltage, reducing the current draw. The push-pull output supports the rail-to-rail output swing, and interfaces with the CMOS/TTL logic. The output toggle frequency can reach 4 MHz typical while limiting the supply current surges and dynamic power consumption during the switching.

The TP1941 single comparator is available in the shout-down function, output latch version, and the tiny SC70/SOT23 package for space-conservative designs. All devices are specified for the temperature range of –40°C to +125°C.

Typical Application Circuit



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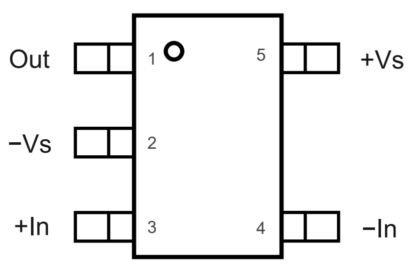
Revision History

Date	Revision	Notes
2022-04-29	Rev.1.6	Updated Order Information.
2023-03-13	Rev.1.7	The following updates are all about the new datasheet formats or typos, and the actual product remains unchanged. Updated Package Outline Dimensions. Updated Tape and Reel Information.
2024-01-11	Rev.1.8	The following updates are all about the new datasheet formats or typos, and the actual product remains unchanged. Updated the HBM value from 4500 to 4.5 kV. Updated the CDM value from 1500 to 1.5 kV.
2026-01-15	Rev.A.0	Updated Electrical Characteristics: Min of the supply voltage: from 1.8 V to 1.75 V. The following updates are all about the new datasheet formats or typos, and the actual product remains unchanged. • Updated to a new datasheet format. • Updated the Package Outline Dimensions. Updated Operating Temperature Range max value from 85 °C to 125 °C Updated Electrical Characteristics: • Changed V_{HYST} min value from 4 mV to 2 mV • Changed T_{PD+} conditions from Overdrive = 100 mV, V_{IN-} = 1.2 V to Overdrive = 100 mV, V_{IN+} = 1.2 V and from V_{IN+}0 to VCC, V_{IN-} = 1.2 V to V_{IN-}0 to VCC, V_{IN+} = 1.2 V • Changed T_{PD-} conditions from Overdrive = 100 mV, V_{IN-} = 1.2 V to Overdrive = 100 mV, V_{IN+} = 1.2 V and from V_{IN+} VCC to 0, V_{IN-} = 1.2 V to V_{IN-} VCC to 0, V_{IN+} = 1.2 V • Changed T_{PDSKEW} conditions from Overdrive = 100 mV, V_{IN-} = 1.2 V to Overdrive = 100 mV, V_{IN+} = 1.2 V

Pin Configuration and Functions



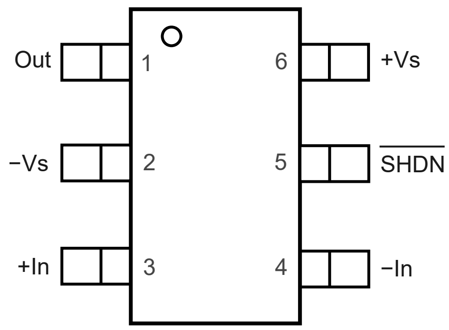
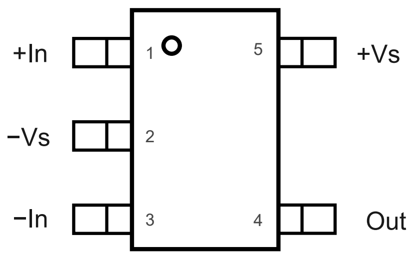


Table 1. Pin Functions: TP1941/TP1941N

Pin No.		Name	I/O	Description
TP1941	TP1941N			
1	1	Out	O	The output of the comparator. The voltage range extends to within millivolts of each supply rail.
2	2	$-V_S$	Power Supply	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V+ and V– is from 1.75 V to 5.5 V. If it is not connected to ground, bypass it with a capacitor of 0.1 µF as close to the part as possible.
3	3	+In	I	Noninverting input of comparator. This pin has the same voltage range as –IN.
4	4	−In	I	Inverting input of the comparator. The voltage range of this pin can go from (V–) – 0.3 V to (V+) + 0.3V.
5	6	$+V_S$	Power Supply	Positive power supply. Typically, the voltage is from 1.75 V to 5.5 V. Split supplies are possible as long as the voltage between V+ and V– is between 1.75 V and 5.5 V. A bypass capacitor of 0.1 µF as close to the part as possible should be used between the power supply pins or between supply pins and ground.
	5	$\overline{SHDN}$		Active lowshutdown. The shutdown threshold is 1/2 V+ above the negative supply rail.

TP1941U
SOT23-5/SC70-5
(−T and −C Suffixes)
Top View



TP1941U2
SOT23-5
(−T Suffix)
Top View

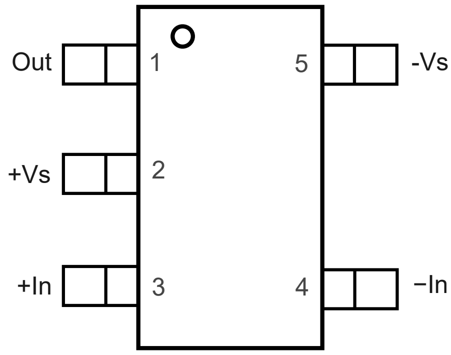
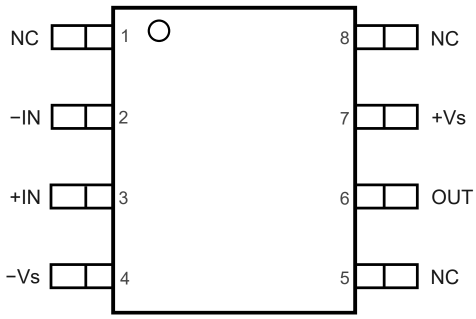


Table 2. Pin Functions: TP1941U/TP1941U2

Pin No.		Name	I/O	Description
TP1941U	TP1941U2			
1	3	+In	I	Noninverting input of comparator. This pin has the same voltage range as –IN.
2	5	$-V_S$	Power Supply	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V+ and V– is from 1.75 V to 5.5 V. If it is not connected to ground, bypass it with a capacitor of 0.1 μF as close to the part as possible.
3	4	−In	I	Inverting input of the comparator. The voltage range of this pin can go from (V–) – 0.3 V to (V+) + 0.3V.
4	1	Out	O	The output of the comparator. The voltage range extends to within millivolts of each supply rail.
5	2	$+V_S$	Power Supply	Positive power supply. Typically, the voltage is from 1.75 V to 5.5 V. Split supplies are possible as long as the voltage between V+ and V– is between 1.75 V and 5.5 V. A bypass capacitor of 0.1 μF as close to the part as possible should be used between the power supply pins or between supply pins and ground.

TP1941
SOP8
(−S Suffix)
Top View



TP1941N
SOP8
(−S Suffix)
Top View

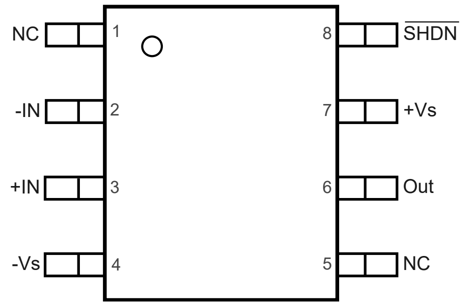


Table 3. Pin Functions: TP1941/TP1941N

Pin No.		Name	I/O	Description
TP1941	TP1941N			
1	1	NC		Not connected.
2	2	−IN	I	Inverting input of the comparator. The voltage range of this pin can go from (V–) – 0.3 V to (V+) + 0.3V.
3	3	+IN	I	Noninverting input of comparator. This pin has the same voltage range as –IN.
4	4	$-V_S$	Power Supply	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V+ and V– is from 1.75 V to 5.5 V. If it is not connected to ground, bypass it with a capacitor of 0.1 µF as close to the part as possible.
5	5	NC		Not connected.
6	6	OUT	O	The output of the comparator. The voltage range extends to within millivolts of each supply rail.
7	7	$+V_S$	Power Supply	Positive power supply. Typically, the voltage is from 1.75 V to 5.5 V. Split supplies are possible as long as the voltage between V+ and V– is between 1.75 V and 5.5 V. A bypass capacitor of 0.1 µF as close to the part as possible should be used between the power supply pins or between supply pins and ground.
8		NC		Not connected.
	8	$\overline{SHDN}$		Active low shutdown. The shutdown threshold is 1/2 V+ above the negative supply rail.

TP1941NU
SOP8/MSOP8
(−S, −V and −D Suffixes)
Top View

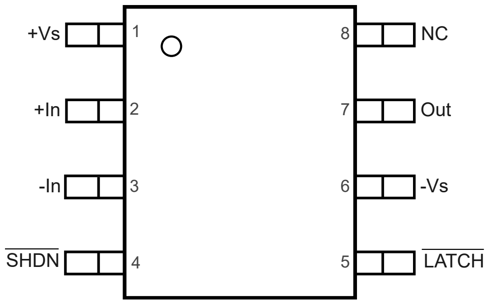
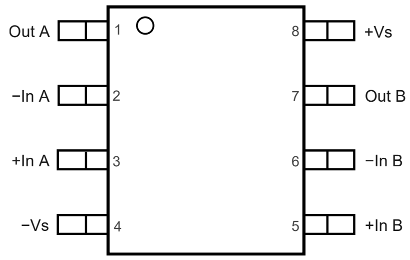


Table 4. Pin Functions: TP1941NU

Pin No. TP1941NU	Name	I/O	Description
1	$+V_S$	Power Supply	Positive power supply. Typically, the voltage is from 1.75 V to 5.5 V. Split supplies are possible as long as the voltage between V+ and V– is between 1.75 V and 5.5 V. A bypass capacitor of 0.1 μF as close to the part as possible should be used between the power supply pins or between supply pins and ground.
2	+In	I	Noninverting input of comparator. This pin has the same voltage range as –IN.
3	−In	I	Inverting input of the comparator. The voltage range of this pin can go from (V–) – 0.3 V to (V+) + 0.3V.
4	$\overline{\text{SHDN}}$		Active low shutdown. The shutdown threshold is 1/2 V+ above the negative supply rail.
5	$\overline{\text{LATCH}}$		Active lowlatch enable. The latch enable threshold is 1/2 V+ above negative supply rail.
6	$-V_S$	Power Supply	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V+ and V– is from 1.75 V to 5.5 V. If it is not connected to ground, bypass it with a capacitor of 0.1 μF as close to the part as possible.
7	Out	O	The output of the comparator. The voltage range extends to within millivolts of each supply rail.
8	NC		Not connected.

TP1942
SOT23-8/SOP8/MSOP8
(−T, −S, −V and −D Suffixes)
Top View



TP1942U
SOP8/MSOP8
(−S and −V Suffixes)
Top View

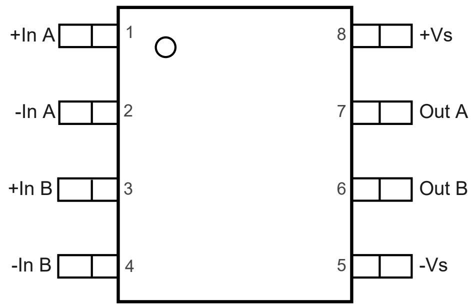


Table 5. Pin Functions: TP1942/TP1942U

Pin No.		Name	I/O	Description
TP1942	TP1942U			
1	7	Out A	O	The output of the comparator. The voltage range extends to within millivolts of each supply rail.
2	2	−In A	I	Inverting input of the comparator. The voltage range of this pin can go from (V–) – 0.3 V to (V+) + 0.3V.
3	1	+In A	I	Noninverting input of comparator. This pin has the same voltage range as –IN.
4	5	$-V_S$	Power Supply	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V+ and V– is from 1.75 V to 5.5 V. If it is not connected to ground, bypass it with a capacitor of 0.1 µF as close to the part as possible.
5	3	+In B	I	Noninverting input of comparator. This pin has the same voltage range as –IN.
6	4	−In B	I	Inverting input of the comparator. The voltage range of this pin can go from (V–) – 0.3 V to (V+) + 0.3V.
7	6	Out B	O	The output of the comparator. The voltage range extends to within millivolts of each supply rail.
8	8	$+V_S$	Power Supply	Positive power supply. Typically, the voltage is from 1.75 V to 5.5 V. Split supplies are possible as long as the voltage between V+ and V– is between 1.75 V and 5.5 V. A bypass capacitor of 0.1 µF as close to the part as possible should be used between the power supply pins or between supply pins and ground.

TP1944
SOP14/TSSOP14
(−S, −T and −D Suffixes)
Top View

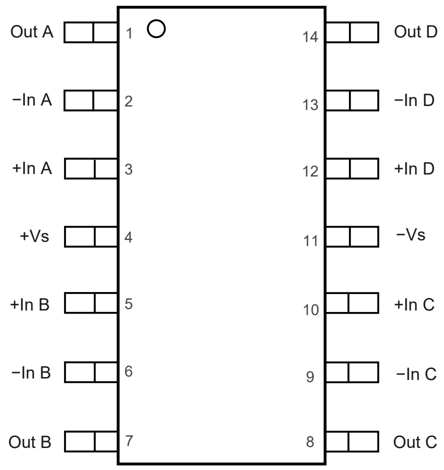


Table 6. Pin Functions: TP1944

Pin No. TP1944	Name	I/O	Description
1	Out A	Power Supply	The output of the comparator. The voltage range extends to within millivolts of each supply rail.
2	−In A	I	Inverting input of the comparator. The voltage range of this pin can go from (V–) – 0.3 V to (V+) + 0.3V.
3	+In A	I	Noninverting input of comparator. This pin has the same voltage range as –IN.
4	$+V_S$	Power Supply	Positive power supply. Typically, the voltage is from 1.75 V to 5.5 V. Split supplies are possible as long as the voltage between V+ and V– is between 1.75 V and 5.5 V. A bypass capacitor of 0.1 µF as close to the part as possible should be used between the power supply pins or between supply pins and ground.
5	+In B	I	Noninverting input of comparator. This pin has the same voltage range as –IN.
6	−In B	I	Inverting input of the comparator. The voltage range of this pin can go from (V–) – 0.3 V to (V+) + 0.3V.
7	Out B	O	The output of the comparator. The voltage range extends to within millivolts of each supply rail.
8	Out C	O	The output of the comparator. The voltage range extends to within millivolts of each supply rail.
9	−In C	I	Inverting input of the comparator. The voltage range of this pin can go from (V–) – 0.3 V to (V+) + 0.3V.
10	+In C	I	Noninverting input of comparator. This pin has the same voltage range as –IN.
11	$-V_S$	Power Supply	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V+ and V– is from 1.75 V to 5.5 V.

Pin No.	Name	I/O	Description
TP1944			
			If it is not connected to ground, bypass it with a capacitor of 0.1 μF as close to the part as possible.
12	+In D	I	Noninverting input of comparator. This pin has the same voltage range as –IN.
13	−In D	I	Inverting input of the comparator. The voltage range of this pin can go from (V–) – 0.3 V to (V+) + 0.3V.
14	Out D	O	The output of the comparator. The voltage range extends to within millivolts of each supply rail.

Specifications

Absolute Maximum Ratings [1]

Parameter		Min	Max	Unit
	Supply Voltage, (V+) − (V−)		6.0	V
	Input Voltage	(V−) − 0.3	(V+) + 0.3	V
	Input Current: +IN, −IN [2]	−10	+10	mA
	Output Current: OUT	−45	+45	mA
	Output Short-Circuit Duration [3]		Indefinite	
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500 mV beyond the power supply, the input current should be limited to less than 10 mA.
(3) A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many comparators are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 [1]	4.5	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 [2]	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Electrical Characteristics

All test conditions: T_A = 27°C, V_{DD} = +1.75 V to +5.5 V, V_{IN+} = V_{DD}, V_{IN-} = 1.2 V, R_{PU} = 10 kΩ, C_L = 15 pF, unless otherwise noted.

The ● denotes the specifications which apply over the full operating temperature range.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	Supply Voltage		●	1.75		5.5	V
V_{OS}	Input Offset Voltage (1)	V_{CM} = 1.2 V		−3	±0.6	+3	mV
$V_{OS}TC$	Input Offset Voltage Drift (1)	V_{CM} = 1.2 V			0.3		uV/°C
V_{HYST}	Input Hysteresis Voltage (1)	V_{CM} = 1.2 V		2	6	8	mV
V_{HYST} TC	Input Hysteresis Voltage Drift (1)	V_{CM} = 1.2 V			20		uV/°C
I_B	Input Bias Current	V_{CM} = 1.2 V			6		pA
I_{OS}	Input Offset Current				4		pA
R_{IN}	Input Resistance				> 100		GΩ
C_{IN}	Input Capacitance	Differential Mode			2		pF
		Common Mode			4		pF
CMRR	Common-Mode Rejection Ratio	V_{CM} = V_{SS} to V_{DD}			70		dB
V_{CM}	Common-Mode Input Voltage Range			(V_{SS}) − 0.1		(V_{DD}) + 0.1	V
PSRR	Power Supply Rejection Ratio				75		dB
V_{OH}	High-Level Output Voltage	I_{OUT} = −1 mA	●	V_{DD} − 0.3			V
V_{OL}	Low-Level Output Voltage	I_{OUT} = 1 mA	●			(V_{SS}) + 0.3	V
I_{SC}	Output Short-Circuit Current	Sink or Source Current			25		mA
I_Q	Quiescent Current per Comparator				46	58	µA
$I_{Q(off)}$	Supply Current in Shutdown (2)					1.5	µA
V_{IL}	SHDN Input Low Voltage (2)	Disable	●			0.2V_{DD}	V
V_{IH}	SHDN Input High Voltage (2)	Enable	●	0.8V_{DD}			V
t_{ON}	Turn-On Time (2)	SHDN Toggle from V_{SS} to V_{DD}			15		µs
t_{OFF}	Turn-Off Time (2)	SHDN Toggle from V_{DD} to V_{SS}			1		µs
t_{LPD}	Latch Propagation Delay (3)				200		ns
t_R	Rising Time				5		ns
t_F	Falling Time				5		ns
T_{PD+}	Propagation Delay (Low-to-High)	Overdrive = 100 mV, V_{IN+} = 1.2 V			89		ns
		V_{IN-} 0 to VCC, V_{IN+} = 1.2 V			300		ns

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{PD-}	Propagation Delay (High-to-Low)	Overdrive = 100 mV, V_{IN+} = 1.2 V			93		ns
		V_{IN-} VCC to 0, V_{IN+} = 1.2 V			28		ns
T_{PDSKEW}	Propagation Delay Skew	Overdrive = 100 mV, V_{IN+} = 1.2 V			−4		ns

(1) The input offset voltage is the average of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.
(2) Specifications apply to the TP1941N with shutdown.
(3) Specifications apply to the TP1941NU with shutdown and latch enable.
(4) The propagation delay skew is defined as: $t_{PD\text{-}SKEW} = t_{PD+} - t_{PD-}$.

Typical Performance Characteristics

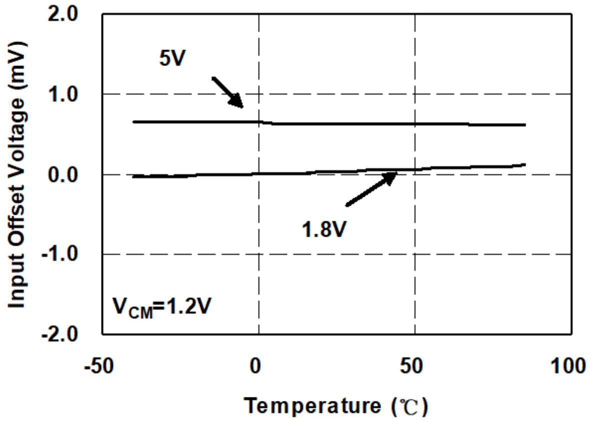


Figure 1. Input Offset Voltage vs. Temperature

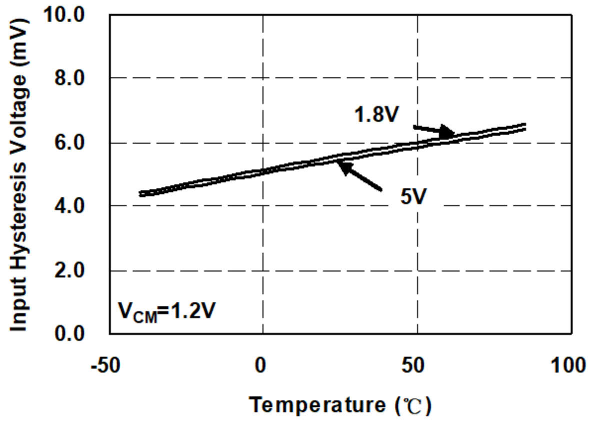


Figure 2. Input Hysteresis Voltage vs. Temperature

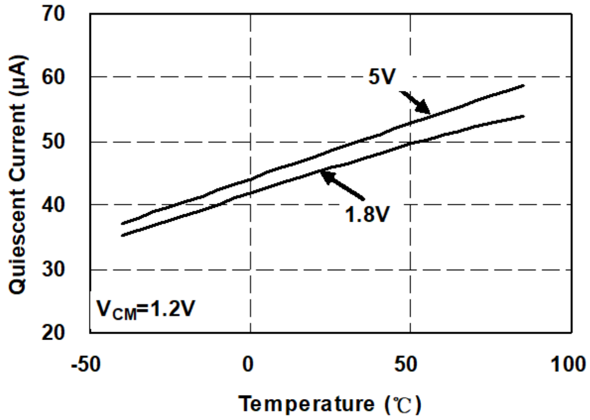


Figure 3. Quiescent Current vs. Temperature

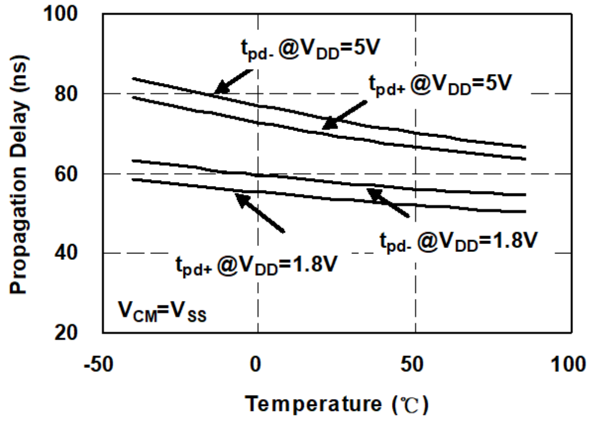


Figure 4. Propagation Delay vs. Temperature

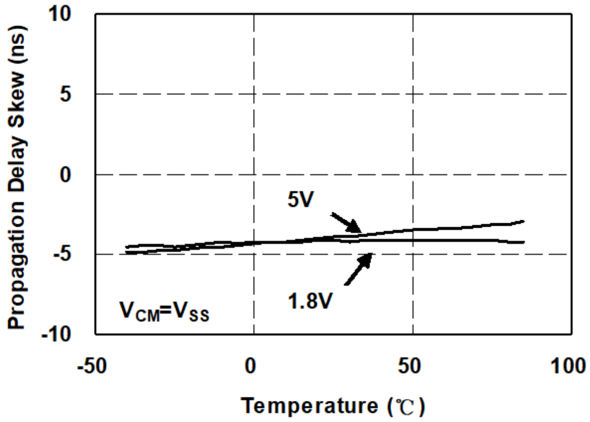


Figure 5. Propagation Delay Skew vs. Temperature

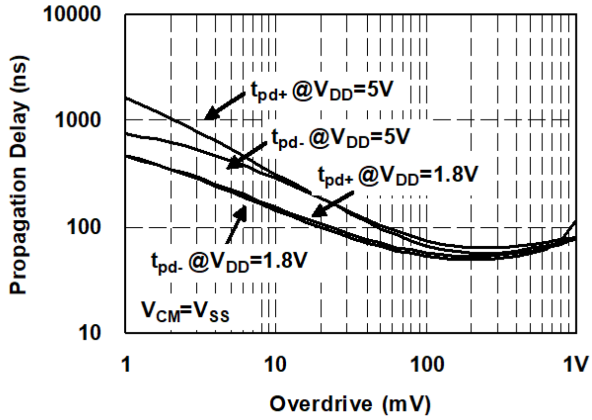


Figure 6. Propagation Delay vs. Overdrive Voltage

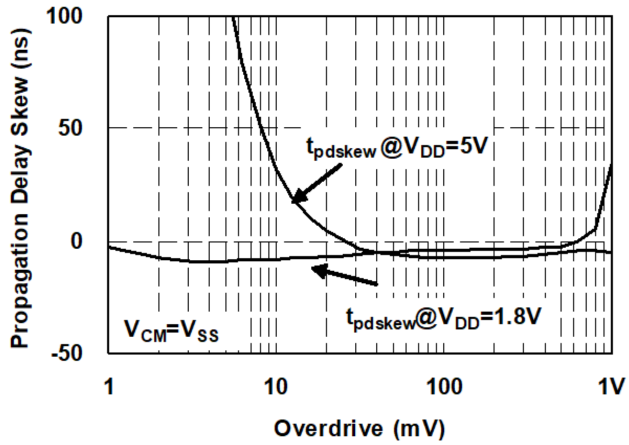


Figure 7. Propagation Delay Skew vs. Overdrive Voltage

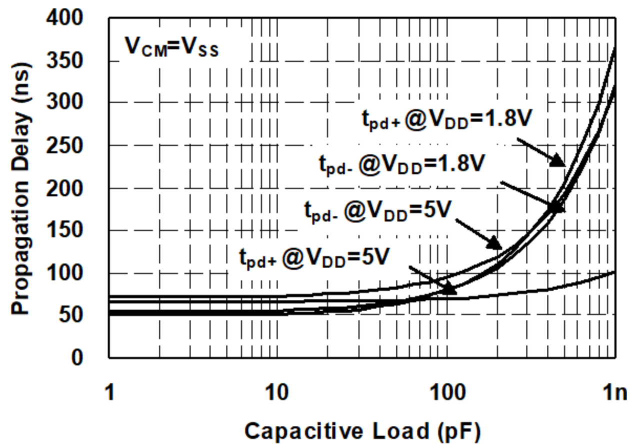


Figure 8. Propagation Delay vs. Capacitor Loading

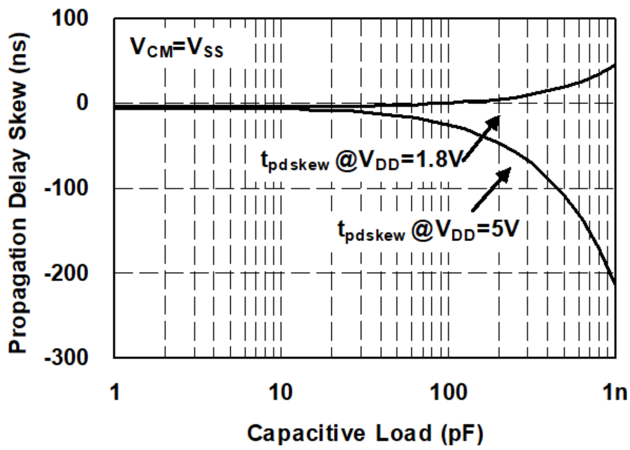


Figure 9. Propagation Delay Skew vs. Capacitor Loading

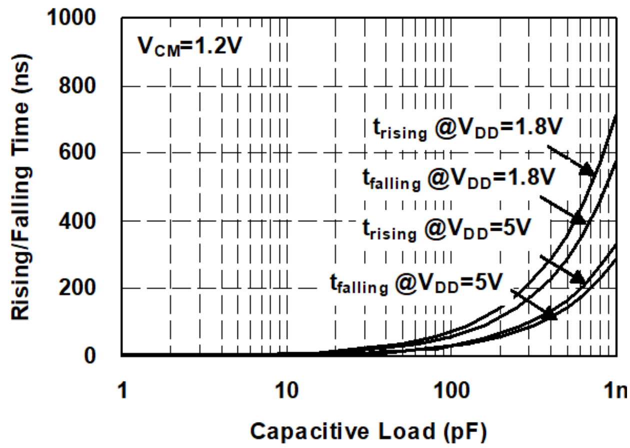


Figure 10. Rising/Falling Time vs. Capacitor Loading

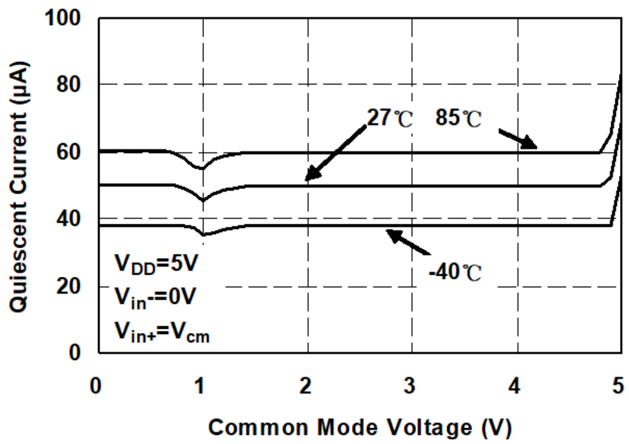


Figure 11. Quiescent Current vs. Common-Mode Voltage

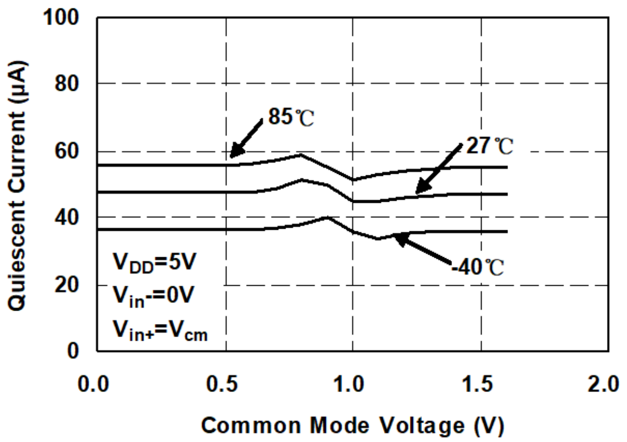


Figure 12. Quiescent Current vs. Common-Mode Voltage

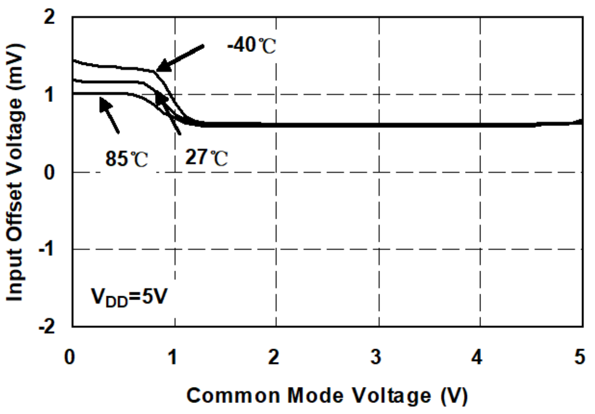


Figure 13. Input Offset Voltage vs. Common-Mode Voltage

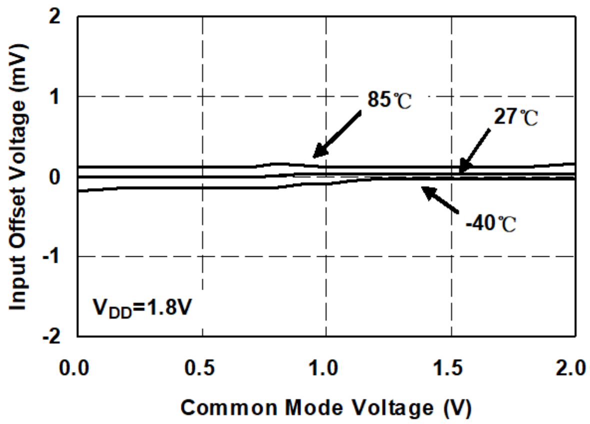


Figure 14. Input Offset Voltage vs. Common-Mode Voltage

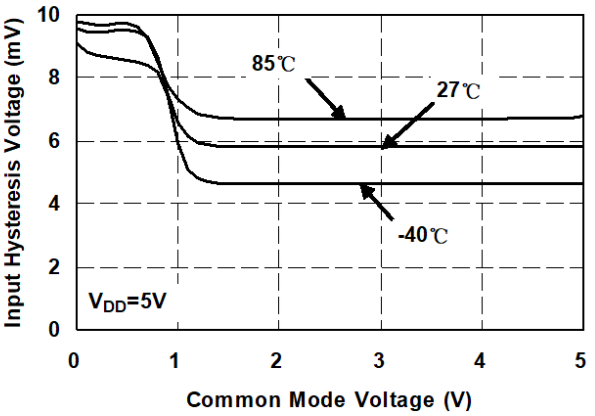


Figure 15. Input Hysteresis Voltage vs. Common-Mode Voltage

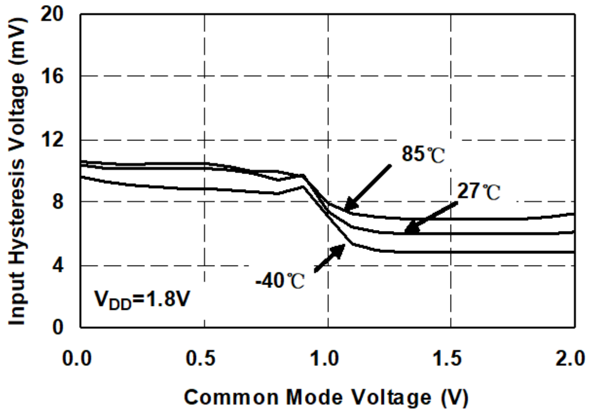


Figure 16. Input Hysteresis Voltage vs. Common-Mode Voltage

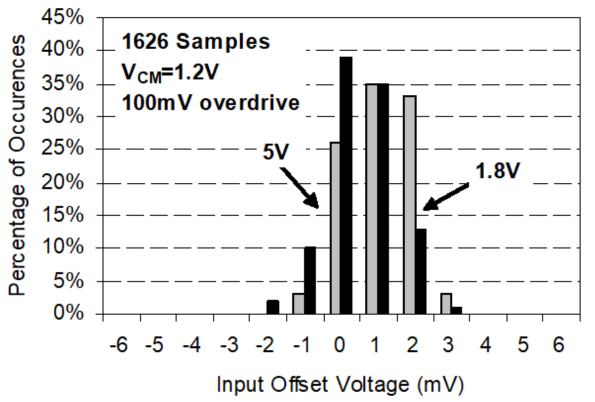


Figure 17. Input Offset Voltage Distribution

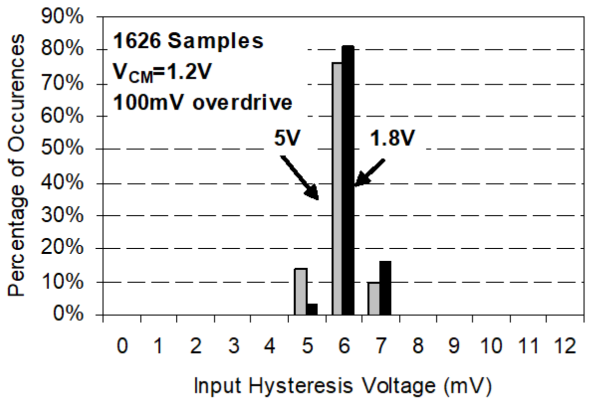


Figure 18. Input Hysteresis Voltage Distribution

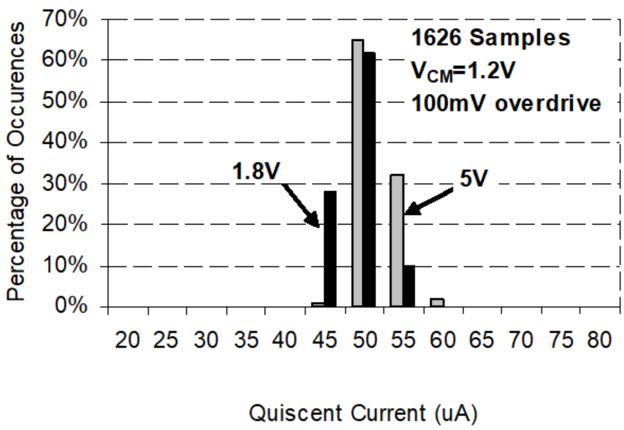


Figure 19. Quiescent Current Distribution

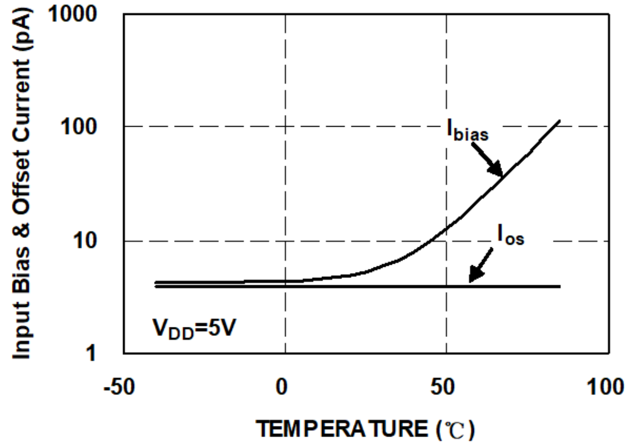


Figure 20. Input Bias and Offset Current vs. Temperature

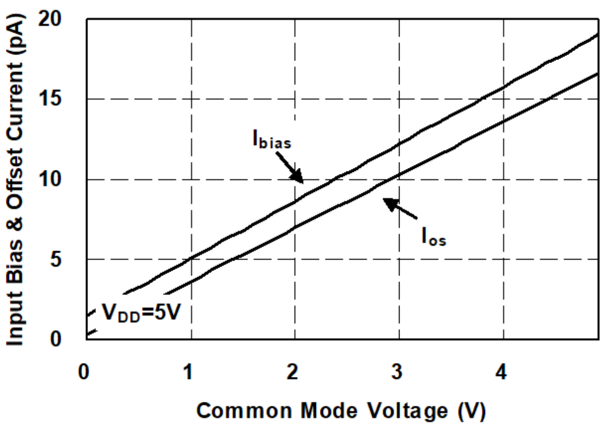


Figure 21. Input Bias Current vs. Common-Mode Voltage

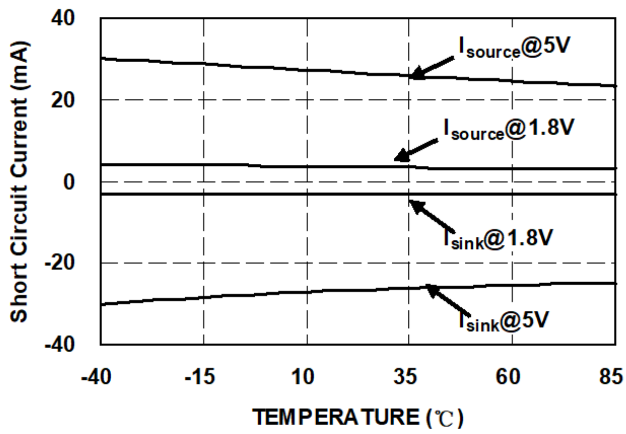


Figure 22. Output Short Circuit Current vs. Temperature

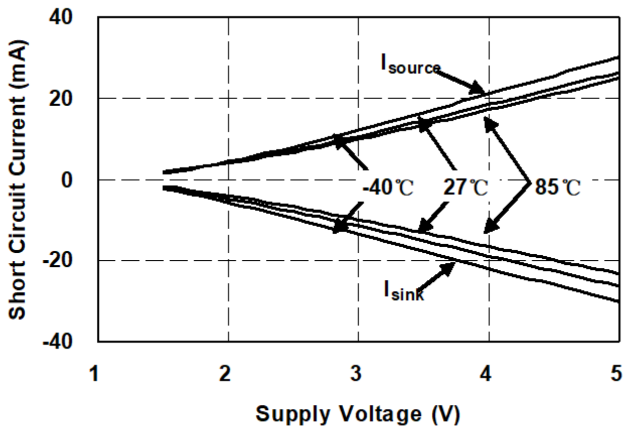


Figure 23. Output Short Circuit vs. Supply Voltage

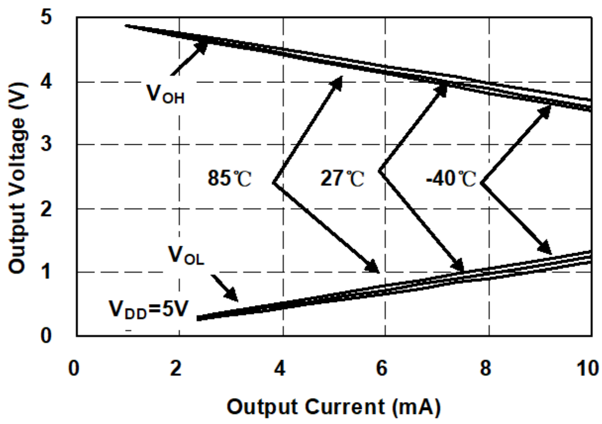


Figure 24. Output Voltage Headroom vs. Output Current

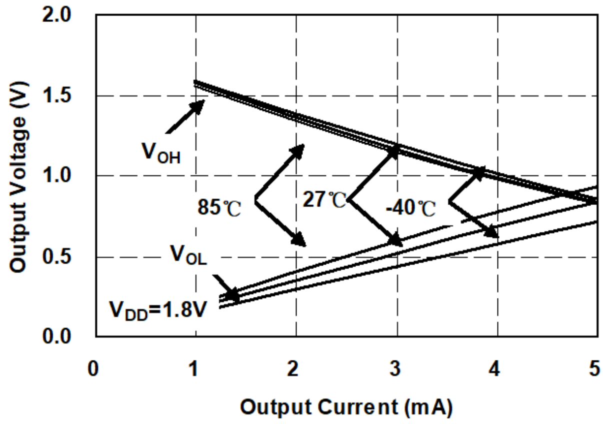


Figure 25. Output Voltage Headroom vs. Output Current

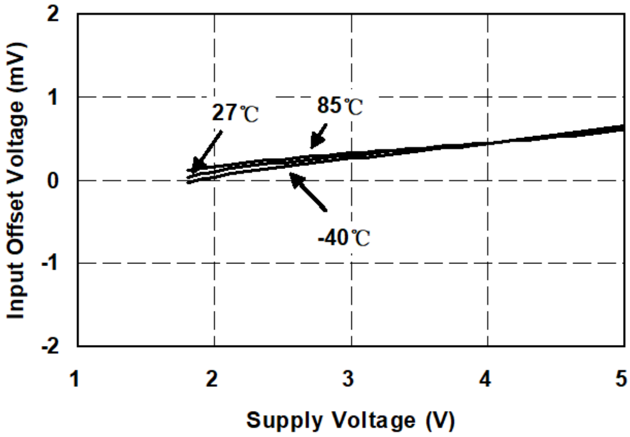


Figure 26. Input Offset Voltage vs. Supply Voltage

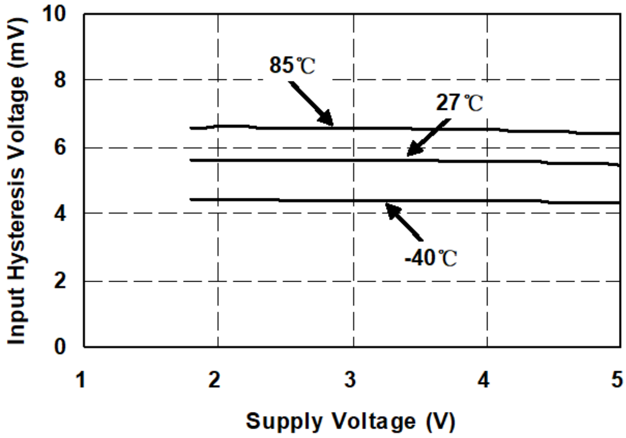


Figure 27. Input Hysteresis Voltage vs. Supply Voltage

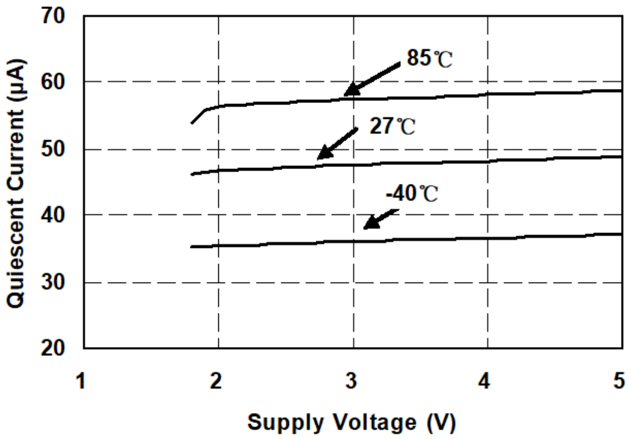


Figure 28. Quiescent Current vs. Supply Voltage

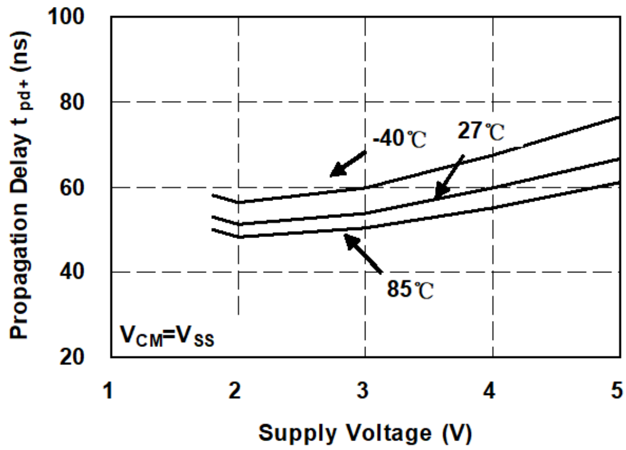


Figure 29. Low-to-High Propagation Delay vs. Supply Voltage

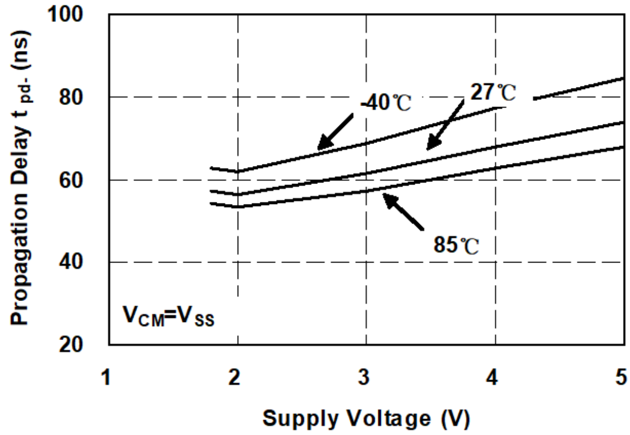


Figure 30. High-to-Low Propagation Delay vs. Supply Voltage

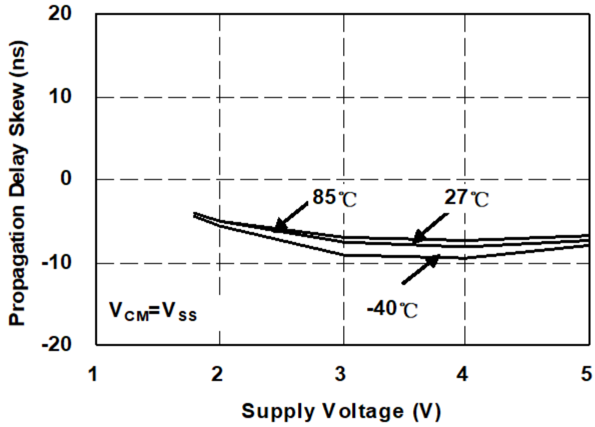


Figure 31. Propagation Skew Delay vs. Supply Voltage

Detailed Description

Overview

The TP194x single-supply comparators feature internal hysteresis, high speed, and low power. The input signal range extends beyond the negative and positive power supplies. The output can even extend all the way to the negative supply. The input stage is active over different ranges of common-mode input voltage. The rail-to-rail input voltage range and low-voltage single-supply operation make these devices ideal for portable equipment.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

Inputs

The TP194x series uses CMOS transistors at the input which prevents the phase inversion when the input pins exceed the supply voltages. Figure 32 shows an input voltage exceeding both supplies with no resulting phase inversion.

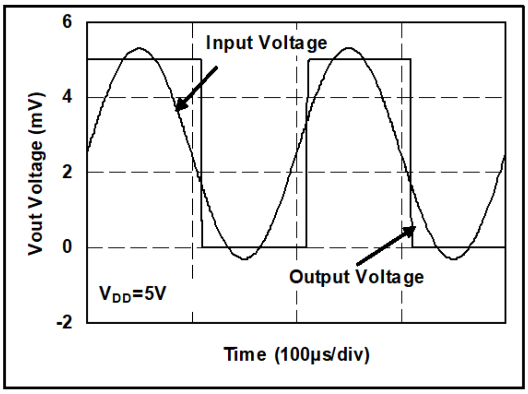


Figure 32. Comparator Response to Input Voltage

The electrostatic discharge (ESD) protection input structure of two back-to-back diodes and 1-kΩ series resistors are used to limit the differential input voltage applied to the precision input of the comparator by clamping input voltages that exceed supply voltages, as shown in Figure 33. Large differential voltages exceeding the supply voltage should be avoided to prevent damage to the input stage.

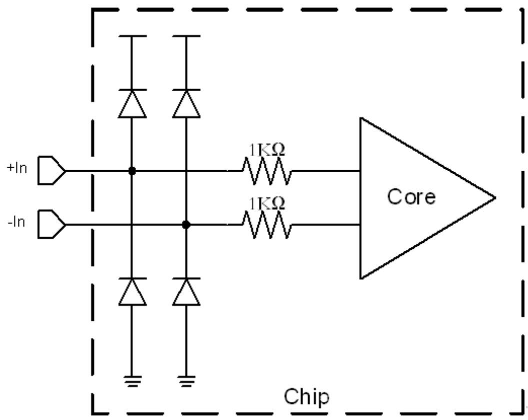


Figure 33. Equivalent Input Structure

Internal Hysteresis

Most high-speed comparators oscillate in the linear region because of the noise or undesired parasitic feedback. This tends to occur when the voltage on one input is equal to the voltage on the other input. To counter the parasitic effects and noise, the TP194x series implements the internal hysteresis.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and the other for the falling input voltage. The difference between the trip points is the hysteresis. When the input voltages of the comparators are equal, the hysteresis effectively causes one input voltage of the comparator to move quickly past the other, and thus taking the input out of the region where the oscillation occurs. Figure 34 illustrates the case where IN− is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the outputs would be inverted.

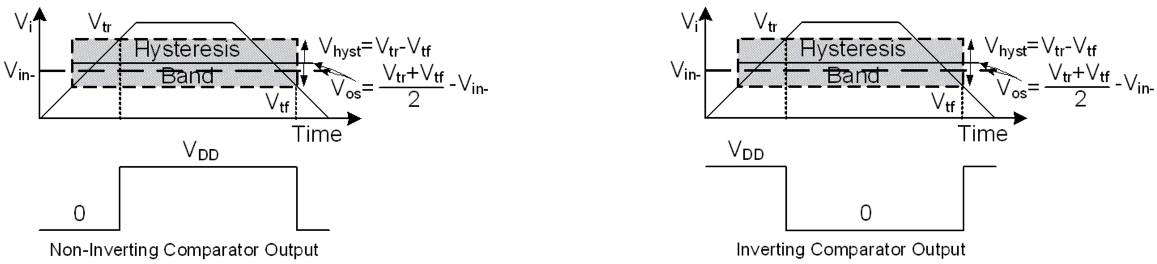


Figure 34. Comparator's Hysteresis and Offset

External Hysteresis

Greater flexibility in selecting hysteresis is achieved by using external resistors. The hysteresis reduces the output chattering when one input is slowly moving past the other. It also helps in systems where it is best not to cycle between high and low states too frequently (e.g., air conditioner thermostatic control). The output chattering also increases the dynamic supply current.

Non-Inverting Comparator with Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network, as shown in Figure 35 and a voltage reference (V_r) at the inverting input.

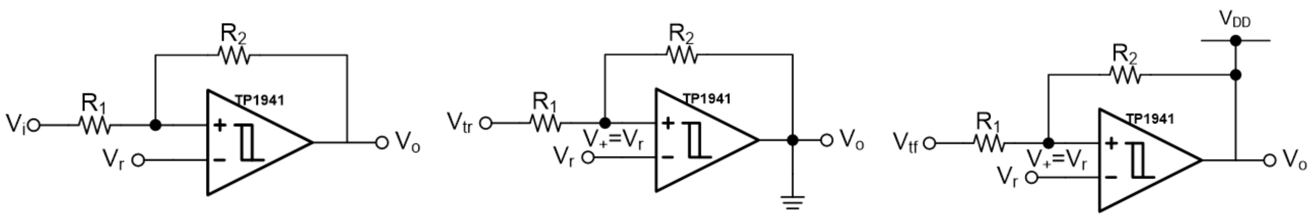


Figure 35. Noninverting Configuration with Hysteresis

When V_i is low, the output is also low. For the output to switch from low to high, V_i must rise up to V_{tr}. When V_i is high, the output is also high. In order for the comparator to switch back to a low state, V_i must equal V_{tf} before the non-inverting input V_+ is again equal to V_r.

$$V_r = \frac{R_2}{R_1 + R_2} V_{tr} \tag{1}$$

$$V_r = (V_{DD} - V_{tf}) \frac{R_1}{R_1 + R_2} + V_{tf} \tag{2}$$

$$V_{tr} = \frac{R_1 + R_2}{R_2} V_r \tag{3}$$

$$V_{tf} = \frac{R_1 + R_2}{R_2} V_r - \frac{R_1}{R_2} V_{DD} \quad (4)$$

$$V_{hyst} = V_{tr} - V_{tf} = \frac{R_1}{R_2} V_{DD} \quad (5)$$

Inverting Comparator with Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the supply voltage (V_{DD}) of the comparator, as shown in Figure 36.

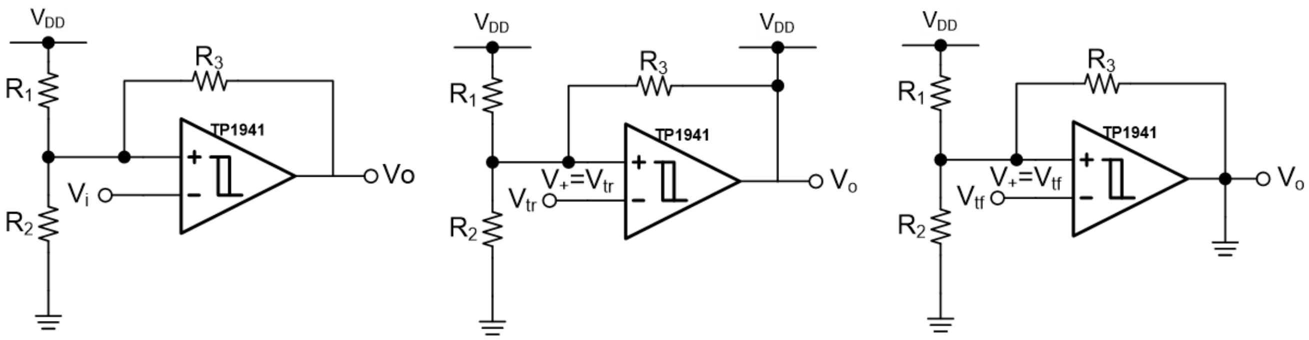


Figure 36. Inverting Configuration with Hysteresis

When V_i is greater than V_+, the output voltage is low. In this case, the three network resistors can be presented as paralleled resistor $R_2 \parallel R_3$ in series with R_1. When V_i at the inverting input is less than V_+, the output voltage is high. The three network resistors can be represented as $R_1 \parallel R_3$ in series with R_2.

$$V_{tr} = \frac{R_2}{R_1 \,||\, R_3 + R_2} V_{DD} \quad (6)$$

$$V_{tf} = \frac{R_2 \,||\, R_3}{R_2 \,||\, R_3 + R_1} V_{DD} \quad (7)$$

$$V_{hyst} = V_{tr} - V_{tf} = \frac{R_1 \,||\, R_2}{R_1 \,||\, R_2 + R_3} V_{DD} \quad (8)$$

Low Input Bias Current

The TP194x series is a CMOS comparator series and features very low input bias current in the pA range. The low input bias current allows the comparators to be used in applications with high resistance sources. Care must be taken to minimize the PCB surface leakage. See PCB Surface Leakage section below for more details.

PCB Surface Leakage

In applications where the low input bias current is critical, the Printed Circuit Board (PCB) surface leakage effects need to be considered. The surface leakage is caused by humidity, dust, or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is 10^{12} Ω. A 5-V difference would cause a 5-pA current to flow, which is greater than the input bias current of the TP194x series at +27°C (±6 pA, typical). It is recommended to use the multi-layer PCB layout and route the −IN and +IN signal of the device under the PCB surface.

An effective way to reduce surface leakage is to use a guard ring around the sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 37 for inverting gain applications.

1. For noninverting configuration:
   a. Connect the noninverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b. Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the common-mode input voltage.

2. For inverting configuration:
   a. Connect the guard ring to the noninverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the comparator (e.g., V_{DD} / 2 or ground).
   b. Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

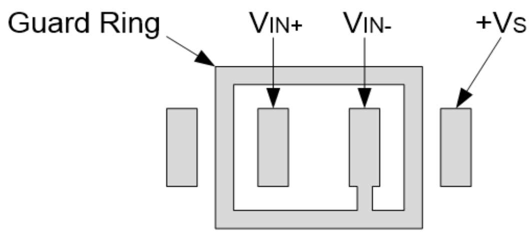


Figure 37. Example Guard Ring Layout of Inverting Comparator

Ground Sensing and Rail-to-Rail Output

The TP194x series implements a rail-to-rail topology that is capable of swinging to within 10 mV of either rail. Since the inputs can go 300 mV beyond either rail, the comparator can easily perform 'True Ground Sensing'.

The maximum output current is a function of the total supply voltage. As the supply voltage of the comparator increases, the output current capability also increases. Attention must be paid to keeping the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.5 V beyond either supply, otherwise the current flows through these diodes.

ESD

The TP194x series has reverse-biased ESD protection diodes on all inputs and outputs. The input and output pins cannot be biased more than 300 mV beyond either supply rail.

Power Supply Layout and Bypass

The power supply pin of theTP194x series should have a local bypass capacitor (i.e., 0.01 μF to 0.1 μF) within 2 mm for good high-frequency performance. It can also use a bulk capacitor (i.e., 1 μF or larger) within 100 mm to provide large and slow currents. This bulk capacitor can be shared with other analog parts.

The good ground layout improves performance by decreasing the amount of the stray capacitance and noise at the inputs and outputs of the comparator. To decrease the stray capacitance, minimize the PCB lengths and resistor leads, and place external components as close to the pins as possible.

Typical Applications

IR Receiver

The TP1941 is an ideal candidate to be used as an infrared receiver shown in Figure 38. The infrared photo diode creates a current relative to the amount of infrared light present. The current creates a voltage across R_D. When this voltage level crosses the voltage applied by the voltage divider to the inverting input, the output transitions. Optional R_o provides additional hysteresis for the noise immunity.

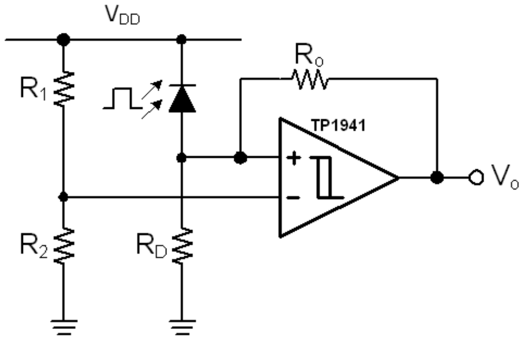


Figure 38. IR Receiver

Relaxation Oscillator

A relaxation oscillator using TP1941 is shown in Figure 39. Resistors R_1 and R_2 set the bias point at the inverting input of the comparator. The period of the oscillator is set by the time constant of R_4 and C_1. The maximum frequency is limited by the large signal propagation delay of the comparator. The low propagation delay of the TP1941 guarantees the high frequency oscillation.

If the inverted input (V_{C1}) is lower than the noninverting input (V_A), the output is high which charges C_1 through R_4 until V_{C1} is equal to V_A. The value of V_A at this point is

$$V_{A1} = \frac{V_{DD} \cdot R_2}{R_1 \,||\, R_3 + R_2} \quad (9)$$

At this point the comparator switches and pulls down the output to the negative rail. The value of V_A at this point is

$$V_{A2} = \frac{V_{DD} \cdot R_2 \,||\, R_3}{R_1 + R_2 \,||\, R_3} \quad (10)$$

If $R_1 = R_2 = R_3$, then $V_{A1} = 2\ V_{DD} / 3$, and $V_{A2} = V_{DD} / 3$.

The capacitor C_1 now discharges through R_4, and the voltage V_C decreases till it is equal to V_{A2}, at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge C_1 from $2\ V_{DD} / 3$ to $V_{DD} / 3$. Hence the frequency is:

$$Freq = \frac{1}{2 \cdot \ln 2 \cdot R_4 \cdot C_1} \quad (11)$$

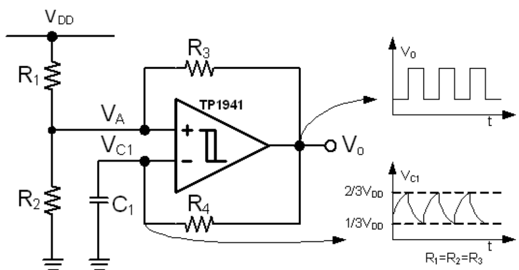


Figure 39. Relaxation Oscillator

Windowed Comparator

Figure 40 shows one approach to designing a windowed comparator using a single TP1942 chip. Choose different thresholds by changing the values of R_1, R_2, and R_3. OutA provides an active-low undervoltage indication, and OutB gives an active-low overvoltage indication. ANDing the two outputs provides an active-high, power-good signal. When the input voltage V_i reaches the overvoltage threshold V_{OH}, OutB gets low. Once V_i falls to the undervoltage threshold V_{UH}, OutA gets low. When $V_{UH} < V_i < V_{OH}$, the AND Gate gets high.

$V_{OH} = V_r \cdot (R_1 + R_2 + R_3) / R_1$ (12)

$V_{UH} = V_r \cdot (R_1 + R_2 + R_3) / + (R_1 + R_2)$ (13)

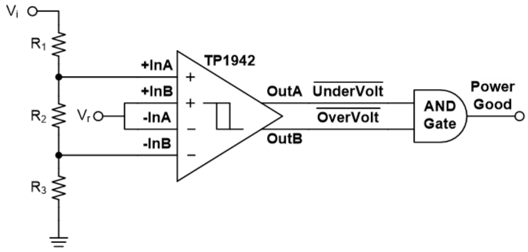
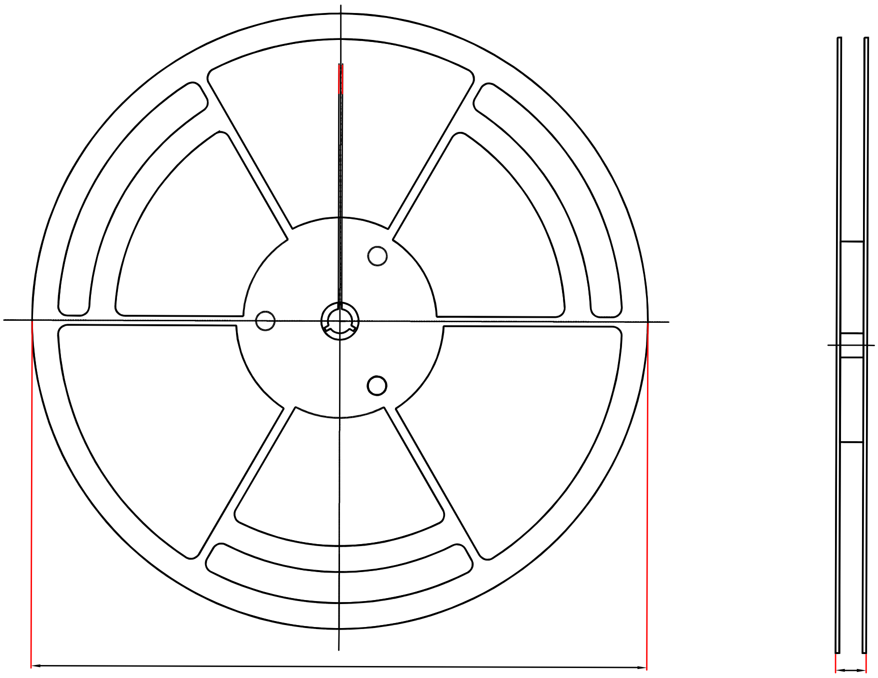
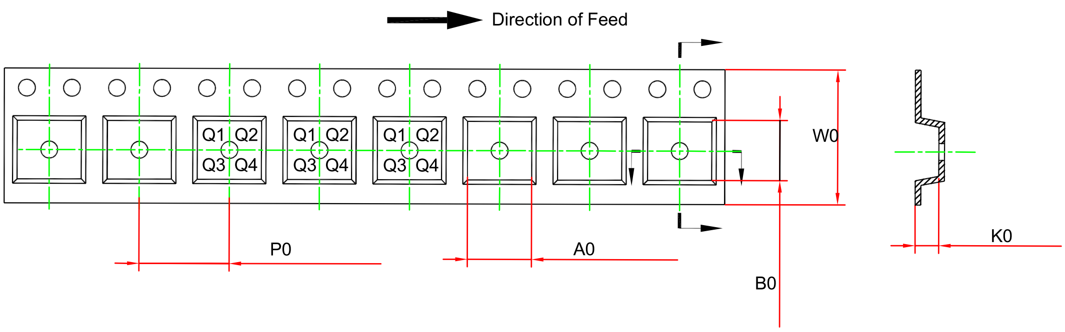


Figure 40. Windowed Comparator

Tape and Reel Information



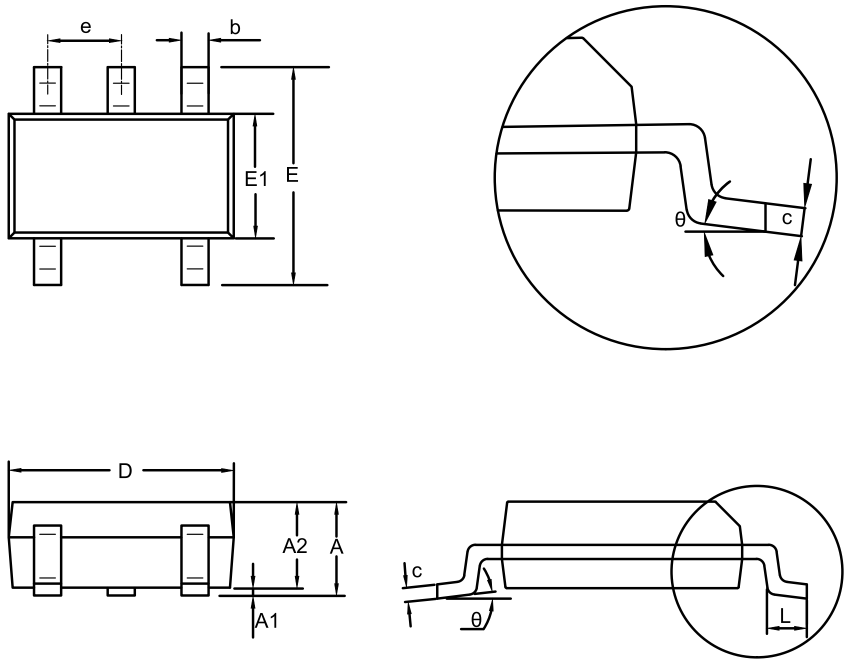


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TP1941-TR	SOT23-5	180.0	12.0	3.2	3.2	1.4	4.0	8.0	Q3
TP1941-CR	SOT353 (SC70-5)	178.0	12.3	2.4	2.5	1.2	4.0	8.0	Q3
TP1941U-CR	SOT353 (SC70-5)	178.0	12.3	2.4	2.5	1.2	4.0	8.0	Q3
TP1942-SR	SOP8	330.0	17.6	6.5	5.4	2	8.0	12.0	Q1
TP1942-VR	MSOP8	330.0	12.9	5.3	3.3	1.3	8.0	12.0	Q1

Package Outline Dimensions

SOT353 (SC70-5)

Package Outline Dimensions SC5(SOT353-5-A)



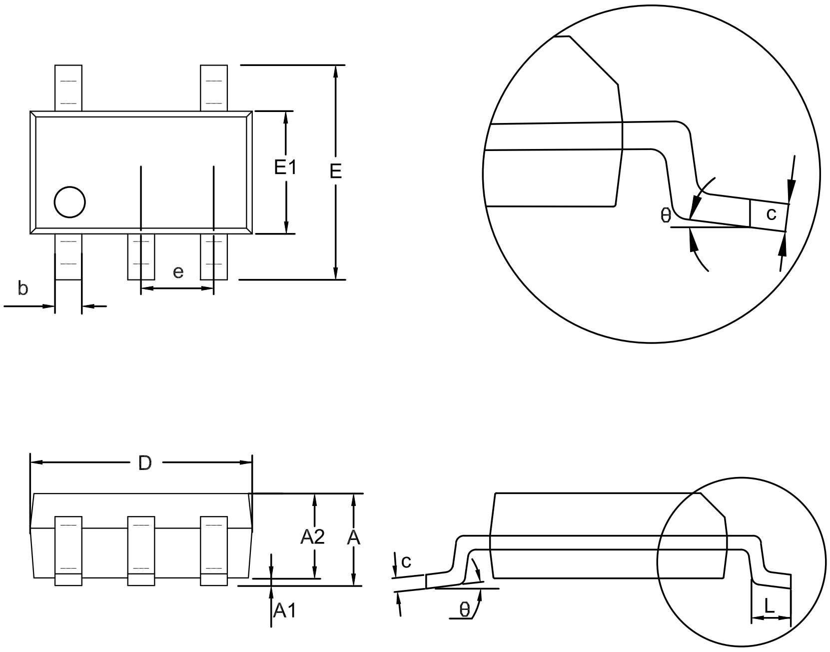
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.850	1.100	0.033	0.043
A1	0.000	0.100	0.000	0.004
A2	0.800	1.000	0.031	0.039
b	0.150	0.350	0.006	0.014
c	0.110	0.230	0.004	0.009
D	2.000	2.200	0.079	0.087
E	2.150	2.450	0.085	0.096
E1	1.150	1.350	0.045	0.053
e	0.650 BSC		0.026 BSC	
L	0.260	0.460	0.010	0.018
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

SOT23-5

Package Outline Dimensions S5T(SOT23-5-A)



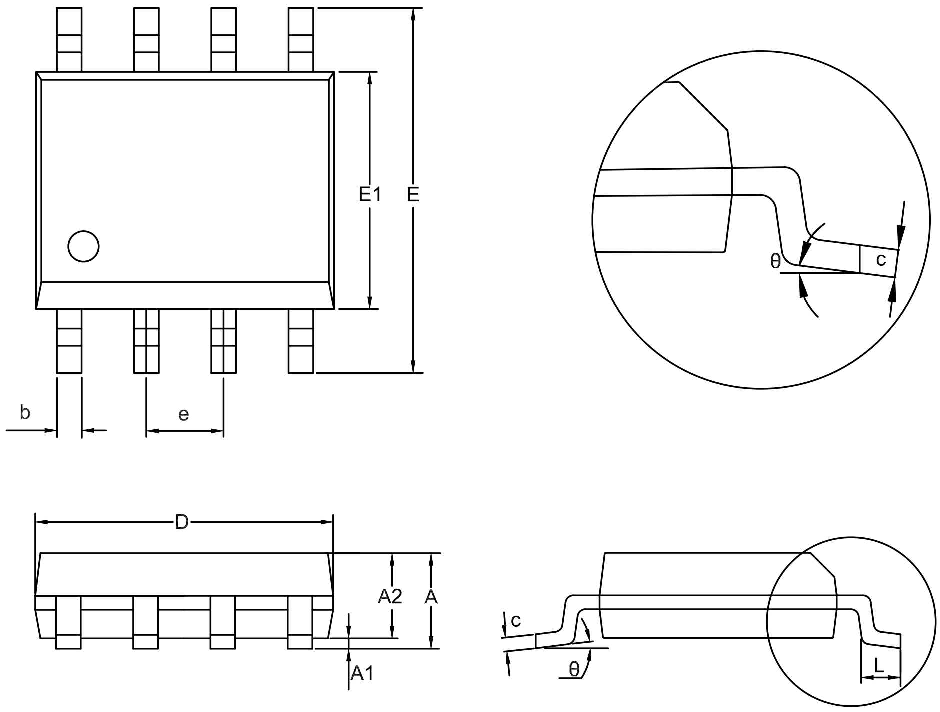
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.280	0.500	0.011	0.020
c	0.100	0.230	0.004	0.009
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.720	0.059	0.068
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

SOP8

Package Outline Dimensions SO1(SOP-8-A)



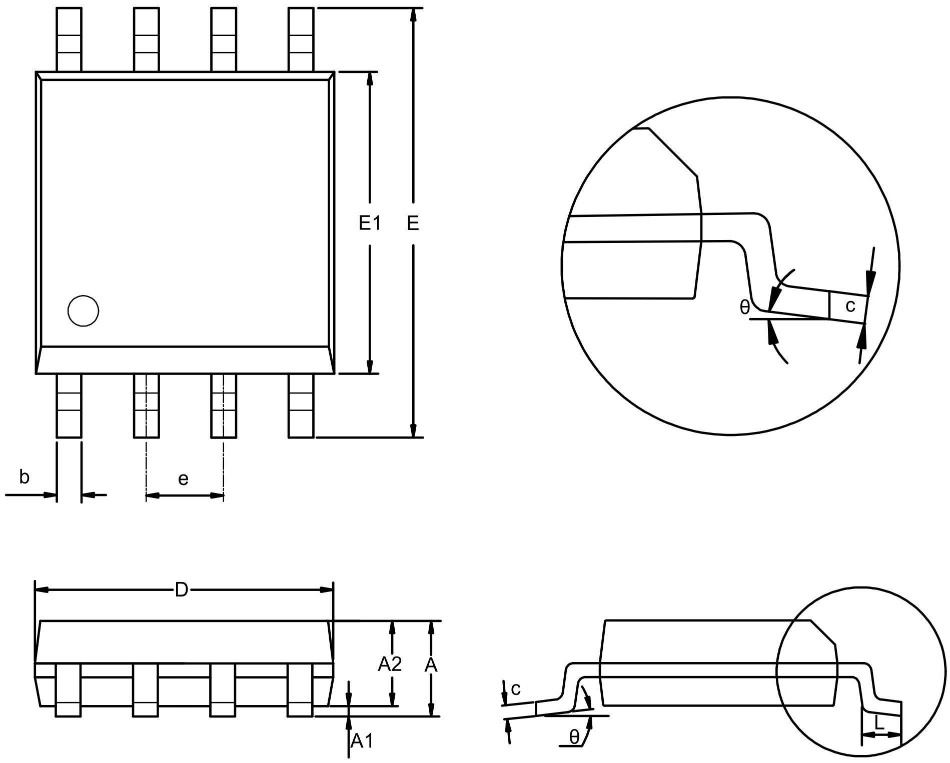
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

MSOP8

Package Outline Dimensions VS1(MSOP-8-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TP1941-TR	−40 to 125°C	SOT23-5	C4T	3	Tape and Reel, 3000	Green
TP1941-CR	−40 to 125°C	SC70-5	C4C	3	Tape and Reel, 3000	Green
TP1941U-CR	−40 to 125°C	SC70-5	C4U	3	Tape and Reel, 3000	Green
TP1942-SR	−40 to 125°C	SOP8	1942S	3	Tape and Reel, 4000	Green
TP1942-VR	−40 to 125°C	MSOP8	1942V	3	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

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