Zero-Drift, Bi-directional Current Sense Amplifier

Features

- TP182A1/A2 VOLTAGE OFFSET: **±50uV (MAX)**
- TP182A3/A4 VOLTAGE OFFSET: **±35uV (MAX)**
- WIDE COMMON MODE VOLTAGE: **-0.3V to +36V**
- SUPPLY VOLTAGE: **2.7V to +30V**
- ACCURACY and ZERO-DRIFT PERFORMANCE
  - **±1% Gain Error (Max over temperature)**
  - **0.5μV/°C Offset Drift (Max)**
  - **10ppm/°C Gain Drift (Max)**
- THREE GAIN OPTIONS for VOLTAGE OUTPUT
  - TP182A1: 50V/V
  - TP182A2: 100V/V
  - TP182A3: 200V/V
  - TP182A4: 500V/V
- LOW SUPPLY CURRENT: 120uA (TYP)
- **Rail-to-Rail Output**
- PACKAGE: SC70-6
- Industrial –40°C to 125°C Operation Range
- ESD Rating: Robust 2KV – HBM, 2KV – CDM
- Higher performance Drop-In Compatible With INA213, INA214, INA199, NCS199 Products

Applications

- CURRENT SENSING (High−Side/Low−Side)
- BATTERY CHARGERS
- POWER MANAGEMENT
- CELL PHONE CHARGER
- ELECTRICAL CIGIRATE
- WIRELESS CHARGER
- TELECOM EQUIPMENT

Description

The TP182 series of zero-drift, bi-directional current sense amplifier can sense voltage drops across shunts at common-mode voltages from –0.3V to 36V, independent of the supply voltage. Three fixed gains are available: 50V/V, 100V/V and 200V/V. The low offset of the zero-drift architecture enables current sensing with maximum drops across the shunt as low as **10mV** full-scale.

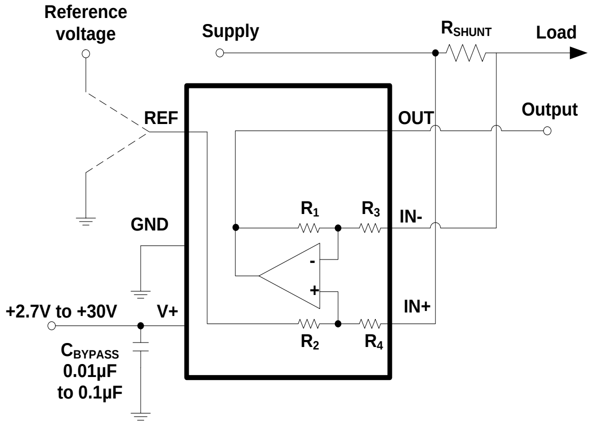
TP182 devices operate from a single +2.7V to 30V power supply, with drawing a typical of 120uA of supply current. All versions are specified from –40°C +125°C, and offered in SC70-6 packages.

GAIN OPTIONS TABLE

PRODUCT	GAIN	R3 and R4	R1 and R2
TP182A1	50	20kΩ	1MΩ
TP182A2	100	10kΩ	1MΩ
TP182A3	200	5kΩ	1MΩ
TP182A4	500	2kΩ	1MΩ

$$V_{OUT} = (I_{LOAD} \times R_{SHUNT})GAIN + V_{REF}$$

Application schematic



Pin Configuration

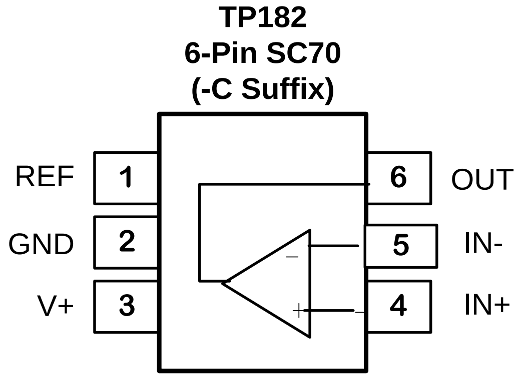


Table of Contents

Revision History

Date	Revision	Notes
2018-11-1	Rev.A.0	Release Version, TP182A1, G=50
2019-4-10	Rev.A.1	Add TP182A2, G=100
2019-7-17	Rev.A.2	Add TP182A3, G=200
2020-09-16	Rev.A.3	Add TP182A4, G=500; update Maximum Working Junction Temperature 150°C
2021-01-21	Rev.A.4	Product HBM ESD is 2kV, Modify “ESD Rating: Robust 2KV – HBM” in Features description
2023-08-24	Rev.A.5	The following updates are all about the new datasheet formats or typo, the actual product remains unchanged. Updated to new format of package dimensions. Added tape and reel information.

Order Information

Model Name	Order Number	Gain	Package	Transport Media, Quantity	Package Marking
TP182	TP182A1-CR	50V/V	6-Pin SC70	Tape and Reel, 3,000	9A1
	TP182A2-CR	100V/V	6-Pin SC70	Tape and Reel, 3,000	9A2
	TP182A3-CR	200V/V	6-Pin SC70	Tape and Reel, 3,000	9A3
	TP182A4-CR	500V/V	6-Pin SC70	Tape and Reel, 3,000	9A4

Absolute Maximum Ratings Note 1

Supply Voltage Note 2………………….................42.0V
Input Voltage....................................GND– 0.3 to 42V
Input Current: +IN, –IN Note 3..............................±5mA
Output Current: OUT.................................... ±35mA

Current at Supply Pins…………….............. ±60mA
Operating Temperature Range........–40°C to 125°C
Maximum Working Junction Temperature......150°C
Storage Temperature Range.......... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
Note 2: The op amp supplies must be established simultaneously, with, or before, the application of any input signals.
Note 3: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	±2	kV

Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
6-Pin SC70	227	80	°C/W

Electrical Characteristics

The specifications are at TA = 25°C, VSENSE = VIN+ – VIN–, VS = 5 V, VIN+ = 12V, and VREF = VS / 2, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INPUT						
V_{OS}	Input Offset Voltage	VSENSE=0mV, VIN+=5V, TP182A1& TP182A2		±10	**±50**	uV
		VSENSE=0mV, VIN+=5V, TP182A3 & TP182A4		±10	**±35**	uV
V_{OS} TC	Input Offset Voltage Drift	VSENSE = 0 mV, -40°C to 125°C		0.1	0.5	μV/°C
V_{CM}	Common-mode Input Range	-40°C to 125°C	-0.3		**36**	V
CMRR	Common Mode Rejection Ratio	VIN+ = 5~26 V, VSENSE = 0 mV, -40°C to 125°C	95	120		dB
I_B	Input Bias Current	VSENSE = 0 mV		35		uA
I_{OS}	Input Offset Current	VSENSE = 0 mV		0.4		uA
PSRR	Power Supply Rejection Ratio	Vs = +2.7~18V, VIN+ = +18V, VSENSE = 0 mV		±1		uV/V
NOISE RTI Note 4						
e_n	Input Voltage Noise Density	f = 1kHz		30		nV/√Hz
OUTPUT						
G	Gain	TP182A1		50		V/V
		TP182A2		100		V/V
		TP182A3		200		V/V
		TP182A4		500		V/V
GE	Gain Error	VSENSE = -5~5mV, -40°C to 125°C		±0.1%	±1%	
GE TC	Gain Error Vs Temperature	-40°C to 125°C		3	10	ppm
C_{LOAD}	Maxim capacitive load	No oscillation		1		nF
V_{OH}	Output Swing from Supply Rail	R_{LOAD} = 10kΩ to GND, -40°C to 125°C		0.02	0.05	V
V_{OL}	Output Swing from GND	R_{LOAD} = 10kΩ to GND, -40°C to 125°C		0.01	0.05	V
FREQUENCY RESPONSE						
BW	Bandwidth	CLOAD = 10pF, TP182A1		48		kHz
		CLOAD = 10pF, TP182A2		30		kHz
		CLOAD = 10pF, TP182A3		20		kHz
		CLOAD = 10pF, TP182A4		9		kHz
SR	Slew Rate			0.6		V/μs
POWER SUPPLY						
V+	Supply Voltage		2.7		30	V
I_Q	Quiescent Current	VSENSE = 0 mV		120	150	μA
TEMPERATURE RANGE						
	Specified range		-40		125	°C
	Operating range		-55		150	°C

Note 4: RTI = referred to input

Typical Performance Characteristics

The TP182A1 is used for characteristics at TA = 25°C, VS = 5V, VIN+ =12V, and VREF=VS/2, unless otherwise noted

Input Bias Current vs Common-Mode Voltage

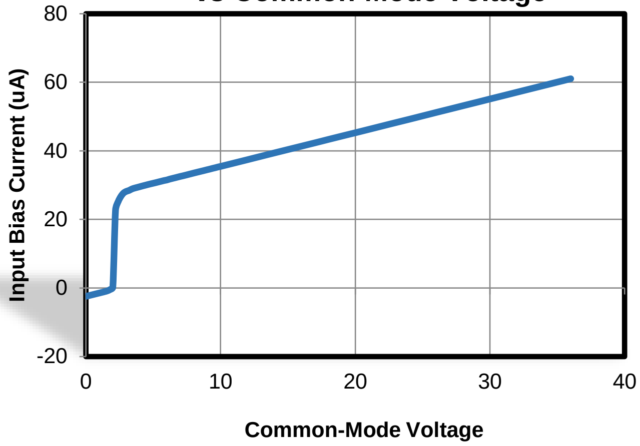


Figure 1

CMRR vs. Temperature

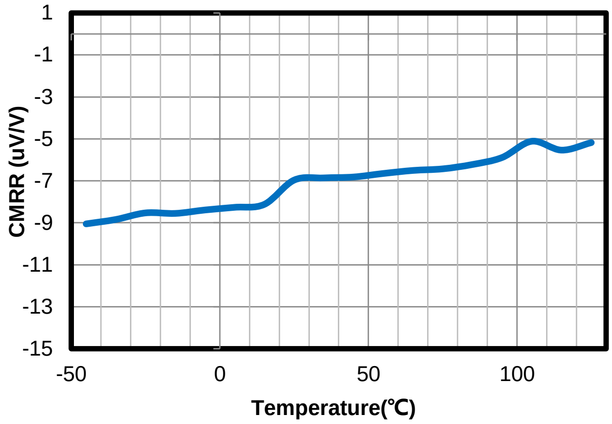


Figure 2

Gain vs. Frequency

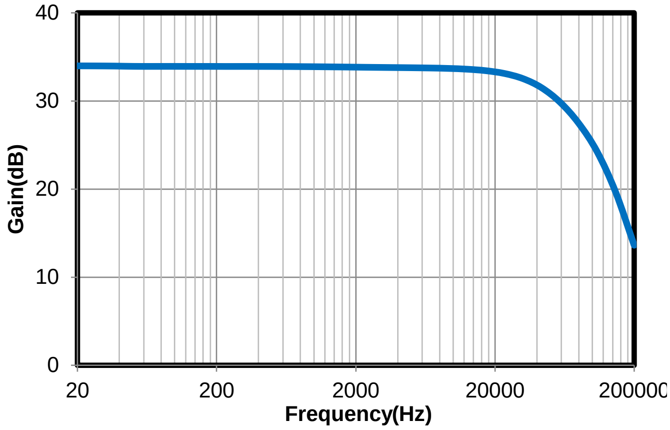


Figure 3

CMRR Vs Frequency

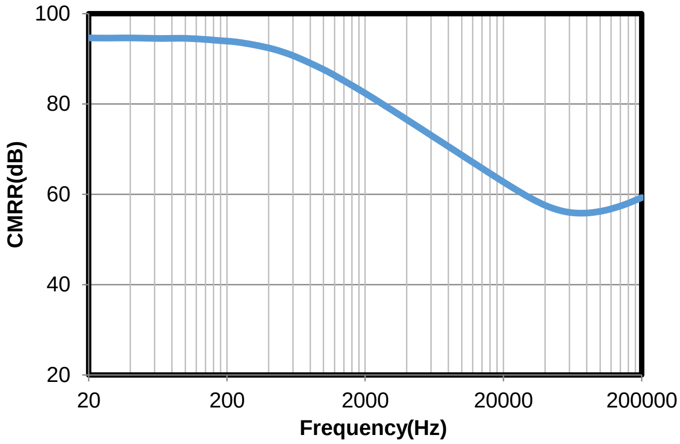


Figure 4

PSRR vs. Frequency

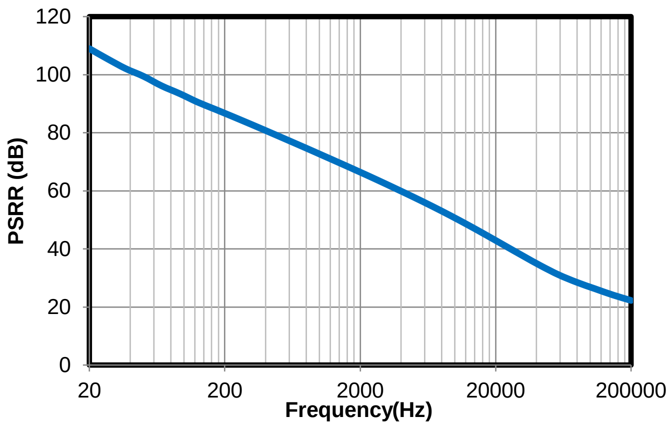


Figure 5

0.1-Hz to 10Hz Voltage Noise (Referred-to-Input)

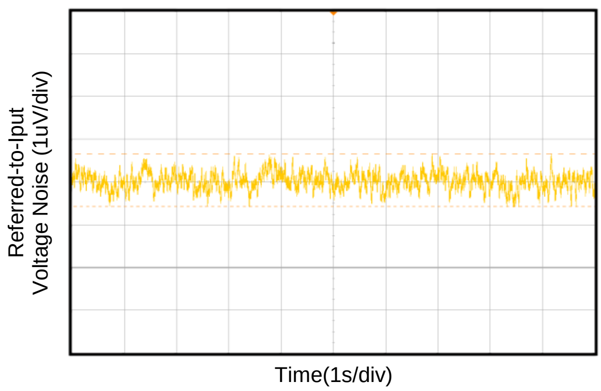


Figure 6

Typical Performance Characteristics

The TP182A1 is used for characteristics at TA = 25°C, VS = 5V, VIN+ =12V, and VREF=VS/2, unless otherwise noted

Step response (10-mVpp Input Step)

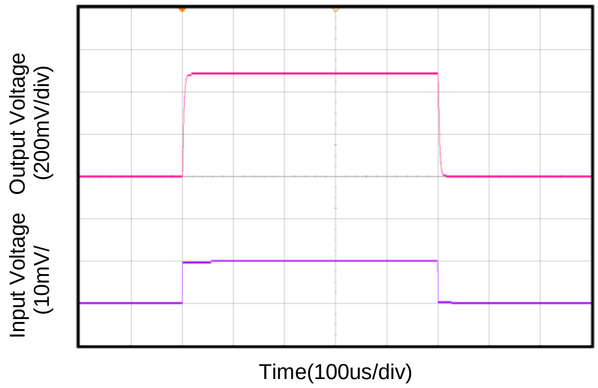


Figure 7

Common-Mode Voltage Transient Response

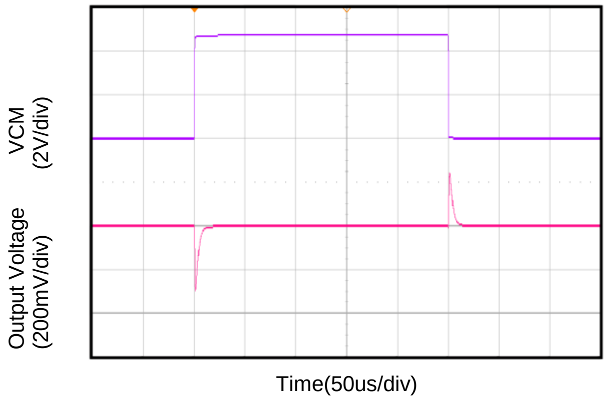


Figure 8

Noninverting Differential Input Overload

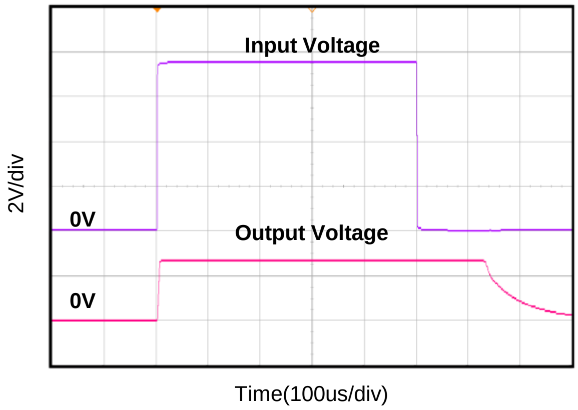


Figure 9

Inverting Differential Input Overload

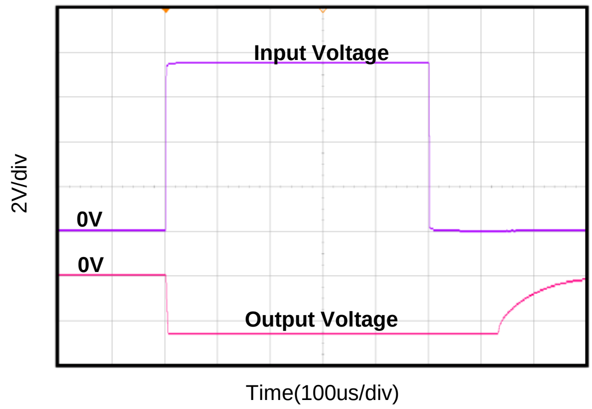


Figure 10

Start-up Response

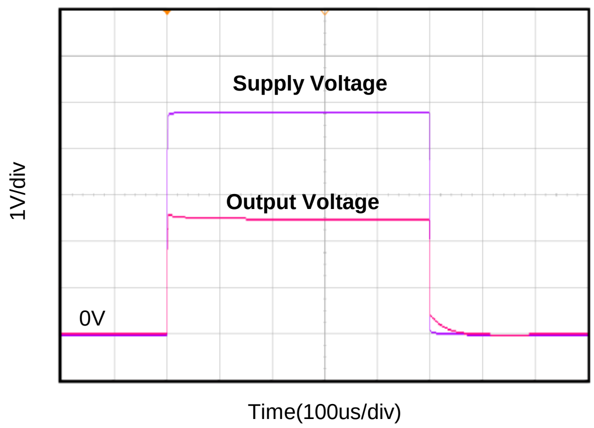


Figure 11

Brownout Recovery

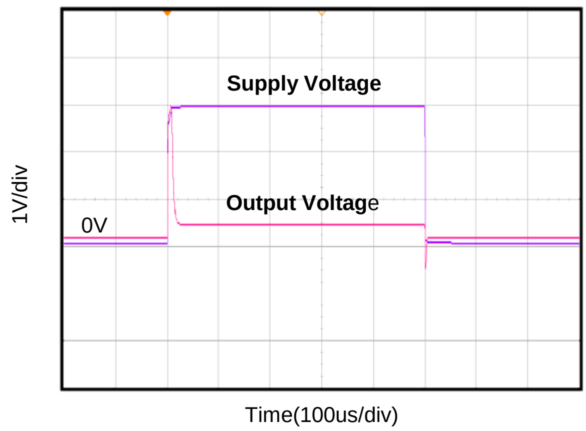


Figure 12

Typical Performance Characteristics

The TP182A1 is used for characteristics at TA = 25°C, VS = 5V, VIN+ =12V, and VREF=VS/2, unless otherwise noted

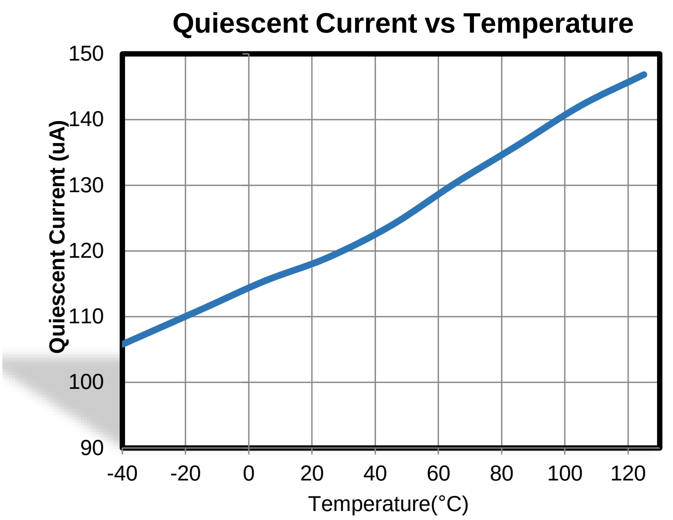


Figure 13

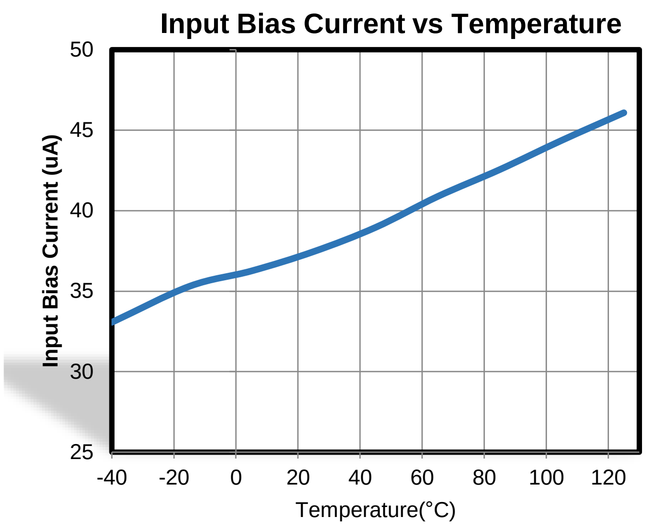


Figure 14

Pin Functions

IN-: Inverting Input of the Amplifier.

IN+: Non-Inverting Input of Amplifier.

OUT: Amplifier Output. The voltage range extends to within mV of each supply rail.

REF: Reference voltage

V+: Positive Power Supply. Typically, the voltage is from 2.7V to 30V. A bypass capacitor of 0.1μF as close to the part as possible should be used between power supply pin and ground pin.

GND: Negative Power Supply.

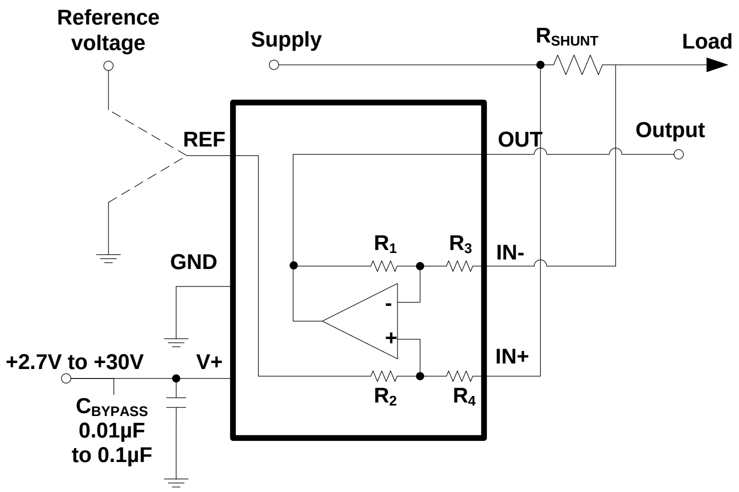
Operation Overview

The TP182 family is 36V common-mode, zero-drift topology, current-sensing amplifiers that can be used in both low-side and high-side configurations. These specially-designed, current-sensing amplifiers are able to accurately measure voltages developed across current-sensing resistors on common-mode voltages that far exceed the supply voltage powering the device. Current can be measured on input voltage rails as high as 36 V while the device can be powered from supply voltages as low as 2.7 V.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 100μV with a maximum temperature contribution of 0.5 μV/°C over the full temperature range of –40°C to 125°C.

Applications Information

Application schematic



Above figure shows the basic connections of the TP182. The input pins, IN+ and IN–, should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistor.

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

Selecting RSHUNT

The zero-drift offset performance of the TP182 offers several benefits. Most often, the primary advantage of the low offset characteristic enables lower full-scale drops across the shunt. For example, nonzero-drift current shunt monitors typically require a full-scale range of 100 mV.

The TP182 family gives equivalent accuracy at a full-scale range on the order of 10 mV. This accuracy reduces shunt dissipation by an order of magnitude with many additional benefits.

Alternatively, there are applications that must measure current over a wide dynamic range that can take advantage of the low offset on the low end of the measurement. Most often, these applications can use the lower gains of the TP182 to accommodate larger shunt drops on the upper end of the scale. For instance, a TP182A1 operating on a 3.3-V supply could easily handle a full-scale shunt drop of 60 mV, with only 100uV of offset.

REF Input Impedance Effects

As with any difference amplifier, the TP182 family common-mode rejection ratio is affected by any impedance present at the REF input. This concern is not a problem when the REF pin is connected directly to most references or power supplies. When using resistive dividers from the power supply or a reference voltage, the REF pin should be buffered by an op amp.

Power Supply Recommendation

The input circuitry of the TP182 can accurately measure beyond its power-supply voltage, V+. For example, the V+ power supply can be 5 V, whereas the load power-supply voltage can be as high as 30 V. However, the output voltage range of the OUT pin is limited by the voltages on the power-supply pin. Note also that the TP182 can withstand the full input signal range up to 36 V at the input pins, regardless of whether the device has power applied or not.

Proper Board Layout

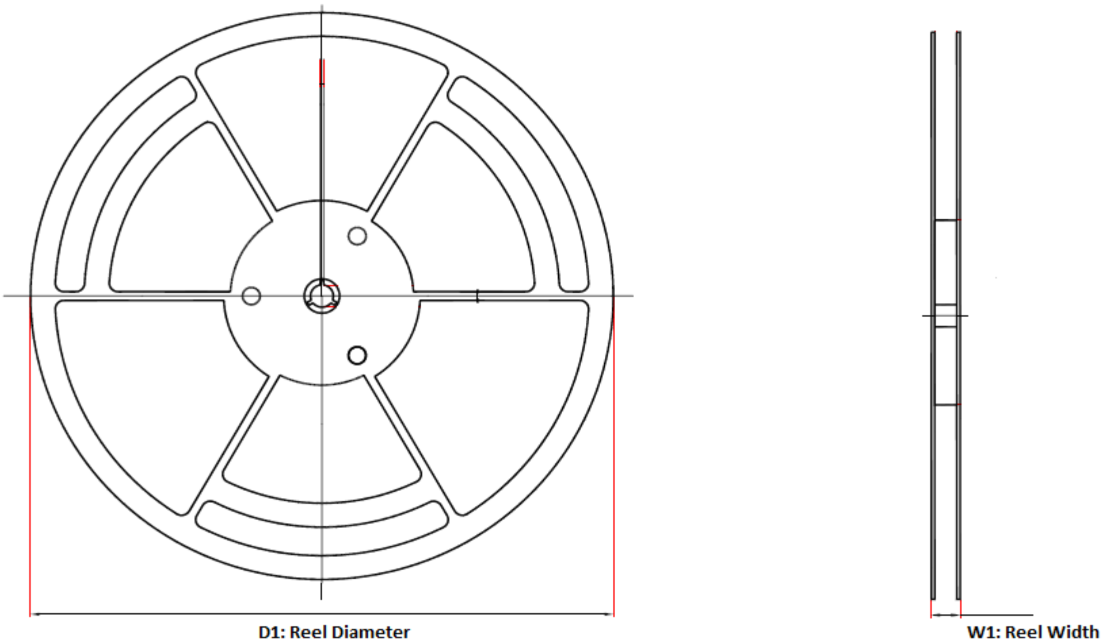
To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

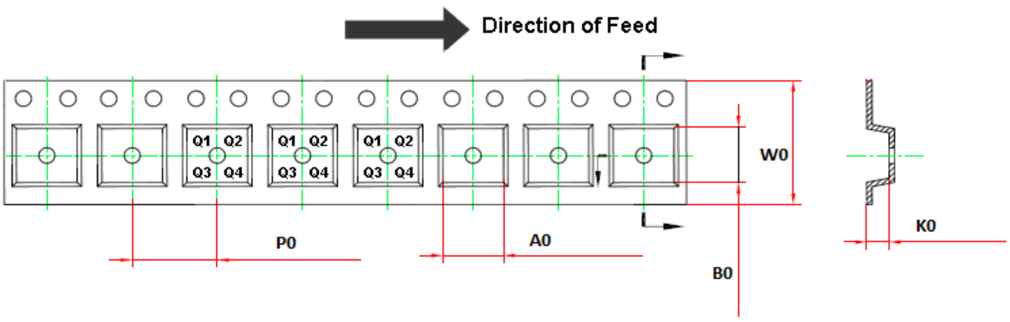
Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

Tape and Reel Information



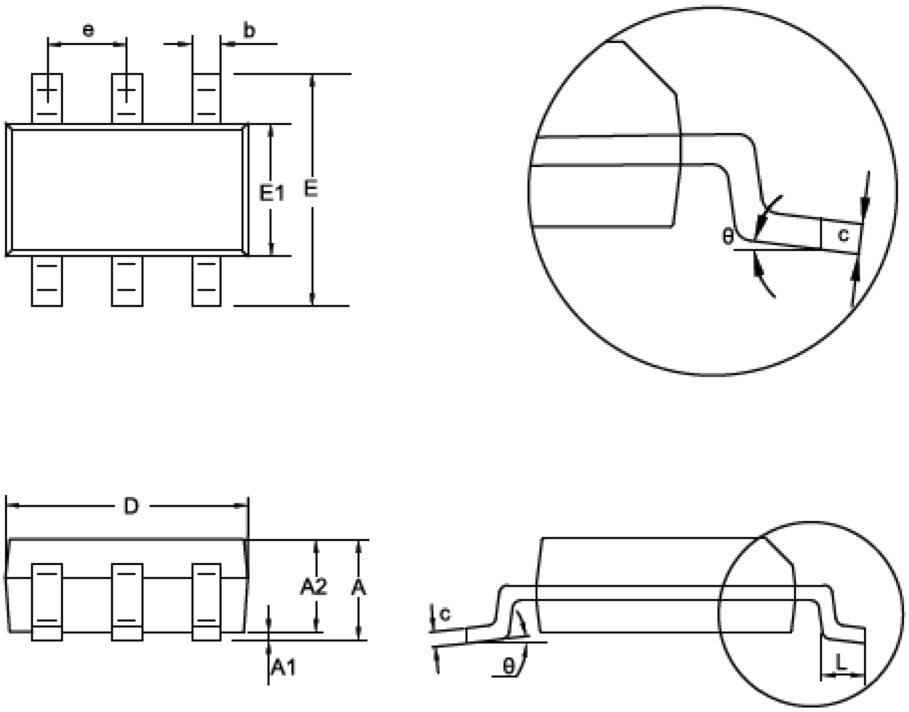


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TP182xx-CR	SOT363(SC70-6)	178.0	12.1	2.4	2.5	1.2	4.0	8.0	Q3

Package Outline Dimensions

SC70-6 /SOT-363

Package Outline Dimensions SC6(SOT363-6-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.850	1.100	0.033	0.043
A1	0.000	0.100	0.000	0.004
A2	0.800	1.000	0.031	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.230	0.003	0.009
D	2.000	2.200	0.079	0.087
E	2.150	2.450	0.085	0.096
E1	1.150	1.350	0.045	0.053
e	0.650 BSC		0.026 BSC	
L	0.260	0.460	0.010	0.018
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

IMPORTANT NOTICE AND DISCLAIMER

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