8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation

Features

- 8-bit Dual-Supply Translating Transceiver with Configurable Voltage Translation
- Dual DIR Control Pins to Allow Different Transation Direction at the Same Time
- Support Suspend Mode
- Supports Partial Power-down Mode
- Max Data Rate:
  - 380 Mbps at V_{CCA} = 1.8 V and V_{CCB} = 3.3 V
  - 200 Mbps at V_{CCA} = 1.1 V and V_{CCB} = 3.3 V
  - 200 Mbps at V_{CCA} = 1.1 V and V_{CCB} = 2.5 V
  - 200 Mbps at V_{CCA} = 1.1 V and V_{CCB} = 1.8 V
  - 150 Mbps at V_{CCA} = 1.1 V and V_{CCB} = 1.5 V
  - 100 Mbps at V_{CCA} = 1.1 V and V_{CCB} = 1.2 V
- Voltage-Level Translation between:
  - V_{CCA} Range: 0.8 V to 5.5 V
  - V_{CCB} Range: 0.8 V to 5.5 V
- ESD Protection:
  - A Port ±8000-V Human-Body Model
  - B Port ±8000-V Human-Body Model
  - 1000-V Charged-Device Model

Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer Handsets
- Industrial Automation

Description

The T74V8T245 device is an 8-bit level shifter with an enable ($\overline{OE}$) input and can work within the V_{CCA} range from 0.8 V to 5.5 V and the V_{CCB} range from 0.8 V to 5.5 V.

The T74V8T245 enables asynchronous communication between data buses. Depending on the logic level of the direction control (DIRn) input, this device transmits data either from the A bus to the B bus or from the B bus to the A bus. The output enable ($\overline{OE}$) pin can be used to disable the outputs, effectively isolating the buses.

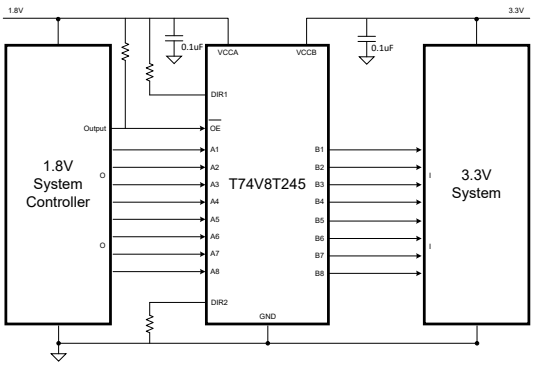
The enable control pin ($\overline{OE}$) and direction control pin (DIRn) of the T74V8T245 are powered by V_{CCA}.

The T74V8T245 fully complies with the specifications for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging backflow current through the device when it is powered down.

For high-impedance operation during power-up/power-down conditions, the output enable ($\overline{OE}$) pin must be tied to V_{CCA} via a pull-up resistor. The minimum resistor value depends on the sink current capability of the driver.

The T74V8T245 is available in the TSSOP24 and QFN5.5X3.5-24 packages are characterized from −40°C to +125°C.

Typical Application



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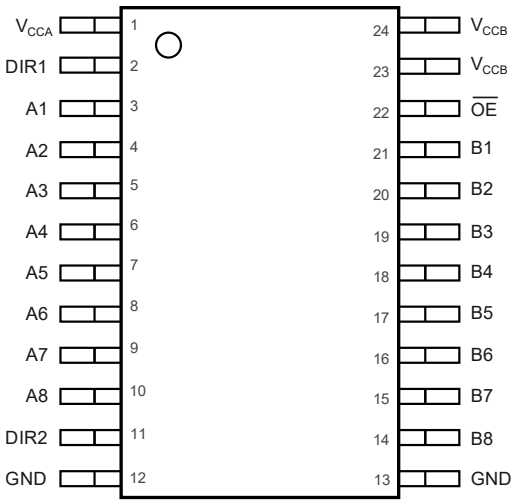
Revision History

Date	Revision	Notes
2025-03-26	Rev.P.0	Initial version
2026-01-22	Rev.A.0	Released version
2026-06-16	Rev.A.1	Changed the V_{CCA} and V_{CCB} range from 0.8 V ~ 3.6 V to 0.8 V ~ 5.5 V Added support for 5 V voltage specifications Added the QFN5.5X3.5-24 package The actual product remains unchanged

Pin Configuration and Functions

T74V8T245-TS5R
TSSOP24
Top View



T74V8T245-QN7R
QFN5.5X3.5-24
Top View

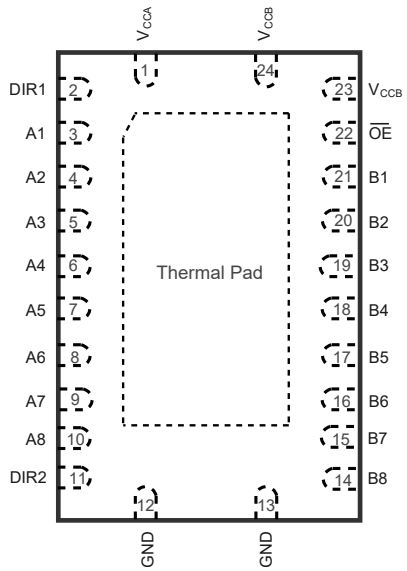


Table 1. Pin Functions: T74V8T245

Pin		I/O	Description
No.	Name		
1	V_{CCA}	P	Side-A Supply Voltage
2	DIR1	I	Direction-control '1'. Referenced to V_{CCA}
3	A1	I/O	Input/output A1. Referenced to V_{CCA}
4	A2	I/O	Input/output A2. Referenced to V_{CCA}
5	A3	I/O	Input/output A3. Referenced to V_{CCA}
6	A4	I/O	Input/output A4. Referenced to V_{CCA}
7	A5	I/O	Input/output A5. Referenced to V_{CCA}
8	A6	I/O	Input/output A6. Referenced to V_{CCA}
9	A7	I/O	Input/output A7. Referenced to V_{CCA}
10	A8	I/O	Input/output A8. Referenced to V_{CCA}
11	DIR2	I	Direction-control '2'. Referenced to V_{CCA}
12	GND	P	Supply Ground
13	GND	P	Supply Ground
14	B8	I/O	Input/output B8. Referenced to V_{CCB}

Pin		I/O	Description
No.	Name		
15	B7	I/O	Input/output B7. Referenced to V_{CCB}
16	B6	I/O	Input/output B6. Referenced to V_{CCB}
17	B5	I/O	Input/output B5. Referenced to V_{CCB}
18	B4	I/O	Input/output B4. Referenced to V_{CCB}
19	B3	I/O	Input/output B3. Referenced to V_{CCB}
20	B2	I/O	Input/output B2. Referenced to V_{CCB}
21	B1	I/O	Input/output B1. Referenced to V_{CCB}
22	$\overline{OE}$	I	Active-low Enable Input, Reference to V_{CCA}
23	V_{CCB}	P	Side-B Supply Voltage
24	V_{CCB}	P	Side-B Supply Voltage
PAD(1)			The Thermal Pad is recommended to be connected to the ground

(1) For the QFN package only.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CCA}	Supply Voltage, Side-A	−0.5	6.5	V
V_{CCB}	Supply Voltage, Side-B	−0.5	6.5	V
I_{IK}	Input Clamp Current, V_I < 0	−50		mA
V_I	Input Voltage Range, Side-A	−0.5	6.5	V
	Input Voltage Range, Side-B	−0.5	6.5	V
I_{OK}	Output Clamp Current, $V_{I/O}$ < 0	−50		mA
V_O	Output Voltage, Active Mode	−0.5	V_{cco} + 0.5	V
	Output Voltage, Suspend or 3-state Mode	−0.5	6.5	V
I_O	Output Current, V_O = 0 V to V_{CCO}	−50	50	mA
I_{CC}	Continuous Current through Each V_{CCA}, V_{CCB}, or GND		100	mA
I_{GND}	Ground Current	−100		
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The values of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.
(4) V_{CCO} is the supply voltage of the output side-A or side-B port.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Value	Unit
HBM	Human Body Model ESD, Side-A Ports	ANSI/ESDA/JEDEC JS-001 (1)	±8	kV
	Human Body Model ESD, Side-B Ports	ANSI/ESDA/JEDEC JS-001 (1)	±8	kV
CDM	Charged Device Model ESD, Side-A and Side-B Ports	ANSI/ESDA/JEDEC JS-002 (2)	±1	kV
LU	Latch up	LU, per JESD78, All Pins (3)	±100	mA

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Test at the temperature of 25℃.

Recommended Operating Conditions

Parameter		Conditions	Min	Typ	Max	Unit
V_{CCA}	Supply Voltage, Side-A		0.8		5.5	V
V_{CCB}	Supply Voltage, Side-B		0.8		5.5	V
V_I	Input Voltage		0		5.5	V
V_O	Output Voltage	Active mode	0		V_{CCO}	V
		Suspend or 3-state mode	0		5.5	V
T_{amb}	Ambient Temperature		−40		125	°C
Δt/ΔV	Input Transition Rise and Fall Rate	V_{CCI} = 0.8 V to 5.5 V			5	ns/V

(1) V_{CCO} is the supply voltage of the output side-A or side-B port.
(2) V_{CCI} is the supply voltage of the input side-A or side-B port.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP24	116.7	48.5	°C/W
QFN5.5X3.5-24	49.2	46.1	°C/W

Electrical Characteristics

All test conditions: V_{CCA} = 0.8 V to 5.5 V, V_{CCB} = 0.8 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level Output Voltage	I_O = 100 uA, V_{CCA}= 0.8 V to 5.5 V, V_{CCB} = 0.8 V to 5.5 V			0.1	V
		I_O = 3 mA, V_{CCA} = V_{CCB} = 1.1 V			0.25	V
		I_O = 6 mA, V_{CCA}= V_{CCB} = 1.4 V			0.35	V
		I_O = 8 mA, V_{CCA} = V_{CCB} = 1.65 V			0.45	V
		I_O = 9 mA, V_{CCA} = V_{CCB} = 2.3 V			0.55	V
		I_O = 12 mA, V_{CCA} = V_{CCB} = 3 V			0.7	V
		I_O = 24 mA, V_{CCA} = V_{CCB} = 3 V			0.8	V
		I_O = 32 mA, V_{CCA} = V_{CCB} = 4.5 V			0.95	V
V_{OH}	HIGH-level Output Voltage	I_O = −100 uA, V_{CCA}= 0.8 V to 5.5 V, V_{CCB} = 0.8 V to 5.5 V	V_{CCO} - 0.1			V
		I_O= −3 mA, V_{CCA} = V_{CCB} = 1.1 V	0.85			V
		I_O= −6 mA, V_{CCA} = V_{CCB} = 1.4 V	1.05			V
		I_O= −8 mA, V_{CCA} = V_{CCB} = 1.65 V	1.2			V
		I_O= −9 mA, V_{CCA} = V_{CCB} = 2.3 V	1.75			V
		I_O= −12 mA, V_{CCA} = V_{CCB} = 3 V	2.3			V
		I_O= −24 mA, V_{CCA} = V_{CCB} = 3 V	V_{CCO} - 0.8			V
		I_O= −32 mA, V_{CCA} = V_{CCB} = 4.5 V	V_{CCO} - 0.95			V
V_{IL}	LOW-level Input Voltage (Data Input)	V_{CCI} = 0.8 V			0.3 x V_{CCI}	V
		V_{CCI} = 1.1 V to 1.95 V			0.35 x V_{CCI}	V
		V_{CCI} = 2.3 V to 2.7 V			0.7	V
		V_{CCI} = 3.0 V to 3.6 V			0.8	V
		V_{CCI} = 4.5 V to 5.5 V			0.3 x V_{CCI}	V
	LOW-level Input Voltage (DIRn, $\overline{OE}$ Input)	V_{CCA} = 0.8 V			0.3 x V_{CCA}	V
		V_{CCA} = 1.1 V to 1.95 V			0.35 x V_{CCA}	V
		V_{CCA} = 2.3 V to 2.7 V			0.7	V
		V_{CCA} = 3.0 V to 3.6 V			0.8	V
		V_{CCA} = 4.5 V to 5.5 V			0.3 x V_{CCA}	V

Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level Input Voltage (Data Input)	V_{CCI} = 0.8 V	0.7 x V_{CCI}			V
		V_{CCI} = 1.1 V to 1.95 V	0.65 x V_{CCI}			V
		V_{CCI} = 2.3 V to 2.7 V	1.6			V
		V_{CCI} = 3.0 V to 3.6 V	2.0			V
		V_{CCI} = 4.5 V to 5.5 V	0.7 x V_{CCI}			V
	HIGH-level Input Voltage (DIRn, $\overline{OE}$ Input)	V_{CCA} = 0.8 V	0.7 x V_{CCA}			V
		V_{CCA} = 1.1 V to 1.95 V	0.65 x V_{CCA}			V
		V_{CCA} = 2.3 V to 2.7 V	1.6			V
		V_{CCA} = 3.0 V to 3.6 V	2.0			V
		V_{CCA} = 4.5 V to 5.5 V	0.7 x V_{CCA}			V
I_I	Input Leakage Current	DIRn, $\overline{OE}$ input, V_I = 0 V or 5.5 V, V_{CCA} = 0.8 V to 5.5 V, V_{CCB}= 0.8 V to 5.5 V	−5		5	uA
I_{OFF}	Power-off Leakage Current	Suspend mode A port, V_O = 0 V or V_{CCO}, V_{CCA}= 5.5 V, V_{CCB}= 0 V	−30		30	uA
		Suspend mode B port, V_O = 0 V or V_{CCO}, V_{CCA}= 0 V, V_{CCB}= 5.5 V	−30		30	uA
I_{OZ}	OFF Dtate Output Current	A port V_I or V_O = 0 V to 5.5 V, V_{CCA}= 0.8 V to 5.5 V, V_{CCB} = 0.8 V to 5.5 V	−30		30	uA
		B port V_I or V_O = 0 V to 5.5 V, V_{CCA}= 0.8 V to 5.5 V, V_{CCB} = 0.8 V to 5.5 V	−30		30	uA
I_{CCA}	Supply Current	A port V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCA}= 0.8 V to 5.5 V, V_{CCB}= 0.8 V to 5.5 V			55	uA
		A port V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCA}= 1.1 V to 5.5 V, V_{CCB}= 1.1 V to 5.5 V			50	uA
		A port V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCA}= 5.5 V, V_{CCB}= 0 V			50	uA
		A port V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCA}= 0 V, V_{CCB}= 5.5 V	−12			uA
I_{CCB}	Supply Current	B port V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCA}= 0.8 V to 5.5 V, V_{CCB}= 0.8 V to 5.5 V			55	uA
		B port V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCA}= 1.1 V to 5.5 V, V_{CCB}= 1.1 V to 5.5 V			50	uA
		B port V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCA} = 5.5 V, V_{CCB} = 0 V	−12			uA
		B port V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCA} = 0 V, V_{CCB} = 5.5 V			50	uA

Parameter		Conditions	Min	Typ	Max	Unit
I_{CCA}+ I_{CCB}	Combined Supply Current	A plus B port, I_O = 0 A, V_I = 0 V or V_{CCI}, V_{CCA}= 0.8 V to 5.5 V, V_{CCB} = 0.8 V to 5.5 V			200	uA
		A plus B port, I_O = 0 A, V_I = 0 V or V_{CCI}, V_{CCA}= 1.1 V to 5.5 V, V_{CCB}= 1.1 V to 5.5 V			200	uA
C_I	Input Capacitance (1)	DIRn, $\overline{OE}$ input, V_I = 0 V or 5.5 V, V_{CCA} = 5.5 V, V_{CCB} = 5.5 V			6	pF
C_{IO}	Input/output Capacitance (1)	A and B port, V_O = 5.5 V or 0 V, V_{CCA}= 5.5 V, V_{CCB} = 5.5 V			10	pF

(1) Test data based on bench tests and design simulation, NOT test in production.

AC Timing Requirements — VCCA = 0.8 V

All test conditions: T_A = 25°C, the data is based on bench test and design simulation, NOT test in production, unless otherwise noted.

t_{en} includes t_{PZL} and t_{PZH}, t_{dis} includes t_{PLZ} and t_{PHZ}.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
t_{PLH} , t_{PHL}	Propagation Delay	A-to-B push-pull driving	0.8 V		14.4		ns
			1.2 V		7.0		ns
			1.5 V		6.2		ns
			1.8 V		6.0		ns
			2.5 V		5.9		ns
			3.3 V		6.0		ns
			5 V		6.0		ns
		B-to-A push-pull driving	0.8 V		14.4		ns
			1.2 V		12.4		ns
			1.5 V		12.1		ns
			1.8 V		11.9		ns
			2.5 V		11.8		ns
			3.3 V		11.8		ns
			5 V		11.8		ns
t_{en}	Enable Time	$\overline{OE}$-to-A	0.8 V		21.9		ns
			1.2 V		21.9		ns
			1.5 V		21.9		ns
			1.8 V		21.9		ns
			2.5 V		21.9		ns
			3.3 V		21.9		ns
			5 V		21.9		ns
		$\overline{OE}$-to-B	0.8 V		22.2		ns
			1.2 V		11.1		ns
			1.5 V		9.8		ns
			1.8 V		9.4		ns
			2.5 V		9.4		ns
			3.3 V		9.6		ns
			5 V		9.6		ns
t_{dis}	Disable Time	$\overline{OE}$-to-A	0.8 V		16.2		ns
			1.2 V		16.2		ns
			1.5 V		16.2		ns
			1.8 V		16.2		ns

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
			2.5 V		16.2		ns
			3.3 V		16.2		ns
			5 V		16.2		ns
		$\overline{OE}$-to-B	0.8 V		17.6		ns
			1.2 V		10.0		ns
			1.5 V		9.0		ns
			1.8 V		9.1		ns
			2.5 V		8.7		ns
			5.5 V		9.3		ns
			3.3 V		9.3		ns
C_{PD}	Power Dissipation Capacitance	A port, A-to-B, output enable	0.8 V		0.2		pF
		A port, A-to-B, output disable			0.2		pF
		A port, B-to-A, output enable			9		pF
		A port, B-to-A, output disable			0.6		pF
		B port, A-to-B, output enable			9		pF
		B port, A-to-B, output disable			0.6		pF
		B port, B-to-A, output enable			0.2		pF
		B port, B-to-A, output disable			0.2		pF

AC Timing Requirements — VCCA = 1.2 V

All test conditions: T_A = −40°C to +125°C, V_{CCA} = 1.2 V ± 0.1 V, the data is based on bench test and design simulation, NOT test in production, unless otherwise noted.

t_{en} includes t_{PZL} and t_{PZH}, t_{dis} includes t_{PLZ} and t_{PHZ}.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
t_{PLH} , t_{PHL}	Propagation Delay	A-to-B push-pull driving	0.8 V		7.0		
			1.2 V ± 0.1 V	0.5		9.5	ns
			1.5 V ± 0.1 V	0.5		7.4	ns
			1.8 V ± 0.15 V	0.5		6.4	ns
			2.5 V ± 0.2 V	0.5		5.4	ns
			3.3 V ± 0.3 V	0.5		5.3	ns
			5 V ± 0.5 V	0.5		5.3	ns
		B-to-A push-pull driving	0.8 V		12.4		
			1.2 V ± 0.1 V	0.5		9.9	ns
			1.5 V ± 0.1 V	0.5		9.4	ns
			1.8 V ± 0.15 V	0.5		9.2	ns
			2.5 V ± 0.2 V	0.5		8.8	ns
			3.3 V ± 0.3 V	0.5		8.6	ns
			5 V ± 0.5 V	0.5		8.6	ns
t_{en}	Enable Time	$\overline{OE}$-to-A	0.8 V		21.9		
			1.2 V ± 0.1 V	1.1		15.9	ns
			1.5 V ± 0.1 V	1.1		15.9	ns
			1.8 V ± 0.15 V	1.1		15.9	ns
			2.5 V ± 0.2 V	1.1		15.9	ns
			3.3 V ± 0.3 V	1.1		15.9	ns
			5 V ± 0.5 V	1.1		15.9	ns
		$\overline{OE}$-to-B	0.8 V		11.1		
			1.2 V ± 0.1 V	1.1		15.7	ns
			1.5 V ± 0.1 V	1.1		11.5	ns
			1.8 V ± 0.15 V	1.1		9.9	ns
			2.5 V ± 0.2 V	1.0		8.5	ns
			3.3 V ± 0.3 V	1.0		8.1	ns
			5 V ± 0.5 V	1.0		8.1	ns
t_{dis}	Disable Time	$\overline{OE}$-to-A	0.8 V		16.2		
			1.2 V ± 0.1 V	0.5		13.0	ns
			1.5 V ± 0.1 V	0.5		13.0	ns
			1.8 V ± 0.15 V	0.5		13.0	ns

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
			2.5 V ± 0.2 V	0.5		13.0	ns
			3.3 V ± 0.3 V	0.5		13.0	ns
			5 V ± 0.5 V	0.5		13.0	ns
		$\overline{OE}$-to-B	0.8 V		10.0		
			1.2 V ± 0.1 V	0.5		13.6	ns
			1.5 V ± 0.1 V	0.5		10.5	ns
			1.8 V ± 0.15 V	0.5		10.4	ns
			2.5 V ± 0.2 V	0.5		8.8	ns
			3.3 V ± 0.3 V	0.5		9.8	ns
			5 V ± 0.5 V	0.5		9.8	ns
C_{PD}(1)	Power Dissipation Capacitance	A port, A-to-B, output enable	1.2 V		0.2		pF
		A port, A-to-B, output disable			0.2		pF
		A port, B-to-A, output enable			9		pF
		A port, B-to-A, output disable			0.6		pF
		B port, A-to-B, output enable			9		pF
		B port, A-to-B, output disable			0.6		pF
		B port, B-to-A, output enable			0.2		pF
		B port, B-to-A, output disable			0.2		pF

(1) C_{PD} test conditions: V_{CCA} = 1.2 V and T_A = 25°C.
(2) Test condition: T_A = 25°C.

AC Timing Requirements — VCCA = 1.5 V

All test conditions: T_A = −40°C to +125°C, V_{CCA} = 1.5 V ± 0.1 V, the data is based on bench test and design simulation, NOT test in production, unless otherwise noted.

t_{en} includes t_{PZL} and t_{PZH}, t_{dis} includes t_{PLZ} and t_{PHZ}.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
t_{PLH} , t_{PHL}	Propagation Delay	A-to-B push-pull driving	0.8 V		6.2		
			1.2 V ± 0.1 V	0.5		9.4	ns
			1.5 V ± 0.1 V	0.5		6.2	ns
			1.8 V ± 0.15 V	0.5		5.2	ns
			2.5 V ± 0.2 V	0.5		4.9	ns
			3.3 V ± 0.3 V	0.5		4.6	ns
			5 V ± 0.5 V	0.5		4.6	ns
		B-to-A push-pull driving	0.8 V		12.1		
			1.2 V ± 0.1 V	0.5		7.4	ns
			1.5 V ± 0.1 V	0.5		6.2	ns
			1.8 V ± 0.15 V	0.5		5.9	ns
			2.5 V ± 0.2 V	0.5		5.8	ns
			3.3 V ± 0.3 V	0.5		5.5	ns
			5 V ± 0.5 V	0.5		5.5	ns
t_{en} (1)	Enable Time	$\overline{OE}$-to-A	0.8 V		21.9		
			1.2 V ± 0.1 V	1.1		9.6	ns
			1.5 V ± 0.1 V	1.1		9.6	ns
			1.8 V ± 0.15 V	1.1		9.6	ns
			2.5 V ± 0.2 V	1.1		9.6	ns
			3.3 V ± 0.3 V	1.1		9.6	ns
			5 V ± 0.5 V	1.1		9.6	ns
		$\overline{OE}$-to-B	0.8 V		9.8		
			1.2 V ± 0.1 V	1.1		14.1	ns
			1.5 V ± 0.1 V	1.1		9.0	ns
			1.8 V ± 0.15 V	1.1		7.9	ns
			2.5 V ± 0.2 V	1.0		6.2	ns
			3.3 V ± 0.3 V	1.0		5.8	ns
			5 V ± 0.5 V	1.0		5.8	ns
t_{dis} (1)	Disable Time	$\overline{OE}$-to-A	0.8 V		16.2		
			1.2 V ± 0.1 V	0.5		9.5	ns
			1.5 V ± 0.1 V	0.5		9.5	ns
			1.8 V ± 0.15 V	0.5		9.5	ns

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
			2.5 V ± 0.2 V	0.5		9.5	ns
			3.3 V ± 0.3 V	0.5		9.5	ns
			5 V ± 0.5 V	0.5		9.5	ns
		$\overline{OE}$-to-B	0.8 V		9.0		
			1.2 V ± 0.1 V	0.5		12.4	ns
			1.5 V ± 0.1 V	0.5		9.3	ns
			1.8 V ± 0.15 V	0.5		8.4	ns
			2.5 V ± 0.2 V	0.5		8.0	ns
			3.3 V ± 0.3 V	0.5		8.6	ns
			5 V ± 0.5 V	0.5		8.6	ns
C_{PD} (1)	Power Dissipation Capacitance	A port, A-to-B, output enable	1.5 V		0.2		pF
		A port, A-to-B, output disable			0.2		pF
		A port, B-to-A, output enable			10		pF
		A port, B-to-A, output disable			0.6		pF
		B port, A-to-B, output enable			10		pF
		B port, A-to-B, output disable			0.6		pF
		B port, B-to-A, output enable			0.2		pF
		B port, B-to-A, output disable			0.2		pF

(1) C_{PD} tested conditions: V_{CCA} = 1.5 V and T_A = 25°C.
(2) Test condition: T_A = 25°C.

AC Timing Requirements — VCCA = 1.8 V

All test conditions: T_A = −40°C to +125°C, V_{CCA} = 1.8 V ± 0.15 V, the data is based on bench test and design simulation, NOT test in production, unless otherwise noted.

t_{en} includes t_{PZL} and t_{PZH}, t_{dis} includes t_{PLZ} and t_{PHZ}.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
t_{PLH} , t_{PHL}	Propagation Delay	A-to-B push-pull driving	0.8 V		6.0		
			1.2 V ± 0.1 V	0.5		9.2	ns
			1.5 V ± 0.1 V	0.5		5.9	ns
			1.8 V ± 0.15 V	0.5		5.0	ns
			2.5 V ± 0.2 V	0.5		4.2	ns
			3.3 V ± 0.3 V	0.5		3.9	ns
			5 V ± 0.5 V	0.5		3.9	ns
		B-to-A push-pull driving	0.8 V		11.9		
			1.2 V ± 0.1 V	0.5		6.4	ns
			1.5 V ± 0.1 V	0.5		5.2	ns
			1.8 V ± 0.15 V	0.5		5.0	ns
			2.5 V ± 0.2 V	0.5		4.8	ns
			3.3 V ± 0.3 V	0.5		4.6	ns
			5 V ± 0.5 V	0.5		4.6	ns
t_{en}	Enable Time	$\overline{OE}$-to-A	0.8 V		21.9		
			1.2 V ± 0.1 V	1.0		7.5	ns
			1.5 V ± 0.1 V	1.0		7.5	ns
			1.8 V ± 0.15 V	1.0		7.5	ns
			2.5 V ± 0.2 V	1.0		7.5	ns
			3.3 V ± 0.3 V	1.0		7.5	ns
			5 V ± 0.5 V	1.0		7.5	ns
		$\overline{OE}$-to-B	0.8 V		9.4		
			1.2 V ± 0.1 V	1.1		13.7	ns
			1.5 V ± 0.1 V	1.1		9.1	ns
			1.8 V ± 0.15 V	1.0		7.4	ns
			2.5 V ± 0.2 V	0.5		5.7	ns
			5 V ± 0.5 V	0.5		5.0	ns
			3.3 V ± 0.3 V	0.5		5.0	ns
t_{dis}	Disable Time	$\overline{OE}$-to-A	0.8 V		16.2		
			1.2 V ± 0.1 V	0.5		7.9	ns
			1.5 V ± 0.1 V	0.5		7.9	ns
			1.8 V ± 0.15 V	0.5		7.9	ns

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
			2.5 V ± 0.2 V	0.5		7.9	ns
			3.3 V ± 0.3 V	0.5		7.9	ns
			5 V ± 0.5 V	0.5		7.9	ns
		$\overline{OE}$-to-B	0.8 V		9.1		
			1.2 V ± 0.1 V	0.5		12.0	ns
			1.5 V ± 0.1 V	0.5		8.6	ns
			1.8 V ± 0.15 V	0.5		7.6	ns
			2.5 V ± 0.2 V	0.5		6.6	ns
			3.3 V ± 0.3 V	0.5		6.4	ns
			5 V ± 0.5 V	0.5		6.4	ns
C_{PD} (1)	Power Dissipation Capacitance	A port, A-to-B, output enable	1.8 V		0.3		pF
		A port, A-to-B, output disable			0.3		pF
		A port, B-to-A, output enable			10		pF
		A port, B-to-A, output disable			0.7		pF
		B port, A-to-B, output enable			10		pF
		B port, A-to-B, output disable			0.7		pF
		B port, B-to-A, output enable			0.3		pF
		B port, B-to-A, output disable			0.3		pF

(1) C_{PD} teste conditions: V_{CCA} = 1.8 V and T_A = 25°C.
(2) Teste condition: T_A = 25°C.

AC Timing Requirements — VCCA = 2.5 V

All test conditions: T_A = −40°C to +125°C, V_{CCA} = 2.5 V ± 0.2 V, the data is based on bench test and design simulation, NOT test in production, unless otherwise noted.

t_{en} includes t_{PZL} and t_{PZH}, t_{dis} includes t_{PLZ} and t_{PHZ}.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
t_{PLH} , t_{PHL}	Propagation Delay	A-to-B push-pull driving	0.8 V		5.9		
			1.2 V ± 0.1 V	0.5		8.8	ns
			1.5 V ± 0.1 V	0.5		5.8	ns
			1.8 V ± 0.15 V	0.5		4.8	ns
			2.5 V ± 0.2 V	0.5		3.7	ns
			3.3 V ± 0.3 V	0.5		3.2	ns
			5 V ± 0.5 V	0.5		3.2	ns
		B-to-A push-pull driving	0.8 V		11.8		
			1.2 V ± 0.1 V	0.5		5.4	ns
			1.5 V ± 0.1 V	0.5		4.9	ns
			1.8 V ± 0.15 V	0.5		4.2	ns
			2.5 V ± 0.2 V	0.5		3.7	ns
			3.3 V ± 0.3 V	0.5		3.5	ns
			5 V ± 0.5 V	0.5		3.5	ns
t_{en}	Enable Time	$\overline{OE}$-to-A	0.8 V		21.9		
			1.2 V ± 0.1 V	0.5		5.3	ns
			1.5 V ± 0.1 V	0.5		5.3	ns
			1.8 V ± 0.15 V	0.5		5.3	ns
			2.5 V ± 0.2 V	0.5		5.3	ns
			3.3 V ± 0.3 V	0.5		5.3	ns
			5 V ± 0.5 V	0.5		5.3	ns
		$\overline{OE}$-to-B	0.8 V		9.4		
			1.2 V ± 0.1 V	1.1		13.1	ns
			1.5 V ± 0.1 V	1.1		8.7	ns
			1.8 V ± 0.15 V	0.5		7.1	ns
			2.5 V ± 0.2 V	0.5		5.1	ns
			3.3 V ± 0.3 V	0.5		4.4	ns
			5 V ± 0.5 V	0.5		4.4	ns
t_{dis}	Disable Time	$\overline{OE}$-to-A	0.8 V		16.2		
			1.2 V ± 0.1 V	0.5		5.7	ns
			1.5 V ± 0.1 V	0.5		5.7	ns
			1.8 V ± 0.15 V	0.5		5.7	ns

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
			2.5 V ± 0.2 V	0.5		5.7	ns
			3.3 V ± 0.3 V	0.5		5.7	ns
			5 V ± 0.5 V	0.5		5.7	ns
		$\overline{OE}$-to-B	0.8 V		8.7		
			1.2 V ± 0.1 V	0.5		11.5	ns
			1.5 V ± 0.1 V	0.5		7.9	ns
			1.8 V ± 0.15 V	0.5		7.0	ns
			2.5 V ± 0.2 V	0.5		5.7	ns
			3.3 V ± 0.3 V	0.5		5.8	ns
			5 V ± 0.5 V	0.5		5.8	ns
C_{PD} (1)	Power Dissipation Capacitance	A port, A-to-B, output enable	2.5 V		0.4		pF
		A port, A-to-B, output disable			0.4		pF
		A port, B-to-A, output enable			11		pF
		A port, B-to-A, output disable			0.7		pF
		B port, A-to-B, output enable			11		pF
		B port, A-to-B, output disable			0.7		pF
		B port, B-to-A, output enable			0.4		pF
		B port, B-to-A, output disable			0.4		pF

(1) C_{PD} teste conditions: V_{CCA} = 2.5 V and T_A = 25°C.
(2) Teste conditions: T_A = 25°C.

AC Timing Requirements — VCCA = 3.3 V

All test conditions: T_A = −40°C to +125°C, V_{CCA} = 3.3 V ± 0.3 V, the data is based on bench test and design simulation, NOT test in production, unless otherwise noted.

t_{en} includes t_{PZL} and t_{PZH}, t_{dis} includes t_{PLZ} and t_{PHZ}.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
t_{PLH} , t_{PHL}	Propagation Delay	A-to-B push-pull driving	0.8 V		7.0		
			1.2 V ± 0.1 V	0.5		8.6	ns
			1.5 V ± 0.1 V	0.5		5.5	ns
			1.8 V ± 0.15 V	0.5		4.6	ns
			2.5 V ± 0.2 V	0.5		3.5	ns
			3.3 V ± 0.3 V	0.5		3.0	ns
			5 V ± 0.5 V	0.5		3.0	ns
		B-to-A push-pull driving	0.8 V		12.4		
			1.2 V ± 0.1 V	0.5		5.3	ns
			1.5 V ± 0.1 V	0.5		4.6	ns
			1.8 V ± 0.15 V	0.5		3.9	ns
			2.5 V ± 0.2 V	0.5		3.2	ns
			3.3 V ± 0.3 V	0.5		3.0	ns
			5 V ± 0.5 V	0.5		3.0	ns
t_{en}	Enable Time	$\overline{OE}$-to-A	0.8 V		21.9		
			1.2 V ± 0.1 V	0.5		4.4	ns
			1.5 V ± 0.1 V	0.5		4.4	ns
			1.8 V ± 0.15 V	0.5		4.4	ns
			2.5 V ± 0.2 V	0.5		4.4	ns
			3.3 V ± 0.3 V	0.5		4.4	ns
			5 V ± 0.5 V	0.5		4.4	ns
		$\overline{OE}$-to-B	0.8 V		11.1		
			1.2 V ± 0.1 V	1.1		12.9	ns
			1.5 V ± 0.1 V	1.1		8.6	ns
			1.8 V ± 0.15 V	0.5		6.9	ns
			2.5 V ± 0.2 V	0.5		5.0	ns
			3.3 V ± 0.3 V	1.0		4.3	ns
			5 V ± 0.5 V	1.0		4.3	ns
t_{dis}	Disable Time	$\overline{OE}$-to-A	0.8 V		16.2		
			1.2 V ± 0.1 V	0.5		5.4	ns
			1.5 V ± 0.1 V	0.5		5.4	ns
			1.8 V ± 0.15 V	0.5		5.4	ns

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
			2.5 V ± 0.2 V	0.5		5.4	ns
			3.3 V ± 0.3 V	0.5		5.4	ns
			5 V ± 0.5 V	0.5		5.4	ns
		$\overline{OE}$-to-B	0.8 V		10.0		
			1.2 V ± 0.1 V	0.5		11.2	ns
			1.5 V ± 0.1 V	0.5		8.6	ns
			1.8 V ± 0.15 V	0.5		6.9	ns
			2.5 V ± 0.2 V	0.5		5.0	ns
			3.3 V ± 0.3 V	0.5		4.3	ns
			5 V ± 0.5 V	0.5		4.3	ns
C_{PD} (1)	Power Dissipation Capacitance	A port, A-to-B, output enable	3.3 V		0.5		pF
		A port, A-to-B, output disable			0.5		pF
		A port, B-to-A, output enable			13		pF
		A port, B-to-A, output disable			0.8		pF
		B port, A-to-B, output enable			13		pF
		B port, A-to-B, output disable			0.8		pF
		B port, B-to-A, output enable			0.5		pF
		B port, B-to-A, output disable			0.5		pF

(1) C_{PD} test conditions: V_{CCA} = 3.3 V and T_A = 25°C.
(2) Test conditions: T_A = 25°C.

AC Timing Requirements — VCCA = 5 V

All test conditions: T_A = −40°C to +125°C, V_{CCA} = 5 V ± 0.5 V, the data is based on bench test and design simulation, not test in production, unless otherwise noted.

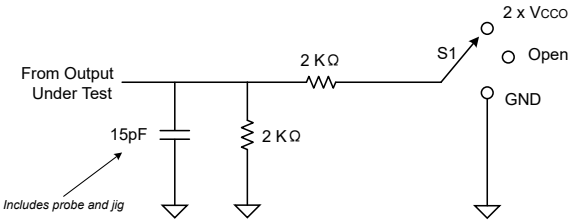
t_{en} includes t_{PZL} and t_{PHL}, t_{dis} includes t_{PLZ} and t_{PHZ}.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
t_{PLH} , t_{PHL}	Propagation Delay	A-to-B push-pull driving	0.8 V(2)		6.5		
			1.2 V ± 0.1 V	0.5		7.9	ns
			1.5 V ± 0.1 V	0.5		5.4	ns
			1.8 V ± 0.15 V	0.5		4.6	ns
			2.5 V ± 0.2 V	0.5		3.5	ns
			3.3 V ± 0.3 V	0.5		3.0	ns
			5 V ± 0.5 V	0.5		3.0	ns
		B-to-A push-pull driving	0.8 V(2)		11.9		
			1.2 V ± 0.1 V	0.5		5.1	ns
			1.5 V ± 0.1 V	0.5		4.4	ns
			1.8 V ± 0.15 V	0.5		3.9	ns
			2.5 V ± 0.2 V	0.5		3.2	ns
			3.3 V ± 0.3 V	0.5		3.0	ns
			5 V ± 0.5 V	0.5		3.0	ns
t_{en}	Enable Time	$\overline{OE}$-to-A	0.8 V(2)		21.4		
			1.2 V ± 0.1 V	0.5		4.2	ns
			1.5 V ± 0.1 V	0.5		4.2	ns
			1.8 V ± 0.15 V	0.5		4.2	ns
			2.5 V ± 0.2 V	0.5		4.2	ns
			3.3 V ± 0.3 V	0.5		4.2	ns
			5 V ± 0.5 V	0.5		4.2	ns
		$\overline{OE}$-to-B	0.8 V(2)		10.6		
			1.2 V ± 0.1 V	1.1		12.4	ns
			1.5 V ± 0.1 V	1.1		8.4	ns
			1.8 V ± 0.15 V	0.5		6.8	ns
			2.5 V ± 0.2 V	0.5		5.0	ns
			3.3 V ± 0.3 V	1.0		4.3	ns
			5 V ± 0.5 V	1.0		4.3	ns
t_{dis}	Disable Time	$\overline{OE}$-to-A	0.8 V(2)		15.7		
			1.2 V ± 0.1 V	0.5		5.2	ns
			1.5 V ± 0.1 V	0.5		5.2	ns
			1.8 V ± 0.15 V	0.5		5.2	ns

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
			2.5 V ± 0.2 V	0.5		5.2	ns
			3.3 V ± 0.3 V	0.5		5.2	ns
			5 V ± 0.5 V	0.5		5.2	ns
		$\overline{OE}$-to-B	0.8 V(2)		9.5		
			1.2 V ± 0.1 V	0.5		10.7	ns
			1.5 V ± 0.1 V	0.5		8.6	ns
			1.8 V ± 0.15 V	0.5		6.9	ns
			2.5 V ± 0.2 V	0.5		5.0	ns
			3.3 V ± 0.3 V	0.5		4.3	ns
			5 V ± 0.5 V	0.5		4.3	ns
C_{PD}(1)	Power Dissipation Capacitance	A port, A-to-B, output enable	5 V		0.5		pF
		A port, A-to-B, output disable			0.5		pF
		A port, B-to-A, output enable			13		pF
		A port, B-to-A, output disable			0.8		pF
		B port, A-to-B, output enable			13		pF
		B port, A-to-B, output disable			0.8		pF
		B port, B-to-A, output enable			0.5		pF
		B port, B-to-A, output disable			0.5		pF

(1) C_{PD} tested V_{CCA} = 5 V and T_A = 25°C.

Parameter Measurement Waveforms



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CCO}
t_{PHZ}/t_{PZH}	GND

Figure 1. Timing Measurement Load Circuit

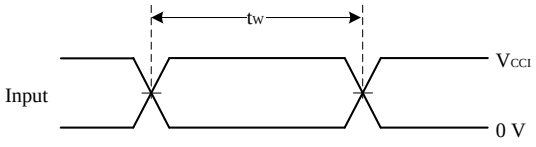


Figure 2. Pulse Duration

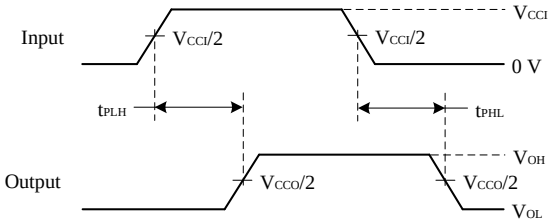
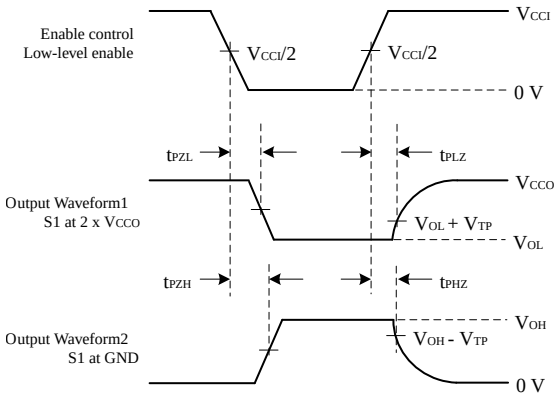


Figure 3. Propagation Delay Times



V_{CCO}	V_{TP}
0.8 V	0.1 V
1.2 V	0.1 V
1.5 V ± 0.1 V	0.1 V
1.8 V ± 0.15 V	0.15 V
2.5 V ± 0.2 V	0.15 V
3.3 V ± 0.3 V	0.3 V
5 V ± 0.5 V	0.3 V

Figure 4. Enable and Disable Times

Note:

t_{plz} and t_{phz} are the same as t_{dis}.

t_{pzl} and t_{pzh} are the same as t_{en}.

V_{CCI} is V_{CC} associated with the input port.

V_{CCO} is V_{CC} associated with the output port.

t_{PLH} and t_{PHL} are the same as t_{pd}.

Detailed Description

Overview

The T74V8T245 device is an 8-bit level shifter, and only supports Push-Pull mode, which functions with an enable ($\overline{OE}$) input and can work within the V_{CCA} range from 0.8 V to 5.5 V and the V_{CCB} range from 0.8 V to 5.5 V. V_{CCA} powers the A-port and control pins (DIRn and $\overline{OE}$), while V_{CCB} supplies the B-port. The A-port supports I/O voltage levels from 0.8 V to 5.5 V, and the B-port also accommodates I/O voltages ranging from 0.8 V to 5.5 V.

Functional Block Diagram

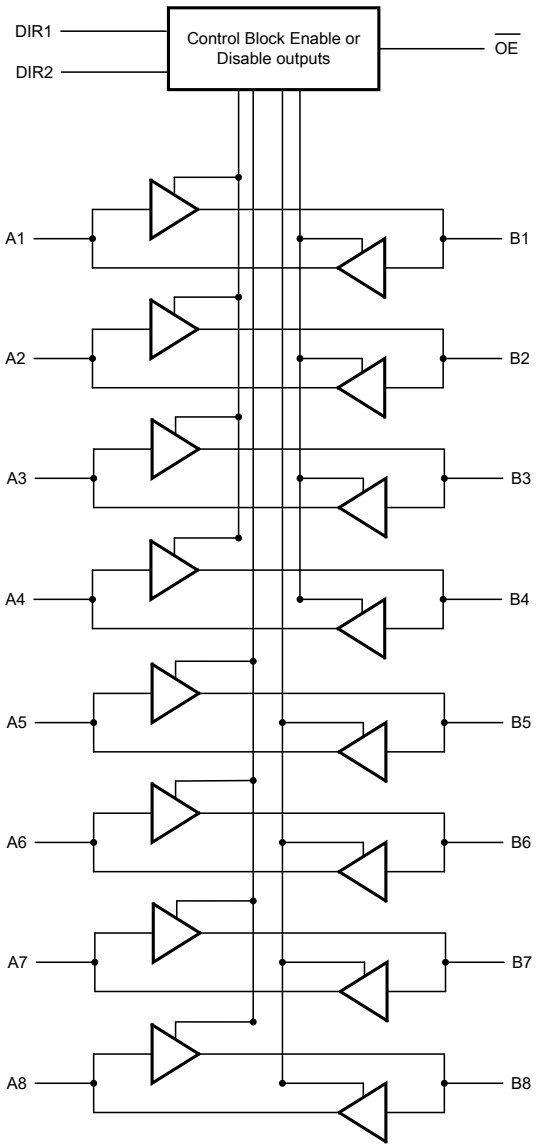


Figure 5. Functional Block Diagram

Feature Description

I_{off} Feature

The I_{off} feature supports Partial-Power-Down mode operation.

The I_{off} feature ensures safe operation when the chip is powered down (VCC = 0 V). It automatically disables all outputs in a high-impedance state, preventing any damaging backflow current from flowing through the unpowered device. This allows the bus to remain active while protecting both the chip and connected components.

Enable ($\overline{OE}$) and Direction-control (DIRn)

The Output Enable ($\overline{OE}$) is a critical chip function that manages output states. When $\overline{OE}$ is high, all output ports enter a high-impedance state, when $\overline{OE}$ is low, the chip operates normally according to the DIRn pin's configuration.

Table 2. Device Function Table

V_{CCA}, V_{CCB}	Input $\overline{OE}$	Input DIR1	Input DIR2	Translator Function 1 to 4	Translator Function 5 to 8
0.8 V to 5.5 V	L	H	L	A => B	
0.8 V to 5.5 V	L	L	L	B => A	
0.8 V to 5.5 V	L	H	H	A => B	B => A
0.8 V to 5.5 V	L	L	H	B => A	A => B
0.8 V to 5.5 V	H	X	X	Hi-Z	
0V	X	X	X	Hi-Z	

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The T74V8T245 can be used for level-translation applications to interface devices or systems operating at different supply voltages. This device is an ideal solution for bidirectional data transmission scenarios. It is recommended to connect all unused I/O pins to ground, and no I/O pins should be left floating during direction switching. When the supply voltage exceeds 1.8V, the device can support a maximum data rate of up to 380 Mbps.

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer Handsets
- Industrial Automation

Typical Application

A typical application is shown in Figure 6. The T74V8T245 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The T74V8T245 device is ideal for use in applications where a push-pull driver is connected to the data I/Os.

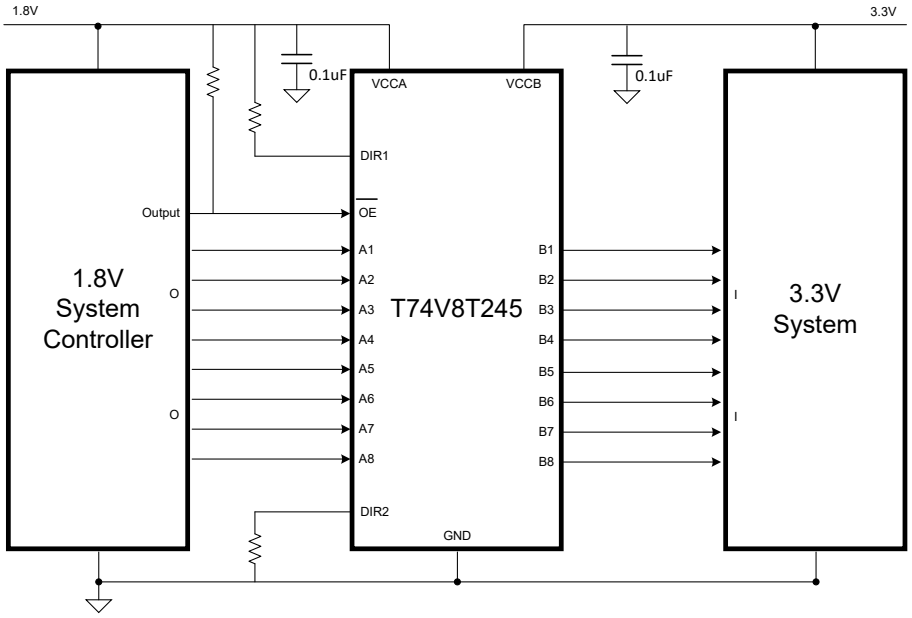


Figure 6. Typical Application Circuit

Layout

Layout Example

Reflections and matching are closely related to loop antenna theory but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in the width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they have to turn corners. Below are progressively better techniques for rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

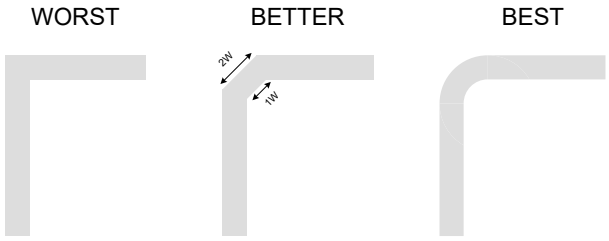


Figure 7. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

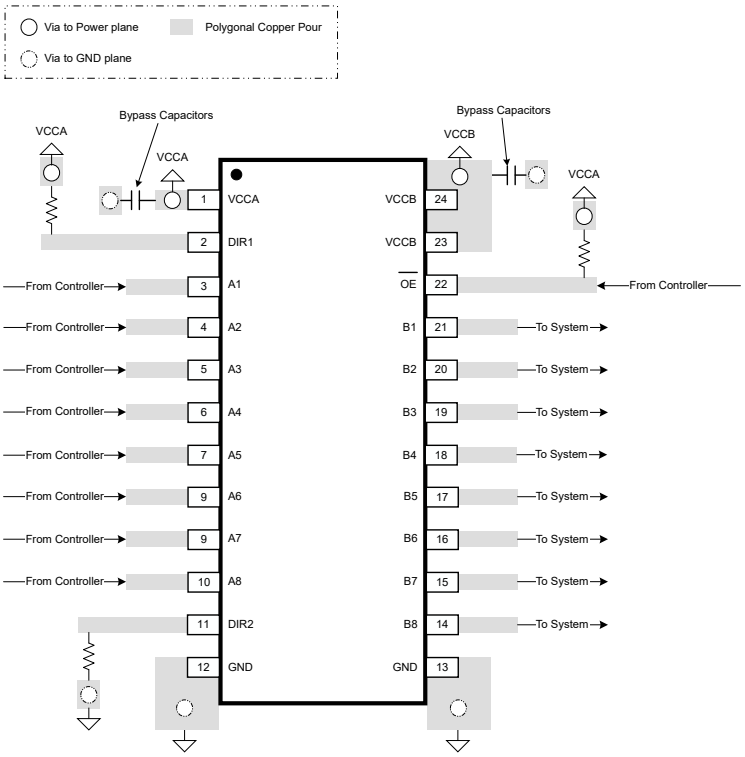
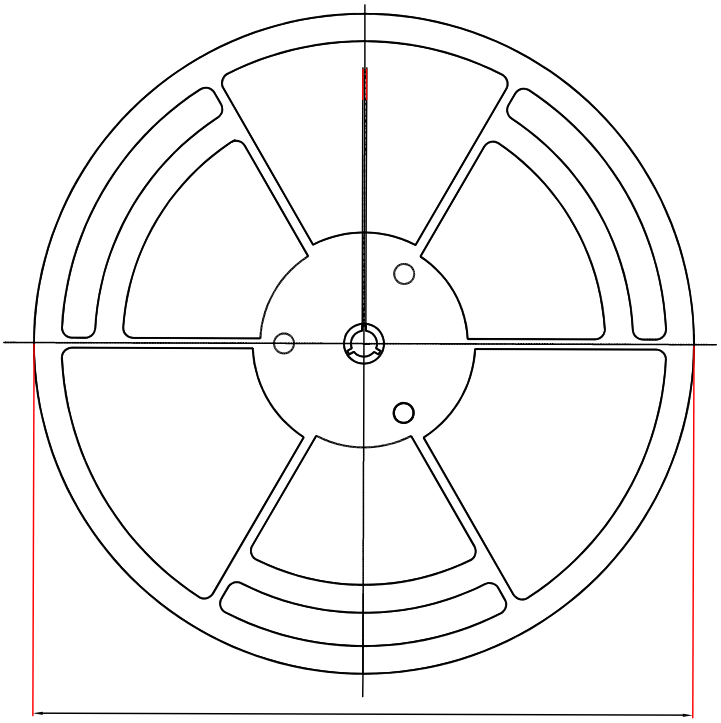
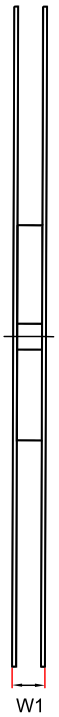
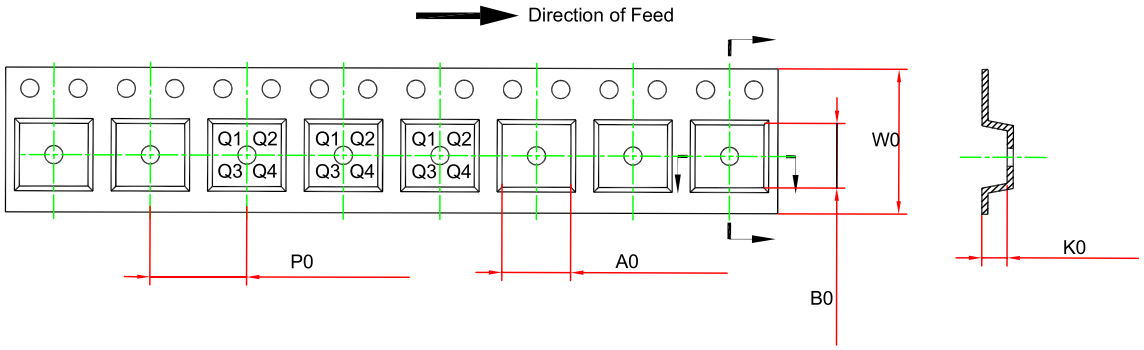


Figure 8. Layout Example

Tape and Reel Information





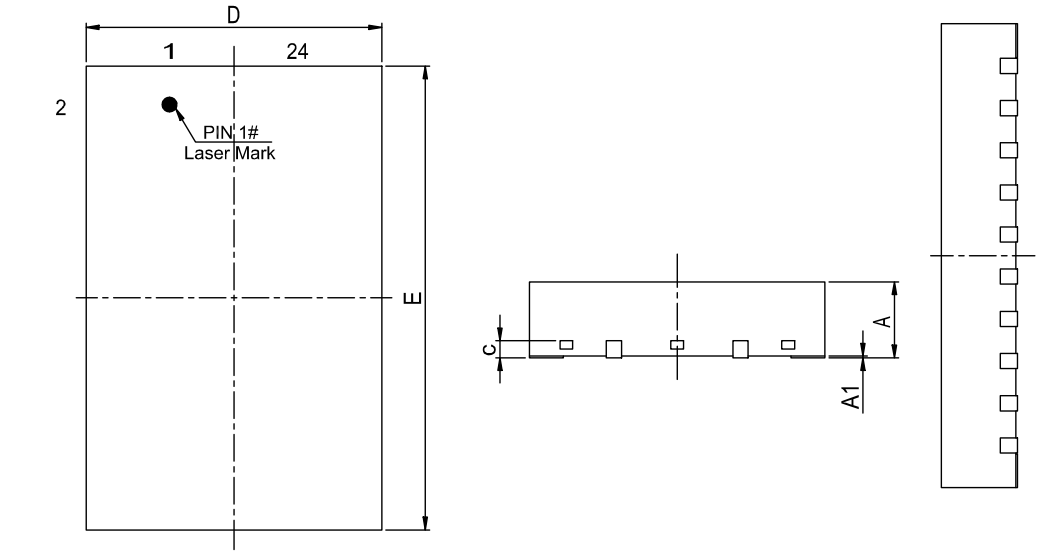


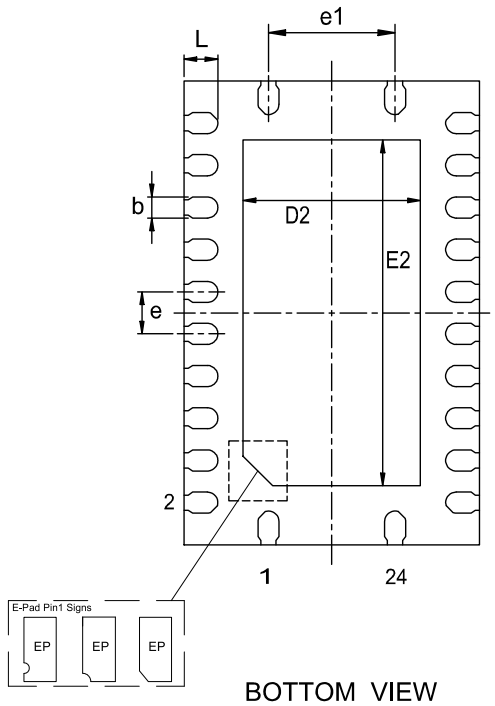
Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
T74V8T245-TS5R	TSSOP24	330	6.95	1.6	16	20.4	8.3	8.0	Q1
T74V8T245-QN7R	QFN5.5X2.5-24	330	3.8	1.05	12	17.6	5.8	8.0	Q1

Package Outline Dimensions

QFN5.5X3.5-24

Package Outline Dimensions QFX(QFN5.5X3.5-24-B)



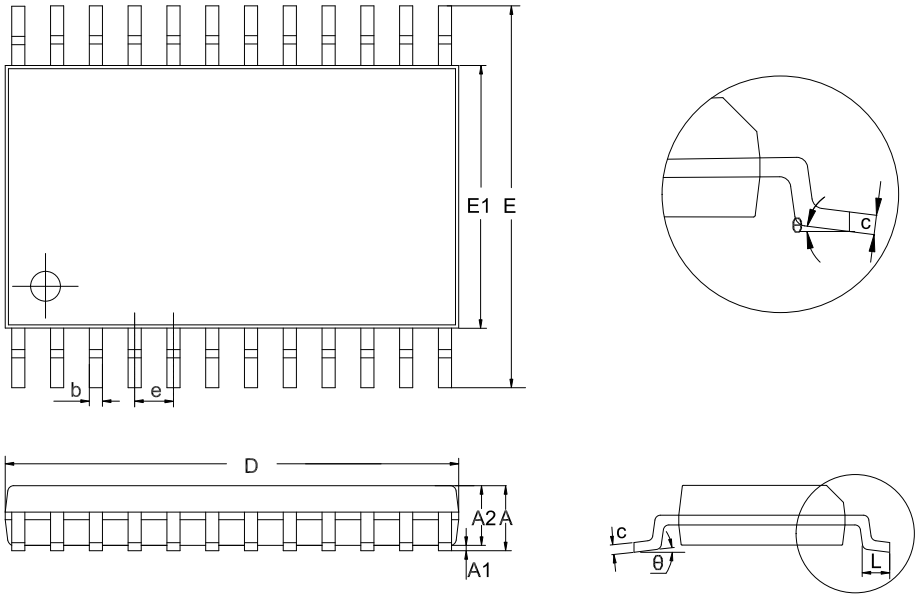


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
c	0.203REF		0.008REF	
D	3.400	3.600	0.134	0.142
E	5.400	5.600	0.213	0.220
e	0.500BSC		0.020BSC	
e1	1.500BSC		0.059BSC	
D2	2.000	2.200	0.079	0.087
E2	4.000	4.200	0.157	0.165
L	0.350	0.450	0.014	0.018

NOTES:
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad PIN1 signs may appear in the product

TSSOP24

Package Outline Dimensions TS5(TSSOP-24-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	7.700	7.900	0.303	0.311
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
T74V8T245-TS5R	−40 to 125°C	TSSOP24	8T245	MSL3	Tape and Reel,4000	Green
T74V8T245-QN7R	−40 to 125°C	QFN5.5X3.5-24	8T245	MSL3	Tape and Reel,3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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