4-bit Dual Supply Translating Transceiver, 3-state

Features

- 4-bit Dual Supply Translating Transceiver with Configurable Voltage Translation
- Fully Configurable Dual-rail Design Allows Each Port to Operate across the Full 0.8 V to 3.6 V Power Supply Range
- Support Partial Power-down Mode Operation
- No Power-up Sequence Required for V_{CCA} and V_{CCB}
- Max Data Rate (Push-Pull):
  - Translation from ≥ 1.8 V to 3.3 V: 380 Mbps
  - Translation from ≥ 1.1 V to 3.3 V: 200 Mbps
  - Translation from ≥ 1.1 V to 2.5 V: 200 Mbps
  - Translation from ≥ 1.1 V to 1.8 V: 200 Mbps
  - Translation from ≥ 1.1 V to 1.5 V: 150 Mbps
  - Translation from ≥ 1.1 V to 1.2 V: 150 Mbps
- ESD Protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 Class 3B Exceeds 8000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 Class C3 Exceeds 1000 V

Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer Handsets
- Industrial Automation

Description

The T74V4T774 device is a 4-bit level shifter, with an enable ($\overline{OE}$) input and can work within the V_{CCA} range from 0.8 V to 3.6 V and the V_{CCB} range from 0.8 V to 3.6 V.

The T74V4T774 enables asynchronous communication between data buses. Depending on the logic level of the direction control (DIRn) input, this device transmits data either from the A bus to the B bus or from the B bus to the A bus. The output enable ($\overline{OE}$) pin can be used to disable the outputs, effectively isolating the buses.

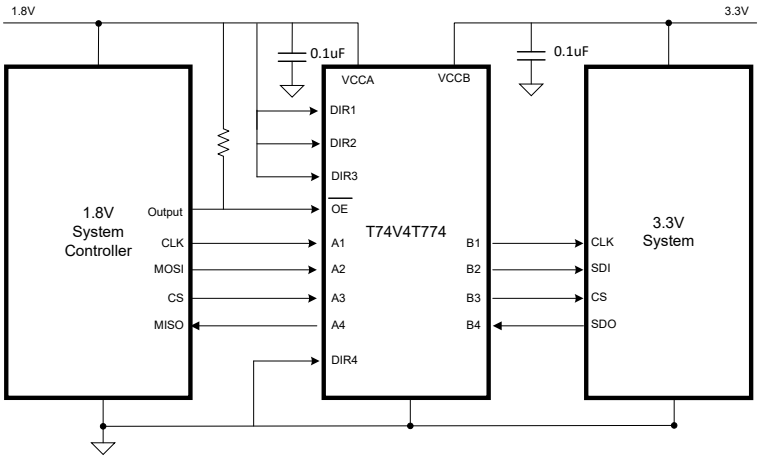
The enable control pin ($\overline{OE}$) and direction control pin (DIRn) of the T74V4T774 are powered by V_{CCA}.

The T74V4T774 fully complies with the specifications for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging backflow current through the device when it is powered down.

For high-impedance operation during power-up/power-down conditions, the $\overline{OE}$ (output enable) pin must be tied to V_{CCA} via a pull-up resistor. The minimum resistor value depends on the sink current capability of the driver.

The T74V4T774 is available in the QFN1.8X2.6-16 package and is characterized from −40°C to +125°C.

Typical Application



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Revision History

Date	Revision	Notes
2025-08-02	Rev.P.0	Initial version
2026-01-21	Rev.A.0	Released version

Pin Configuration and Functions

T74V4T774-QN6R
QFN1.8X2.6-16
Top View

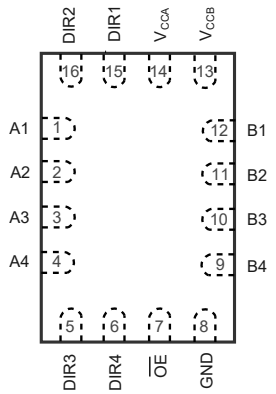


Table 1. Pin Functions: T74V4T774-QN6R

Pin		I/O	Description
No.	Name		
1	A1	I/O	Input/output A1. Referenced to V_{CCA}
2	A2	I/O	Input/output A2. Referenced to V_{CCA}
3	A3	I/O	Input/output A3. Referenced to V_{CCA}
4	A4	I/O	Input/output A4. Referenced to V_{CCA}
5	DIR3	I	Direction-control Input for '3' Ports. Referenced to V_{CCA}
6	DIR4	I	Direction-control Input for '4' Ports. Referenced to V_{CCA}
7	$\overline{OE}$	I	Active-low Enable Input. Referenced to V_{CCA}
8	GND	P	Supply Ground
9	B4	I/O	Input/output B4. Referenced to V_{CCB}
10	B3	I/O	Input/output B3. Referenced to V_{CCB}
11	B2	I/O	Input/output B2. Referenced to V_{CCB}
12	B1	I/O	Input/output B1. Referenced to V_{CCB}
13	V_{CCB}	P	Side-B Supply Voltage
14	V_{CCA}	P	Side-A Supply Voltage
15	DIR1	I	Direction-control Input for '1' Ports. Referenced to V_{CCA}
16	DIR2	I	Direction-control Input for '2' Ports. Referenced to V_{CCA}

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CCA}	DC Reference Voltage Range, Side-A	−0.5	4.6	V
V_{CCB}	DC Reference Voltage Range, Side-B	−0.5	4.6	V
I_{IK}	Input Clamp Current, V_I < 0	−50		mA
V_I	Input Voltage Range, Side-A	−0.5	4.6	V
	Input Voltage Range, Side-B	−0.5	4.6	V
I_{OK}	Output Clamp Current, $V_{I/O}$ < 0	−50		mA
V_O	Output Voltage, Active mode	−0.5	V_{cco} + 0.5	V
	Output Voltage, Suspend or 3-state Mode	−0.5	4.6	V
I_O	Continuous Output Current	−50	50	mA
I_{CC}	V_{CCA} or V_{CCB} Pin		100	mA
I_{GND}	Per GND Pin	−100		mA
T_{STG}	Storage Temperature Range	−65	150	°C
P_{tot}	Total Power Dissipation		250	mW

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 class 3B (1)	±8	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 class C3 (2)	±1	kV
LU	Latch Up	LU, per JESD78, All Pins	±100	mA

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Conditions	Min	Typ	Max	Unit
V_{CCA}	Supply Voltage Side-A		0.8		3.6	V
V_{CCB}	Supply Voltage Side-B		0.8		3.6	V
V_I	Input Voltage		0		3.6	V
V_O	Output Voltage	Active Mode	0		V_{CCO}	V
		Suspend or 3-state Mode	0		3.6	V

Parameter		Conditions	Min	Typ	Max	Unit
T_{amb}	Ambient Temperature		-40		+125	°C
Δt/ΔV	Input Transition Rise and Fall Rate	V_{CCI} = 0.8 V to 3.6 V			5	ns/V

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
QFN1.8X2.6-16	138.7	65.1	°C/W

Electrical Characteristics

All test conditions: V_{CCA} = 0.8 V to 3.6 V, V_{CCB} = 0.8 V to 3.6 V, T_A = −40°C to +125°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level Output Voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 uA, V_{CCA} = 0.8 V to 3.6 V, V_{CCB} = 0.8 V to 3.6 V			0.1	V
		I_O = 3 mA, V_{CCA} = 1.1 V, V_{CCB} = 1.1 V			0.25	V
		I_O = 6 mA, V_{CCA} = 1.4 V, V_{CCB} = 1.4 V			0.35	V
		I_O = 8 mA, V_{CCA} = 1.65 V, V_{CCB} = 1.65 V			0.45	V
		I_O = 9 mA, V_{CCA} = 2.3 V, V_{CCB} = 2.3 V			0.55	V
		I_O = 12 mA, V_{CCA}= 3 V, V_{CCB} = 3 V			0.7	V
V_{OH}	HIGH-level Output Voltage	V_I = V_{IH} or V_{IL}				
		I_O = −100 uA, V_{CCA} = 0.8 V, V_{CCB} = 0.8 V	0.7			V
		I_O = −100 uA, V_{CCA} = 3.6 V, V_{CCB} = 3.6 V	3.5			V
		I_O = −3 mA, V_{CCA} = 1.1 V, V_{CCB} = 1.1 V	0.85			V
		I_O = −6 mA, V_{CCA} = 1.4 V, V_{CCB} = 1.4 V	1.05			V
		I_O = −8 mA, V_{CCA} = 1.65 V, V_{CCB} = 1.65 V	1.2			V
		I_O = −9 mA, V_{CCA} = 2.3 V, V_{CCB} = 2.3 V	1.75			V
		I_O = −12 mA, V_{CCA} = 3 V, V_{CCB} = 3 V	2.3			V
V_{IL}	LOW-level Input Voltage (Data Input)	V_{CCI} = 0.8 V			0.24	V
		V_{CCI} = 1.1 V			0.385	V
		V_{CCI} = 1.95 V			0.683	V
		V_{CCI} = 2.3 V to 2.7 V			0.7	V
		V_{CCI} = 3.0 V to 3.6 V			0.8	V
	LOW-level Input Voltage (DIRn, OE Input)	V_{CCA} = 0.8 V			0.24	V
		V_{CCA} = 1.1 V			0.385	V
		V_{CCA} = 1.95 V			0.683	V
		V_{CCA} = 2.3 V to 2.7V			0.7	V
		V_{CCA} = 3.0 V to 3.6 V			0.8	V
V_{IH}	HIGH-level Input Voltage (Data Input)	V_{CCI} = 0.8 V	0.56			V
		V_{CCI} = 1.1 V	0.715			V
		V_{CCI} = 1.95 V	1.268			V
		V_{CCI} = 2.3 V to 2.7 V	1.6			V
		V_{CCI} = 3.0 V to 3.6 V	2.0			V
	HIGH-level Input Voltage (DIRn, OE Input)	V_{CCA} = 0.8 V	0.56			V
		V_{CCA} = 1.1 V	0.715			V
		V_{CCA} = 1.95 V	1.268			V

Parameter		Conditions	Min	Typ	Max	Unit
		V_{CCA} = 2.3 V to 2.7 V	1.6			V
		V_{CCA} = 3.0 V to 3.6 V	2.0			V
I_I	Input Leakage Current	DIRn, OE input, V_I = 0 V or 3.6 V, V_{CCA}= 0.8 V to 3.6 V, V_{CCB}= 0.8 V to 3.6 V	−5		5	uA
I_{OZ}	OFF State Output Current	A or B port, V_O = 0 V or V_{CCO}	−30		30	uA
		A port, V_O = 0 V or V_{CCO}, V_{CCA} = 3.6 V, V_{CCB} = 0 V	−30		30	uA
		B port, V_O = 0 V or V_{CCO}, V_{CCA} = 0 V, V_{CCB} = 3.6 V	−30		30	uA
I_{OFF}	Power-off Leakage Current	A port V_I or V_O = 0 V to 3.6 V, V_{CCA} = 0.8 V to 3.6 V, V_{CCB} = 0.8 V to 3.6 V	−30		30	uA
		B port V_I or V_O = 0 V to 3.6 V, V_{CCA} = 0.8 V to 3.6 V, V_{CCB} = 0.8 V to 3.6 V	−30		30	uA
I_{CCA}	Supply Current, Side-A	A port V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCA} = 0.8 V to 3.6 V, V_{CCB} = 0.8 V to 3.6 V			100	uA
		A port V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCA} = 1.1 V to 3.6 V, V_{CCB} = 1.1 V to 3.6 V			100	uA
		A port V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCA} = 3.6 V, V_{CCB} = 0 V			100	uA
		A port V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCA} = 0 V, V_{CCB} = 3.6 V	−100			uA
I_{CCB}	Supply Current, Side-B	B port V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCA} = 0.8 V to 3.6 V, V_{CCB} = 0.8 V to 3.6 V			100	uA
		B port V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCA} = 1.1 V to 3.6 V, V_{CCB} = 1.1 V to 3.6 V			100	uA
		B port V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCA} = 3.6 V, V_{CCB} = 0 V	−100			uA
		B port V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCA} = 0 V, V_{CCB}= 3.6 V			100	uA
$I_{CCA}+I_{CCB}$	Combined Supply Current	A plus B port, I_O = 0 A, V_I = 0 V or V_{CCI}, V_{CCA} = 0.8 V to 3.6 V, V_{CCB} = 0.8 V to 3.6 V			200	uA
		A plus B port, I_O = 0 A, V_I = 0 V or V_{CCI}, V_{CCA} = 1.1 V to 3.6 V, V_{CCB} = 1.1 V to 3.6 V			200	uA
ΔI_{CC}	Additional Supply Current	V_I = 3.0 V, V_{CCA} = V_{CCB} = 3.3 V			650	uA
C_I (1)	Input Capacitance	DIRn, OE input, V_I = 0 V or 3.3 V, V_{CCA} = 3.3 V, V_{CCB} = 3.3 V			6	pF
C_{IO} (1)	Input/Output Capacitance	A and B port, V_O = 3.3 V or 0 V, V_{CCA} = 3.3 V, V_{CCB} = 3.3 V			10	pF

(1) Test data based on bench tests and design simulation, not test in production.

AC Timing Requirements — VCCA = 0.8 V

All test conditions: T_A = 25°C, the data is based on bench test and design simulation, not test in production, unless otherwise noted.

t_{en} includes t_{PZL} and t_{PHL}, t_{dis} includes t_{PLZ} and t_{PHZ}.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
t_{PLH} , t_{PHL}	Propagation Delay	A-to-B push-pull driving	0.8 V		14.4		ns
			1.2 V		7.0		ns
			1.5 V		6.2		ns
			1.8 V		6.0		ns
			2.5 V		5.9		ns
			3.3 V		6.0		ns
t_{PLH}, t_{PHL}	Propagation Delay	B-to-A push-pull driving	0.8 V		14.4		ns
			1.2 V		12.4		ns
			1.5 V		12.1		ns
			1.8 V		11.9		ns
			2.5 V		11.8		ns
			3.3 V		11.8		ns
t_{en}	Enable Time	$\overline{OE}$-to-A	0.8 V		21.9		ns
			1.2 V		21.9		ns
			1.5 V		21.9		ns
			1.8 V		21.9		ns
			2.5 V		21.9		ns
			3.3 V		21.9		ns
t_{en}	Enable Time	$\overline{OE}$-to-B	0.8 V		22.2		ns
			1.2 V		11.1		ns
			1.5 V		9.8		ns
			1.8 V		9.4		ns
			2.5 V		9.4		ns
			3.3 V		9.6		ns
t_{dis}	Disable Time	$\overline{OE}$-to-A	0.8 V		16.2		ns
			1.2 V		16.2		ns
			1.5 V		16.2		ns
			1.8 V		16.2		ns
			2.5 V		16.2		ns
			3.3 V		16.2		ns
t_{dis}	Disable Time	$\overline{OE}$-to-B	0.8 V		17.6		ns
			1.2 V		10.0		ns

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
			1.5 V		9.0		ns
			1.8 V		9.1		ns
			2.5 V		8.7		ns
			3.3 V		9.3		ns
C_{PD}	Power Dissipation Capacitance	A port, A-to-B, output enable	0.8 V		0.35		pF
		A port, A-to-B, output disable			0.35		pF
		A port, B-to-A, output enable			13.7		pF
		A port, B-to-A, output disable			0.35		pF
		B port, A-to-B, output enable			13.7		pF
		B port, A-to-B, output disable			0.35		pF
		B port, B-to-A, output enable			0.35		pF
		B port, B-to-A, output disable			0.35		pF

AC Timing Requirements — VCCA = 1.2 V

All test conditions: T_A = −40°C to +125°C, V_{CCA} = 1.2 V ± 0.1 V, the data is based on bench test and design simulation, not test in production, unless otherwise noted.

t_{en} includes t_{PZL} and t_{PHL}, t_{dis} includes t_{PLZ} and t_{PHZ}.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
t_{PLH} , t_{PHL}	Propagation Delay	A-to-B push-pull driving	0.8 V (1)		7.0		
			1.2 V ± 0.1 V	0.5		9.5	ns
			1.5 V ± 0.1 V	0.5		7.4	ns
			1.8 V ± 0.15 V	0.5		6.4	ns
			2.5 V ± 0.2 V	0.5		5.4	ns
			3.3 V ± 0.3 V	0.5		5.3	ns
		B-to-A push-pull driving	0.8 V (1)		12.4		
			1.2 V ± 0.1 V	0.5		9.9	ns
			1.5 V ± 0.1 V	0.5		9.4	ns
			1.8 V ± 0.15 V	0.5		9.2	ns
			2.5 V ± 0.2 V	0.5		8.8	ns
			3.3 V ± 0.3 V	0.5		8.6	ns
t_{en}	Enable Time	$\overline{OE}$-to-A	0.8 V (1)		21.9		
			1.2 V ± 0.1 V	1.1		15.9	ns
			1.5 V ± 0.1 V	1.1		15.9	ns
			1.8 V ± 0.15 V	1.1		15.9	ns
			2.5 V ± 0.2 V	1.1		15.9	ns
			3.3 V ± 0.3 V	1.1		15.9	ns
		$\overline{OE}$-to-B	0.8 V (1)		11.1		
			1.2 V ± 0.1 V	1.1		15.7	ns
			1.5 V ± 0.1 V	1.1		11.5	ns
			1.8 V ± 0.15 V	1.1		9.9	ns
			2.5 V ± 0.2 V	1.0		8.5	ns
			3.3 V ± 0.3 V	1.0		8.1	ns
t_{dis}	Disable Time	$\overline{OE}$-to-A	0.8 V (1)		16.2		
			1.2 V ± 0.1 V	0.5		13.0	ns
			1.5 V ± 0.1 V	0.5		13.0	ns
			1.8 V ± 0.15 V	0.5		13.0	ns
			2.5 V ± 0.2 V	0.5		13.0	ns
			3.3 V ± 0.3 V	0.5		13.0	ns
		$\overline{OE}$-to-B	0.8 V (1)		10.0		
			1.2 V ± 0.1 V	0.5		13.6	ns

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
			1.5 V ± 0.1 V	0.5		10.5	ns
			1.8 V ± 0.15 V	0.5		10.4	ns
			2.5 V ± 0.2 V	0.5		8.8	ns
			3.3 V ± 0.3 V	0.5		9.8	ns
C_{PD}(1)	power dissipation capacitance	A port, A-to-B, output enable	1.2 V		0.35		pF
		A port, A-to-B, output disable			0.35		pF
		A port, B-to-A, output enable			13.8		pF
		A port, B-to-A, output disable			0.35		pF
		B port, A-to-B, output enable			13.8		pF
		B port, A-to-B, output disable			0.35		pF
		B port, B-to-A, output enable			0.35		pF
		B port, B-to-A, output disable			0.35		pF

(1) Tested V_{CCA} = 1.2 V and T_A = 25°C.

AC Timing Requirements — VCCA = 1.5 V

All test conditions: T_A = −40°C to +125°C, V_{CCA} = 1.5 V ± 0.1 V, the data is based on bench test and design simulation, not test in production, unless otherwise noted.

t_{en} includes t_{PZL} and t_{PHL}, t_{dis} includes t_{PLZ} and t_{PHZ}.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
t_{PLH} , t_{PHL}	Propagation Delay	A-to-B push-pull driving	0.8 V (1)		6.2		
			1.2 V ± 0.1 V	0.5		9.4	ns
			1.5 V ± 0.1 V	0.5		6.2	ns
			1.8 V ± 0.15 V	0.5		5.2	ns
			2.5 V ± 0.2 V	0.5		4.9	ns
			3.3 V ± 0.3 V	0.5		4.6	ns
		B-to-A push-pull driving	0.8 V (1)		12.1		
			1.2 V ± 0.1 V	0.5		7.4	ns
			1.5 V ± 0.1 V	0.5		6.2	ns
			1.8 V ± 0.15 V	0.5		5.9	ns
			2.5 V ± 0.2 V	0.5		5.8	ns
			3.3 V ± 0.3 V	0.5		5.5	ns
t_{en}	Enable Time	$\overline{OE}$-to-A	0.8 V (2)		21.9		
			1.2 V ± 0.1 V	1.1		9.6	ns
			1.5 V ± 0.1 V	1.1		9.6	ns
			1.8 V ± 0.15 V	1.1		9.6	ns
			2.5 V ± 0.2 V	1.1		9.6	ns
			3.3 V ± 0.3 V	1.1		9.6	ns
		$\overline{OE}$-to-B	0.8 V (1)		9.8		
			1.2 V ± 0.1 V	1.1		14.1	ns
			1.5 V ± 0.1 V	1.1		9.0	ns
			1.8 V ± 0.15 V	1.1		7.9	ns
			2.5 V ± 0.2 V	1.0		6.2	ns
			3.3 V ± 0.3 V	1.0		5.8	ns
t_{dis}	Disable Time	$\overline{OE}$-to-A	0.8 V (1)		16.2		
			1.2 V ± 0.1 V	0.5		9.5	ns
			1.5 V ± 0.1 V	0.5		9.5	ns
			1.8 V ± 0.15 V	0.5		9.5	ns
			2.5 V ± 0.2 V	0.5		9.5	ns
			3.3 V ± 0.3 V	0.5		9.5	ns
		$\overline{OE}$-to-B	0.8 V (1)		9.0		
			1.2 V ± 0.1 V	0.5		12.4	ns

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
			1.5 V ± 0.1 V	0.5		9.3	ns
			1.8 V ± 0.15 V	0.5		8.4	ns
			2.5 V ± 0.2 V	0.5		8.0	ns
			3.3 V ± 0.3 V	0.5		8.6	ns
C_{PD}(1)	Power Dissipation Capacitance	A port, A-to-B, output enable	1.5 V		0.35		pF
		A port, A-to-B, output disable			0.35		pF
		A port, B-to-A, output enable			14		pF
		A port, B-to-A, output disable			0.35		pF
		B port, A-to-B, output enable			14		pF
		B port, A-to-B, output disable			0.35		pF
		B port, B-to-A, output enable			0.35		pF
		B port, B-to-A, output disable			0.35		pF

(1) Tested V_{CCA} = 1.5 V and T_A = 25°C.

AC Timing Requirements — VCCA = 1.8 V

All test conditions: T_A = −40°C to +125°C, V_{CCA} = 1.8 V ± 0.15 V, the data is based on bench test and design simulation, not test in production, unless otherwise noted.

t_{en} includes t_{PZL} and t_{PHL}, t_{dis} includes t_{PLZ} and t_{PHZ}.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
t_{PLH} , t_{PHL}	Propagation Delay	A-to-B push-pull driving	0.8 V (1)		6.0		
			1.2 V ± 0.1 V	0.5		9.2	ns
			1.5 V ± 0.1 V	0.5		5.9	ns
			1.8 V ± 0.15 V	0.5		5.0	ns
			2.5 V ± 0.2 V	0.5		4.2	ns
			3.3 V ± 0.3 V	0.5		3.9	ns
		B-to-A push-pull driving	0.8 V (1)		11.9		
			1.2 V ± 0.1 V	0.5		6.4	ns
			1.5 V ± 0.1 V	0.5		5.2	ns
			1.8 V ± 0.15 V	0.5		5.0	ns
			2.5 V ± 0.2 V	0.5		4.8	ns
			3.3 V ± 0.3 V	0.5		4.6	ns
t_{en}	Enable Time	$\overline{OE}$-to-A	0.8 V (1)		21.9		
			1.2 V ± 0.1 V	1.0		7.5	ns
			1.5 V ± 0.1 V	1.0		7.5	ns
			1.8 V ± 0.15 V	1.0		7.5	ns
			2.5 V ± 0.2 V	1.0		7.5	ns
			3.3 V ± 0.3 V	1.0		7.5	ns
		$\overline{OE}$-to-B	0.8 V (1)		9.4		
			1.2 V ± 0.1 V	1.1		13.7	ns
			1.5 V ± 0.1 V	1.1		9.1	ns
			1.8 V ± 0.15 V	1.0		7.4	ns
			2.5 V ± 0.2 V	0.5		5.7	ns
			3.3 V ± 0.3 V	0.5		5.0	ns
t_{dis}	Disable Time	$\overline{OE}$-to-A	0.8 V (1)		16.2		
			1.2 V ± 0.1 V	0.5		7.9	ns
			1.5 V ± 0.1 V	0.5		7.9	ns
			1.8 V ± 0.15 V	0.5		7.9	ns
			2.5 V ± 0.2 V	0.5		7.9	ns
			3.3 V ± 0.3 V	0.5		7.9	ns
		$\overline{OE}$-to-B	0.8 V (1)		9.1		
			1.2 V ± 0.1 V	0.5		12.0	ns

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
			1.5 V ± 0.1 V	0.5		8.6	ns
			1.8 V ± 0.15 V	0.5		7.6	ns
			2.5 V ± 0.2 V	0.5		6.6	ns
			3.3 V ± 0.3 V	0.5		6.4	ns
C_{PD}(1)	Power Dissipation Capacitance	A port, A-to-B, output enable	1.8 V		0.37		pF
		A port, A-to-B, output disable			0.37		pF
		A port, B-to-A, output enable			14.3		pF
		A port, B-to-A, output disable			0.37		pF
		B port, A-to-B, output enable			14.3		pF
		B port, A-to-B, output disable			0.37		pF
		B port, B-to-A, output enable			0.37		pF
		B port, B-to-A, output disable			0.37		pF

(1) Tested V_{CCA} = 1.8 V and T_A = 25°C.

AC Timing Requirements — VCCA = 2.5 V

All test conditions: T_A = −40°C to +125°C, V_{CCA} = 2.5 V ± 0.2 V, the data is based on bench test and design simulation, not test in production, unless otherwise noted.

t_{en} includes t_{PZL} and t_{PHL}, t_{dis} includes t_{PLZ} and t_{PHZ}.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
t_{PLH} , t_{PHL}	Propagation Delay	A-to-B push-pull driving	0.8 V (1)		5.9		
			1.2 V ± 0.1 V	0.5		8.8	ns
			1.5 V ± 0.1 V	0.5		5.8	ns
			1.8 V ± 0.15 V	0.5		4.8	ns
			2.5 V ± 0.2 V	0.5		3.7	ns
			3.3 V ± 0.3 V	0.5		3.2	ns
		B-to-A push-pull driving	0.8 V (1)		11.8		
			1.2 V ± 0.1 V	0.5		5.4	ns
			1.5 V ± 0.1 V	0.5		4.9	ns
			1.8 V ± 0.15 V	0.5		4.2	ns
			2.5 V ± 0.2 V	0.5		3.7	ns
			3.3 V ± 0.3 V	0.5		3.5	ns
t_{en}	Enable Time	$\overline{OE}$-to-A	0.8 V (1)		21.9		
			1.2 V ± 0.1 V	0.5		5.3	ns
			1.5 V ± 0.1 V	0.5		5.3	ns
			1.8 V ± 0.15 V	0.5		5.3	ns
			2.5 V ± 0.2 V	0.5		5.3	ns
			3.3 V ± 0.3 V	0.5		5.3	ns
		$\overline{OE}$-to-B	0.8 V (1)		9.4		
			1.2 V ± 0.1 V	1.1		13.1	ns
			1.5 V ± 0.1 V	1.1		8.7	ns
			1.8 V ± 0.15 V	0.5		7.1	ns
			2.5 V ± 0.2 V	0.5		5.1	ns
			3.3 V ± 0.3 V	0.5		4.4	ns
t_{dis}	Disable Time	$\overline{OE}$-to-A	0.8 V (1)		16.2		
			1.2 V ± 0.1 V	0.5		5.7	ns
			1.5 V ± 0.1 V	0.5		5.7	ns
			1.8 V ± 0.15 V	0.5		5.7	ns
			2.5 V ± 0.2 V	0.5		5.7	ns
			3.3 V ± 0.3 V	0.5		5.7	ns
		$\overline{OE}$-to-B	0.8 V (1)		8.7		
			1.2 V ± 0.1 V	0.5		11.5	ns

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
			1.5 V ± 0.1 V	0.5		7.9	ns
			1.8 V ± 0.15 V	0.5		7.0	ns
			2.5 V ± 0.2 V	0.5		5.7	ns
			3.3 V ± 0.3 V	0.5		5.8	ns
C_{PD}	Power Dissipation Capacitance	A port, A-to-B, output enable	2.5 V		0.37		pF
		A port, A-to-B, output disable			0.37		pF
		A port, B-to-A, output enable			14.5		pF
		A port, B-to-A, output disable			0.37		pF
		B port, A-to-B, output enable			14.5		pF
		B port, A-to-B, output disable			0.37		pF
		B port, B-to-A, output enable			0.37		pF
		B port, B-to-A, output disable			0.37		pF

(1) Tested V_{CCA} = 2.5 V and T_A = 25°C.

AC Timing Requirements — VCCA = 3.3 V

All test conditions: T_A = −40°C to +125°C, V_{CCA} = 3.3 V ± 0.3 V, the data is based on bench test and design simulation, not test in production, unless otherwise noted.

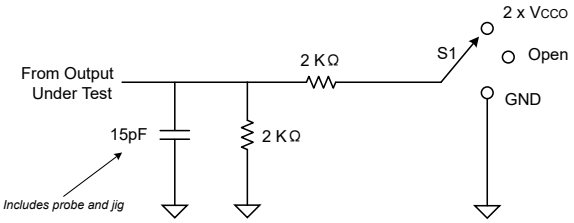
t_{en} includes t_{PZL} and t_{PHL}, t_{dis} includes t_{PLZ} and t_{PHZ}.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
t_{PLH} , t_{PHL}	Propagation Delay	A-to-B push-pull driving	0.8 V (1)		7.0		
			1.2 V ± 0.1 V	0.5		8.6	ns
			1.5 V ± 0.1 V	0.5		5.5	ns
			1.8 V ± 0.15 V	0.5		4.6	ns
			2.5 V ± 0.2 V	0.5		3.5	ns
			3.3 V ± 0.3 V	0.5		3.0	ns
		B-to-A push-pull driving	0.8 V (1)		12.4		
			1.2 V ± 0.1 V	0.5		5.3	ns
			1.5 V ± 0.1 V	0.5		4.6	ns
			1.8 V ± 0.15 V	0.5		3.9	ns
			2.5 V ± 0.2 V	0.5		3.2	ns
			3.3 V ± 0.3 V	0.5		3.0	ns
t_{en}	Enable Time	$\overline{OE}$-to-A	0.8 V (1)		21.9		
			1.2 V ± 0.1 V	0.5		4.4	ns
			1.5 V ± 0.1 V	0.5		4.4	ns
			1.8 V ± 0.15 V	0.5		4.4	ns
			2.5 V ± 0.2 V	0.5		4.4	ns
			3.3 V ± 0.3 V	0.5		4.4	ns
		$\overline{OE}$-to-B	0.8 V (1)		11.1		
			1.2 V ± 0.1 V	1.1		12.9	ns
			1.5 V ± 0.1 V	1.1		8.6	ns
			1.8 V ± 0.15 V	0.5		6.9	ns
			2.5 V ± 0.2 V	0.5		5.0	ns
			3.3 V ± 0.3 V	1.0		4.3	ns
t_{dis}	Disable Time	$\overline{OE}$-to-A	0.8 V (1)		16.2		
			1.2 V ± 0.1 V	0.5		5.4	ns
			1.5 V ± 0.1 V	0.5		5.4	ns
			1.8 V ± 0.15 V	0.5		5.4	ns
			2.5 V ± 0.2 V	0.5		5.4	ns
			3.3 V ± 0.3 V	0.5		5.4	ns
		$\overline{OE}$-to-B	0.8 V (1)		10.0		
			1.2 V ± 0.1 V	0.5		11.2	ns

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
			1.5 V ± 0.1 V	0.5		8.6	ns
			1.8 V ± 0.15 V	0.5		6.9	ns
			2.5 V ± 0.2 V	0.5		5.0	ns
			3.3 V ± 0.3 V	0.5		4.3	ns
C_{PD}(1)	Power Dissipation Capacitance	A port, A-to-B, output enable	1.2 V		0.58		pF
		A port, A-to-B, output disable			0.58		pF
		A port, B-to-A, output enable			15.6		pF
		A port, B-to-A, output disable			0.58		pF
		B port, A-to-B, output enable			15.6		pF
		B port, A-to-B, output disable			0.58		pF
		B port, B-to-A, output enable			0.58		pF
		B port, B-to-A, output disable			0.58		pF

(1) Tested V_{CCA} = 3.3 V and T_A = 25°C.

Parameter Measurement Waveforms



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CCO}
t_{PHZ}/t_{PZH}	GND

Figure 1. Timing Measurement Load Circuit

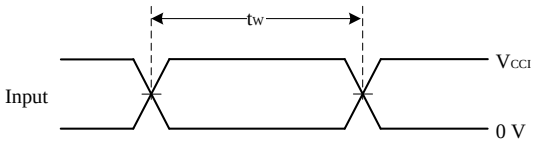


Figure 2. Pulse Duration

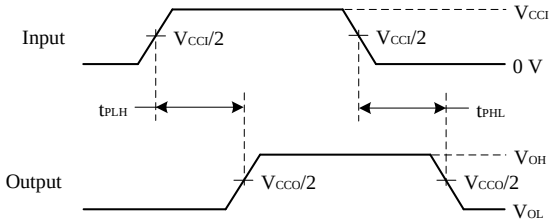
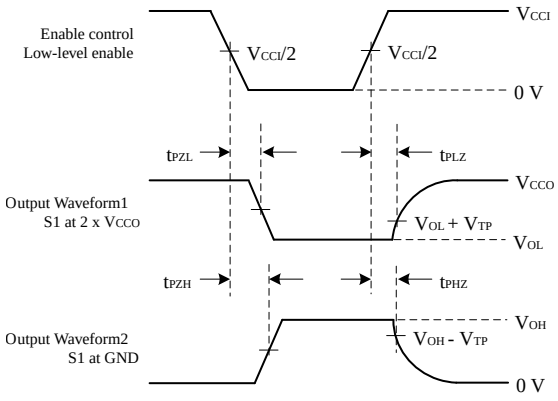


Figure 3. Propagation Delay Times



V_{CCO}	V_{TP}
0.8 V	0.1 V
1.2 V	0.1 V
1.5 V ± 0.1 V	0.1 V
1.8 V ± 0.15 V	0.15 V
2.5 V ± 0.2 V	0.15 V
3.3 V ± 0.3 V	0.3 V

Figure 4. Enable and Disable Times

Note:

t_{plz} and t_{phz} are the same as t_{dis}.

t_{pzl} and t_{pzh} are the same as t_{en}.

V_{CCI} is V_{CC} associated with the input port.

V_{CCO} is V_{CC} associated with the output port.

t_{PLH} and t_{PHL} are the same as t_{pd}.

Detailed Description

Overview

The T74V4T774 device is a 4-bit level shifter, with an enable ($\overline{OE}$) input and can work within the V_{CCA} range from 0.8 V to 3.6 V and the V_{CCB} range from 0.8 V to 3.6 V. V_{CCA} powers the A-port and control pins (DIRn and $\overline{OE}$), while V_{CCB} supplies the B-port. The A-port supports I/O voltage levels from 0.8 V to 3.6 V, and the B-port also accommodates I/O voltages ranging from 0.8 V to 3.6 V. When $\overline{OE}$ is driven low, a high level on DIRn enables data transmission from A to B, and a low level on DIR facilitates data transfer from B to A. When $\overline{OE}$ is set high, both A and B ports enter a high-impedance state.

Functional Block Diagram

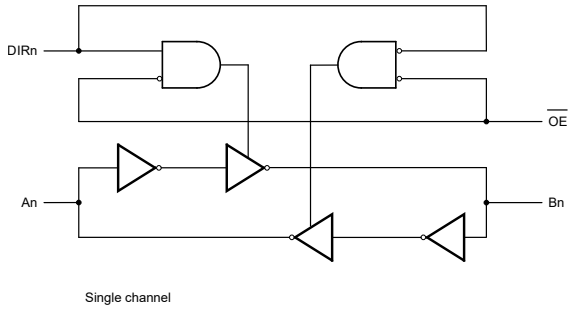


Figure 5. Functional Block Diagram

Feature Description

Enable ($\overline{OE}$) and Direction-control (DIRn)

The Output Enable ($\overline{OE}$) is a critical chip function that manages output states. When $\overline{OE}$ is high, all output ports enter a high-impedance state, when $\overline{OE}$ is low, the chip operates normally according to the DIRn pin's configuration.

The T74V4T774 features a directional control function, where the state of the control pin (DIRn) determines the data transmission path between Port A and Port B. When DIRn is set to a high logic level, data flows unidirectionally from Port A to Port B. Conversely, when DIRn is driven low, the data direction reverses, transmitting from Port B to Port A. To ensure reliable operation during DIRn state transitions, strict timing requirements must be followed. It is generally recommended to first disable the outputs using the $\overline{OE}$ pin, allow the DIRn signal to stabilize, and then re-enable the outputs. This sequence prevents bus contention and signal conflicts.

Table 2. Device Function Table

Supply Voltage	Input		Input/Output	
V_{CCA}, V_{CCB}	$\overline{OE}$ (1)	DIRn (1)	An(1)	Bn (1)
0.8 V to 3.6 V	L	L	An = Bn	Input
0.8 V to 3.6 V	L	H	Input	Bn = An
0.8 V to 3.6 V	H	X	Hi-Z	Hi-Z
0V	X	X	Hi-Z	Hi-Z

(1) The An, DIRn and $\overline{OE}$ input circuit is referenced to V_{CCA}. The Bn input circuit is referenced to V_{CCB}.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The T74V4T774 can be used for level-translation applications to interface devices or systems operating at different supply voltages. This device is an ideal solution for bidirectional data transmission scenarios. It is recommended to connect all unused I/O pins to ground, and no I/O pins should be left floating during direction switching. When the supply voltage exceeds 1.8V, the device can support a maximum data rate of up to 380 Mbps.

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer Handsets
- Industrial Automation

Typical Application

A typical application is shown in Figure 6. The T74V4T774 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The T74V4T774 device is ideal for use in applications where a push-pull driver is connected to the data I/Os.

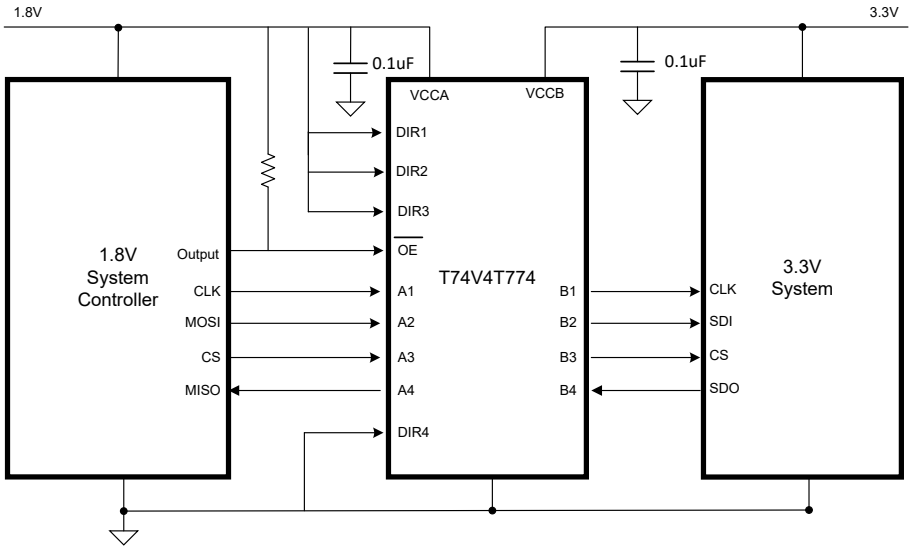


Figure 6. Typical Application Circuit

Layout

Layout Example

Reflections and matching are closely related to loop antenna theory but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in the width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they have to turn corners. Below are progressively better techniques for rounding corners. Only the last example (BEST) maintains a constant trace width and minimizes reflections.

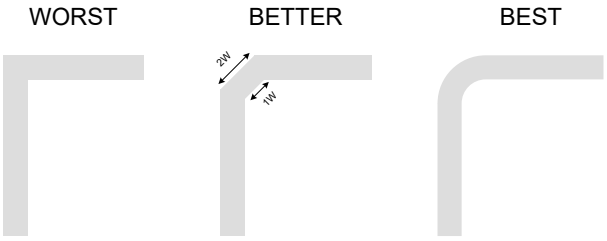


Figure 7. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

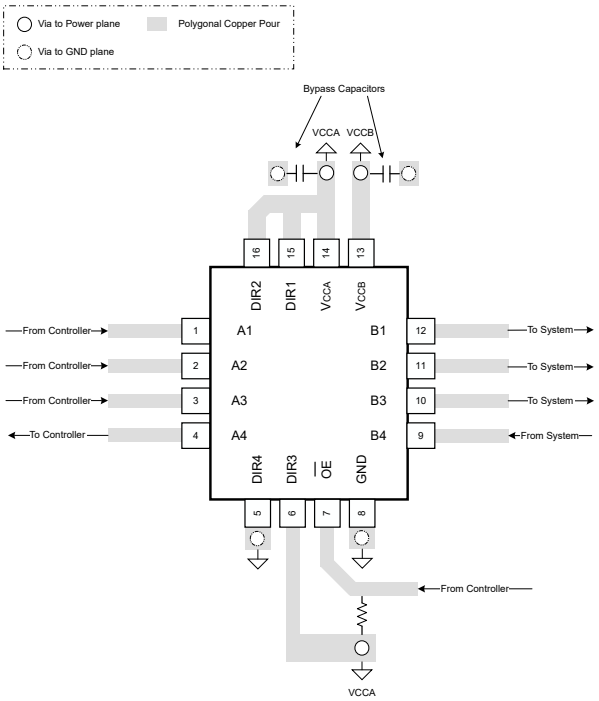
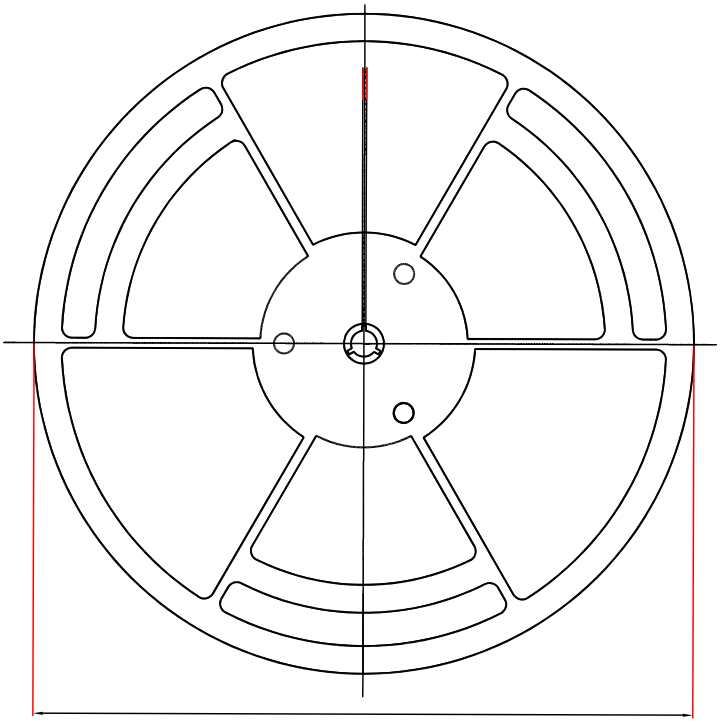
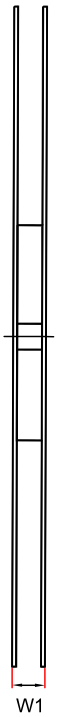
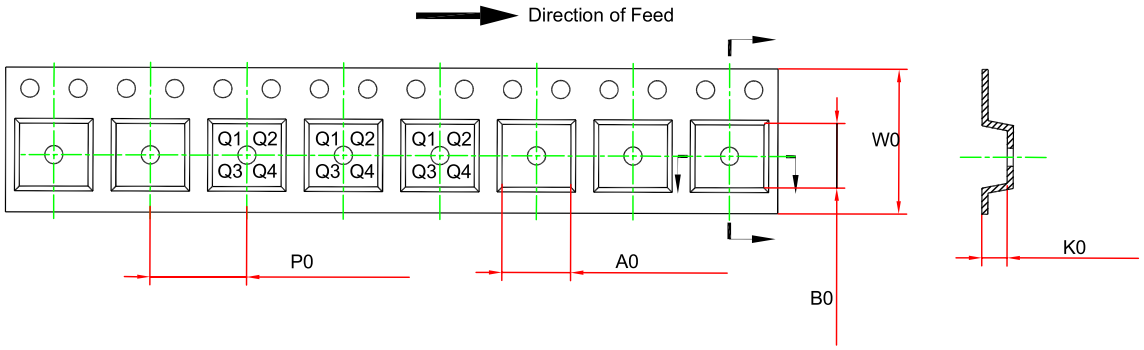


Figure 8. Layout Example

Tape and Reel Information





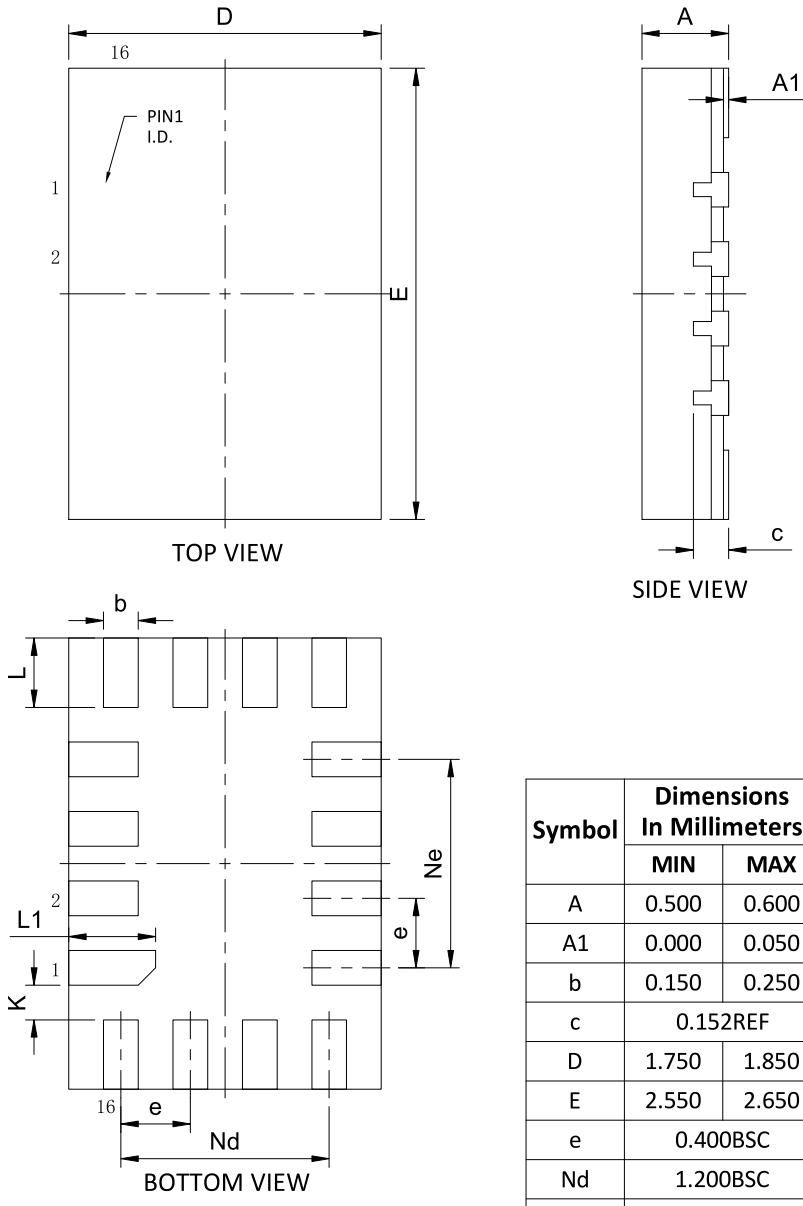


Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
T74V4T774-QN6R	QFN1.8X2.6-16	178	2.1	0.75	8.0	12.1	2.9	4.0	Q1

Package Outline Dimensions

QFN1.8X2.6-16

Package Outline Dimensions QN6(QFN1.8X2.6-16-C)

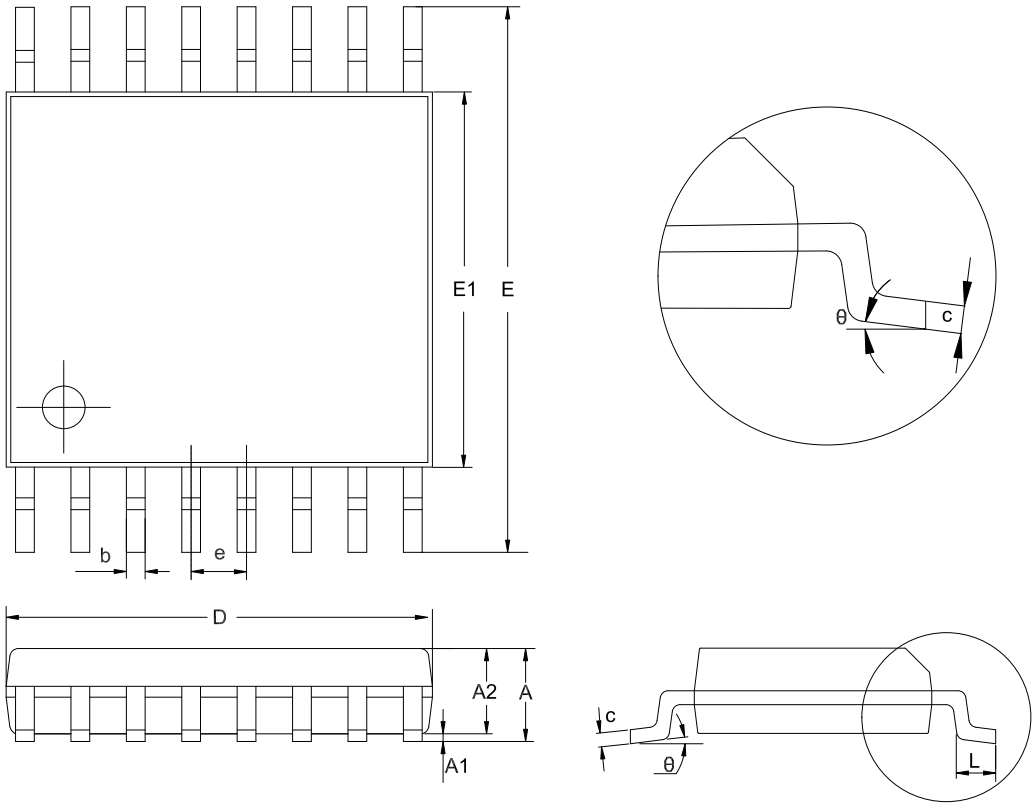


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
b	0.150	0.250	0.006	0.010
c	0.152REF		0.006	
D	1.750	1.850	0.069	0.073
E	2.550	2.650	0.100	0.104
e	0.400BSC		0.016	
Nd	1.200BSC		0.047	
Ne	1.200BSC		0.047	
L	0.350	0.450	0.014	0.018
L1	0.450	0.550	0.018	0.022
K	0.200REF		0.008	

NOTES:
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

TSSOP16

Package Outline Dimensions TS3(TSSOP-16-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
T74V4T774-QN6R	−40 to 125°C	QFN1.8X2.6-16	B77	MSL3	Tape and Reel,3000	Green
T74V4T774-TS3R (1)	−40 to 125°C	TSSOP16	4T774	MSL3	Tape and Reel,3000	Green

(1) For future products, contact the 3PEAK factory for more information and samples.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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