Features

- 8-bit Buffer Driver with 3-state Outputs
- Supply Voltage: 2 V to 5.5 V
- Latch-up Performance Exceeds 100 mA per JESD 78 Class II
- ESD Protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 Class 3B Exceeds 8000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 Class C3 Exceeds 1000 V

Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer Handsets
- Industrial Automation

Description

The T74L541 is an 8-bit buffer/line driver featuring 3-state outputs. This device incorporates two active-low output enable pins ($\overline{OE1}$ and $\overline{OE2}$), the outputs are enabled only when both $\overline{OE1}$ and $\overline{OE2}$ are LOW. A HIGH on either $\overline{OE1}$ or $\overline{OE2}$ will place the outputs in a high-impedance state.

The T74L541 is available in the TSSOP20 package and is characterized from −40°C to +125°C.

Typical Application

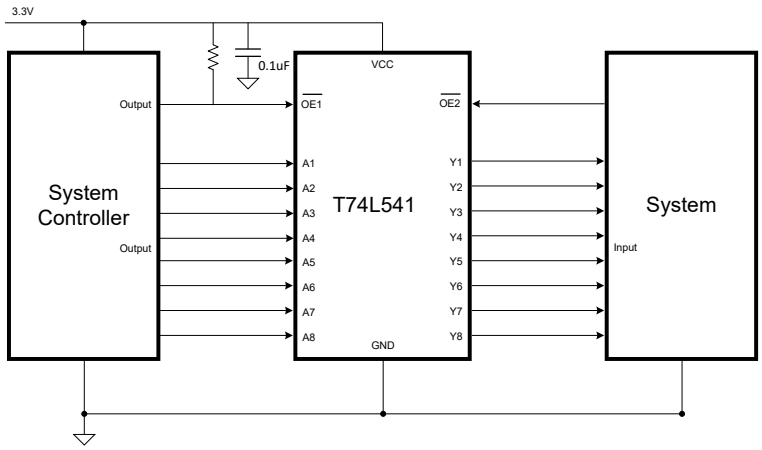


Table of Contents

Revision History

Date	Revision	Notes
2025-07-01	Rev.P.0	Initial version
2026-01-22	Rev.A.0	Released version

Pin Configuration and Functions

T74L541-TS4R
TSSOP20
Top View

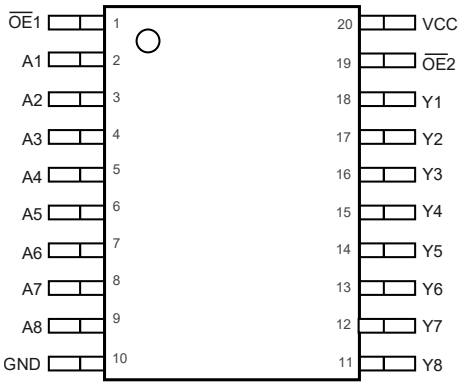


Table 1. Pin Functions: T74L541-TS4R

Pin		I/O	Description
No.	Name		
1	$\overline{OE1}$	I	Active-low Enable Input
2	A1	I	Input A1
3	A2	I	Input A2
4	A3	I	Input A3
5	A4	I	Input A4
6	A5	I	Input A5
7	A6	I	Input A6
8	A7	I	Input A7
9	A8	I	Input A8
10	GND	P	Supply Ground
11	Y8	O	Output Y8
12	Y7	O	Output Y7
13	Y6	O	Output Y6
14	Y5	O	Output Y5
15	Y5	O	Output Y4
16	Y3	O	Output Y3
17	Y2	O	Output Y2
18	Y1	O	Output Y1
19	$\overline{OE2}$	I	Active-low Enable Input
20	VCC	P	Supply Power

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CC}	DC Reference Voltage Range	−0.5	7.0	V
V_I	Input Voltage Range	−0.5	7.0	V
I_{IK}	Input Clamp Current, $V_I < 0$	−20		mA
I_{OK}	Output Clamp Current, $V_O < 0$ or $V_I > V_{CC}$	−50	50	mA
I_O	Output Current, V_O = 0 V or VCC	−35	35	mA
I_{CC}	Continuous Current through Each V_{CC} or GND	−100	100	mA
P_{tot}	Total Power Dissipation		500	mW
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 class 3B (1)	±8	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 class C3 (2)	±1	kV
LU	Latch up	JESD 78 Class II	±100	mA

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Conditions	Min	Max	Unit
V_{CC}	Supply Voltage		2	5.5	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage		0	V_{CC}	V
T_{amb}	Operation Free-air Temperature		−40	125	°C
Δt/ΔV	Input Transition Rise and Fall Rate	V_{CC} = 2.5 V ± 0.2 V		200	ns/V
		V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	ns/V

Electrical Characteristics

All test conditions : T_A = −40 ℃ to 125 ℃, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	Input Logic High	V_{CC} = 2 V	1.5			V
		V_{CC} = 2.3 V to 2.7 V	0.7 x V_{CC}			V
		V_{CC} = 3.0 V to 3.6 V	0.7 x V_{CC}			V
		V_{CC} = 4.5 V to 5.5 V	0.7 x V_{CC}			V
V_{IL}	Input Logic Low	V_{CC} = 2 V			0.5	V
		V_{CC} = 2.3 V to 2.7 V			0.3 x V_{CC}	V
		V_{CC} = 3.0 V to 3.6 V			0.3 x V_{CC}	
		V_{CC} = 4.5 V to 5.5 V			0.3 x V_{CC}	V
V_{OH}	High-level Output Voltage	I_O = −50 μA, V_{CC} = 2 V to 5.5 V	V_{CC} - 0.1			V
		I_O = −2 mA, V_{CC} = 2.3 V	2.0			V
		I_O = −8 mA, V_{CC} = 3.0 V	2.48			V
		I_O = −16 mA, V_{CC} = 4.5 V	3.8			V
V_{OL}	Low-level Output Voltage	I_O = 50 μA, V_{CC} = 2 V to 5.5 V			0.1	V
		I_O = 2 mA, V_{CC} = 2.3 V			0.4	V
		I_O = 8 mA, V_{CC} = 3.0 V			0.44	V
		I_O = 16 mA, V_{CC} = 4.5 V			0.55	V
I_I	Input Leakage Current	V_I = GND to 5.5 V, V_{CC} = 5.5 V	−5.0		5.0	μA
I_{OZ}	OFF-state Output Current	V_I = V_{IH} or V_{IL}, V_O = V_{CC} or GND, VCC = 5.5 V	−5.0		5.0	μA
I_{OFF}	Power-off Leakage Current	V_I or V_O = 5.5 V, V_{CC}= 0 V	−5.0		−5.0	uA
I_{CC}	Supply Current	V_I = GND or V_{CC}, I_O = 0 A, V_{CC} = 5.5 V	−20.0		20.0	uA
C_I (1) (2)	Input Capacitance	V_I = V_{CC} or GND		5.5		pF
C_I (1) (2)	Output Capacitance	V_O = V_{CC} or GND		7.5		pF

(1) Test data based on bench tests and design simulation, NOT test in production.
(2) T_A = 25 ℃.

AC Timing Requirements

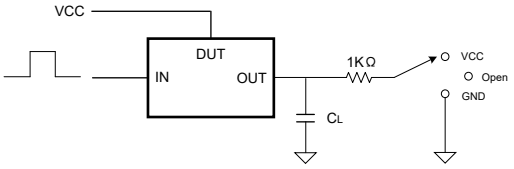
All test conditions: T_A = −40°C to 125°C, the data is based on bench test and design simulation, not test in production, unless otherwise noted.

t_{en} includes t_{PZL} and t_{PHL}, t_{dis} includes t_{PLZ} and t_{PHZ}.

Parameter		Conditions	Min	Typ	Max	Unit
t_{pd}	Propagation Delay	C_{load} = 15 pF, V_{CC}= 2.5 V ± 0.2 V	1.0		13.5	ns
		C_{load} = 15 pF, V_{CC} = 3 V ± 0.3 V	1.0		8.5	ns
		C_{load} = 15 pF, V_{CC} = 5 V ± 0.5 V	1.0		6.0	ns
		C_{load} = 50 pF, V_{CC}= 2.5 V ± 0.2 V	1.0		18.5	ns
		C_{load} = 50 pF, V_{CC} = 3 V ± 0.3 V	1.0		12.0	ns
		C_{load} = 50 pF, V_{CC} = 5 V ± 0.5 V	1.0		8.0	ns
t_{en}	Enable Time	C_{load} = 15 pF, V_{CC}= 2.5 V ± 0.2 V	1.0		18.5	ns
		C_{load} = 15 pF, V_{CC} = 3 V ± 0.3 V	1.0		12.5	ns
		C_{load} = 15 pF, V_{CC} = 5 V ± 0.5 V	1.0		8.5	ns
		C_{load} = 50pF, V_{CC}= 2.5 V ± 0.2 V	1.0		24.0	ns
		C_{load} = 50 pF, V_{CC} = 3 V ± 0.3 V	1.0		17.5	ns
		C_{load} = 50 pF, V_{CC} = 5 V ± 0.5 V	1.0		13.5	ns
t_{dis}	Disable Time	C_{load} = 15 pF, V_{CC}= 2.5 V ± 0.2 V	1.0		20.0	ns
		C_{load} = 15 pF, V_{CC} = 3 V ± 0.3 V	1.0		15.0	ns
		C_{load} = 15 pF, V_{CC} = 5 V ± 0.5 V	1.0		5.0	ns
		C_{load} = 15 pF, V_{CC}= 2.5 V ± 0.2 V	1.0		20	ns
		C_{load} = 15 pF, V_{CC} = 3 V ± 0.3 V	1.0		17.5	ns
		C_{load} = 15 pF, V_{CC} = 5 V ± 0.5 V	1.0		15	ns
t_{sk} (1)	Skew Time	V_{CC} = 2.5 V ± 0.2 V			2.0	ns
		V_{CC} = 3.0 V ± 0.3 V			1.5	ns
		V_{CC} = 5.0 V ± 0.5 V			1.0	ns

(1) T_A = 25 ℃.

Parameter Measurement Waveforms



Test	S1
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	Vcc
t_{PHZ} / t_{PZH}	GND
Open Drain	Vcc

Figure 1. Test Circuit for Measuring Switching Times

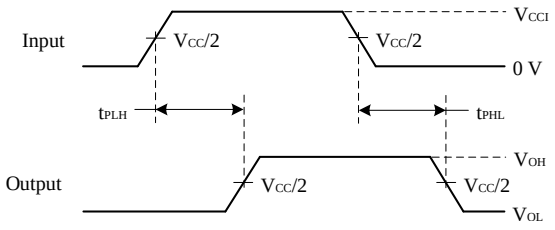


Figure 2. Propagation Delay Input to Output

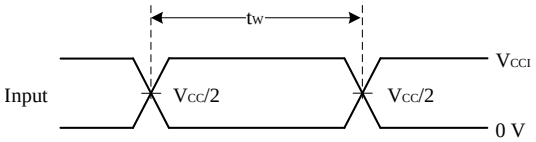


Figure 3. Switching Times

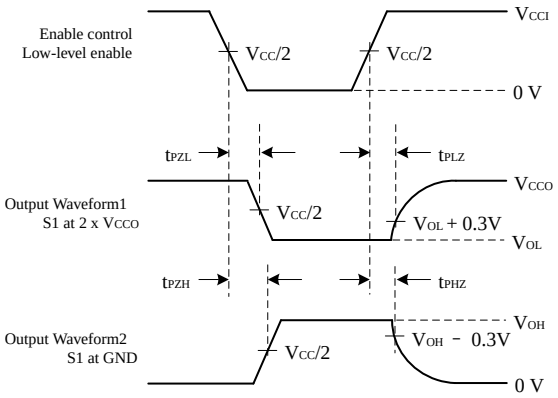


Figure 4. Enable and Disable Times

Detailed Description

Overview

The T74L541 is an 8-bit buffer driver with 3-state outputs.

- When both $\overline{OE1}$ and $\overline{OE2}$ are low, the device transmits data from the A inputs to the Y outputs.
- If either $\overline{OE1}$ or $\overline{OE2}$ is high, the outputs enter high-impedance state.

To ensure the high-impedance state is maintained during power-up or power-down, $\overline{OEn}$ should be connected to V_{CC} through a pull-up resistor. The minimum resistor value is determined by the driver's current-sinking capability.

Functional Block Diagram

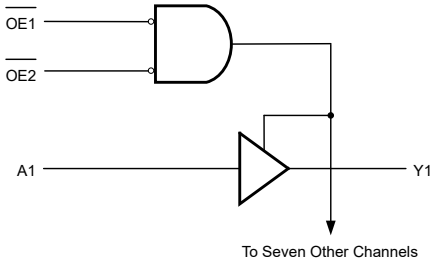


Figure 5. Functional Block Diagram

Feature Description

I_{off} Feature

The I_{off} feature supports Partial-Power-Down mode operation.

The I_{off} feature ensures safe operation when the chip is powered down (VCC = 0 V). It automatically disables all outputs in a high-impedance state, preventing any damaging backflow current from flowing through the unpowered device. This allows the bus to remain active while protecting both the chip and connected components.

Enable ($\overline{OEn}$)

The Output Enable ($\overline{OEn}$) is a critical chip function that manages output states.

Table 2. Device Function Table

V_{CC}	Input $\overline{OE1}$	Input $\overline{OE2}$	Input A	Output Y
2 V to 5.5 V	L	L	H	H
2 V to 5.5 V	L	L	L	L
2 V to 5.5 V	H	L	X	High-impedance
2 V to 5.5 V	L	H	X	High-impedance
0 V	X	X	X	High-impedance

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The T74L541 is an 8-bit buffer/line driver featuring 3-state outputs. This device incorporates two active-low output enable pins ($\overline{OE1}$ and $\overline{OE2}$), the outputs are enabled only when both $\overline{OE1}$ and $\overline{OE2}$ are LOW. A HIGH on either $\overline{OE1}$ or $\overline{OE2}$ will place the outputs in a high-impedance state.

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer Handsets
- Industrial Automation

Typical Application

A typical application is shown in Figure 6.

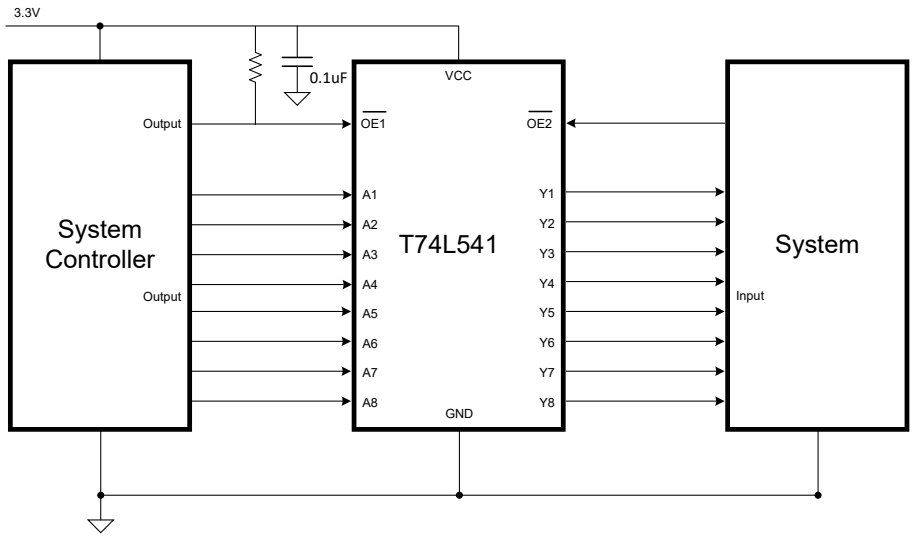


Figure 6. Typical Application Circuit

Layout

Layout Example

Reflections and matching are closely related to loop antenna theory but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in the width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they have to turn corners. Below are progressively better techniques for rounding corners. Only the last example (BEST) maintains a constant trace width and minimizes reflections.

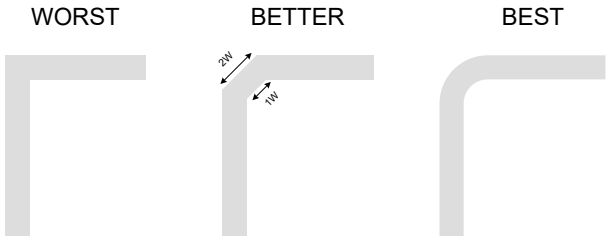


Figure 7. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

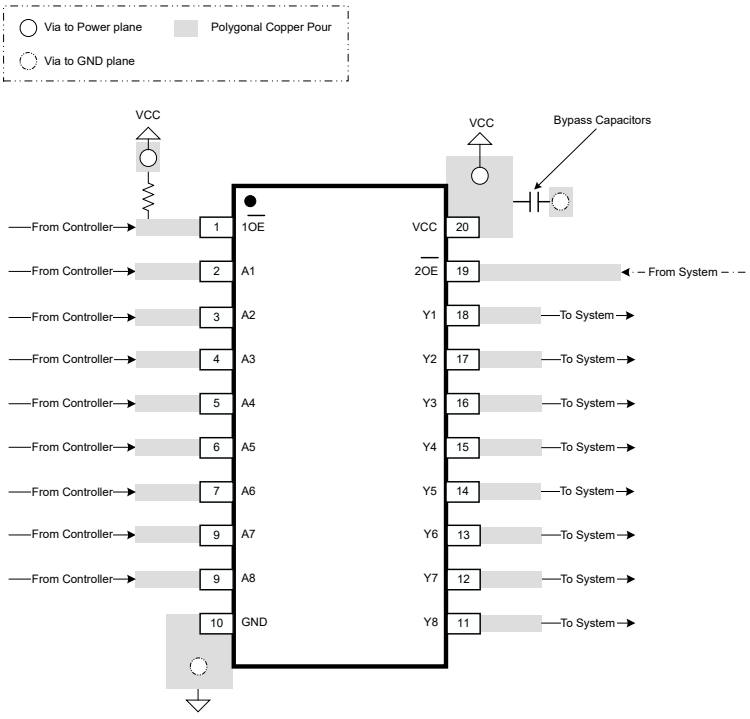
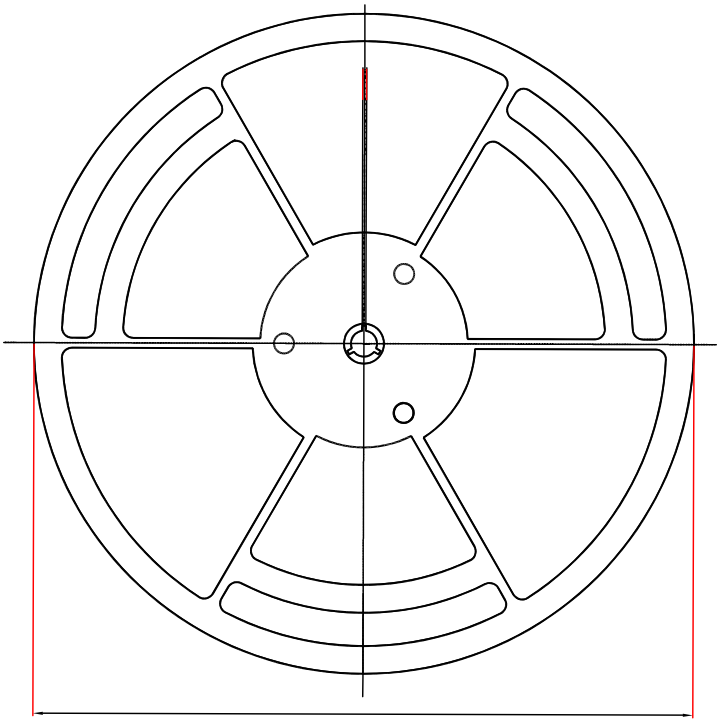
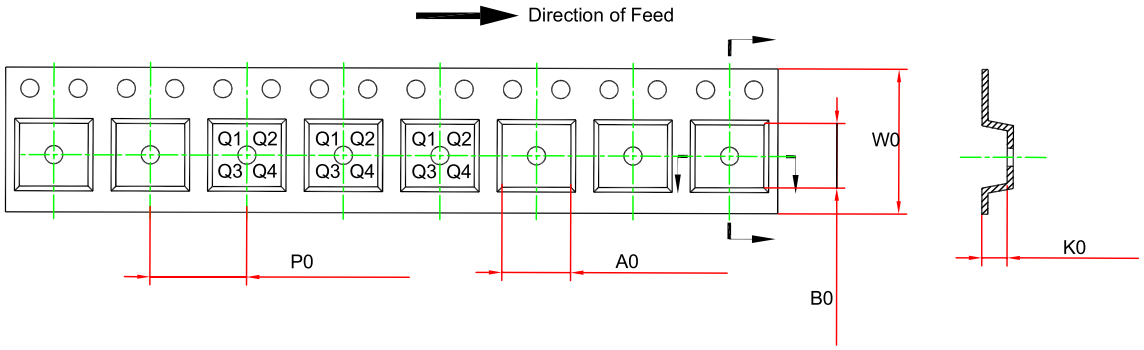


Figure 8. Layout Example

Tape and Reel Information



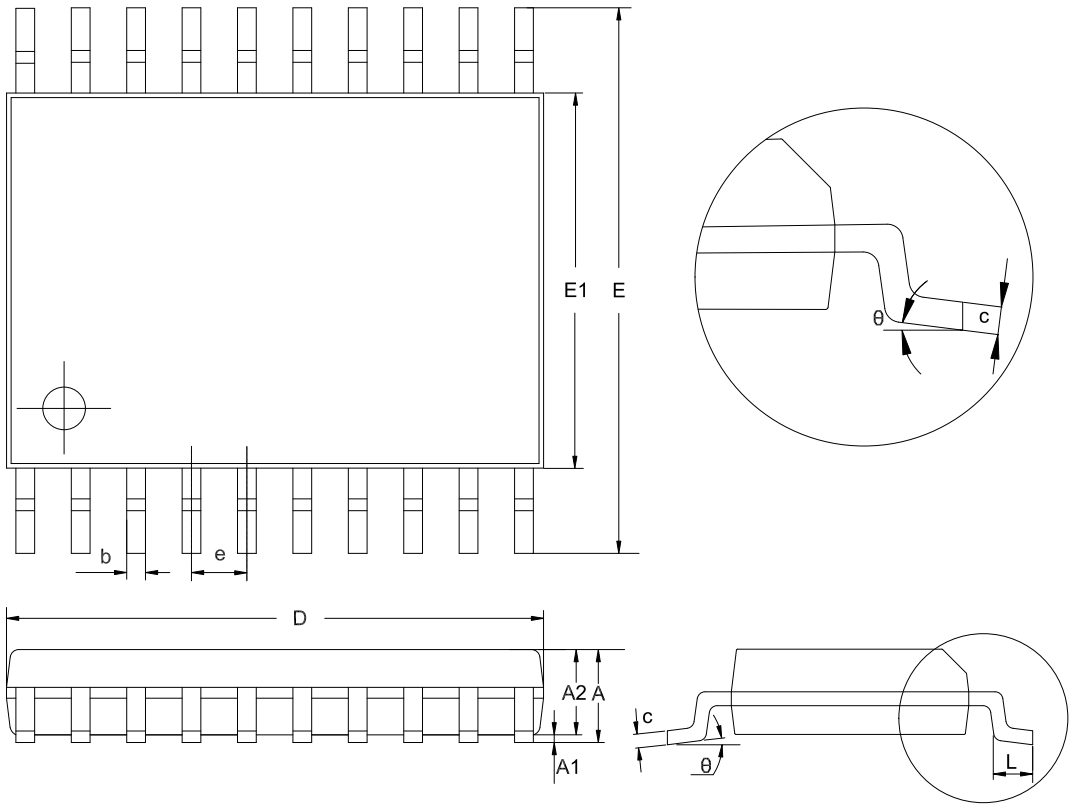


Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
T74L541-TS4R	TSSOP20	330	6.95	1.6	16.0	20.4	7.1	8.0	Q1

Package Outline Dimensions

TSSOP20

Package Outline Dimensions TS4(TSSOP-20-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	6.400	6.600	0.252	0.260
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
T74L541-TS4R	−40 to 125°C	TSSOP20	LV541	MSL3	Tape and Reel,4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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