Dual Supply Translating Transceiver; 3-state

Features

- 2-bit Dual Supply Translating Transceiver with Configurable Voltage Translation
- Voltage-Level Translation Between:
  - V_{CCA} Range: 1.65 V to 5.5 V
  - V_{CCB} Range: 1.65 V to 5.5 V
- Support Partial Power Down Mode Operation
- Maximum Data Rate
  - Translation from 3.3 V to 5 V: 420 Mbps
  - Translation to 3.3 V: 210 Mbps
  - Translation to 2.5 V: 140 Mbps
  - Translation to 1.8 V: 75 Mbps
- ESD Protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 Class 3B Exceeds 8000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 Class C3 Exceeds 1000 V
- Latch-up Performance Exceeds 100 mA Per JESD 78 Class II

Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer Handsets
- Industrial Automation

Description

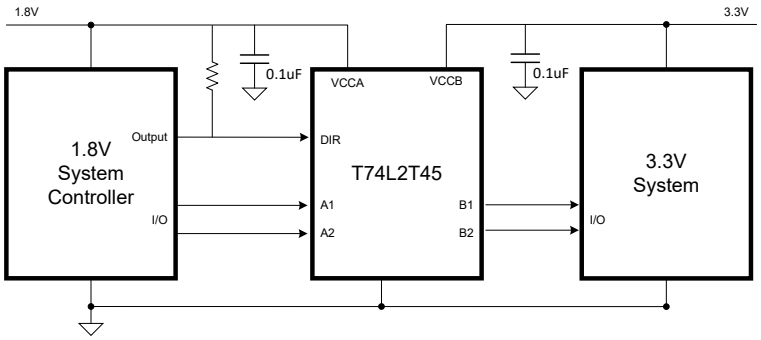
The T74L2T45 is designed for asynchronous communication between two data buses. The logic level of the direction control (DIR) input activates either Port B or Port A output. When Port B output is activated, the device transmits data from Bus A to Bus B, and when Port A output is activated, it transmits data from Bus B to Bus A. The input circuits on Port A and Port B are always active and must be driven to a logic high or low level to prevent excessive I_{CC} and I_{CCZ}.

Port A is designed to track V_{CCA}, which can accept any supply voltage from 1.65 V to 5.5 V. Port B is designed to track V_{CCB}, which can also accept any supply voltage from 1.65 V to 5.5 V. This enables universal low-voltage bidirectional translation between 1.8 V, 2.5 V, 3.3 V, and 5 V voltage nodes.

The V_{CC} isolation feature ensures that when either V_{CC} input is grounded, both ports enter a high-impedance state.

The T74L2T45 is available in the VSSOP8 package and is characterized from −40°C to +125°C.

Typical Application



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Revision History

Date	Revision	Notes
2026-08-26	Rev.A.0	Released version

Pin Configuration and Functions

T74L2T45-VS3R
VSSOP8
Top View

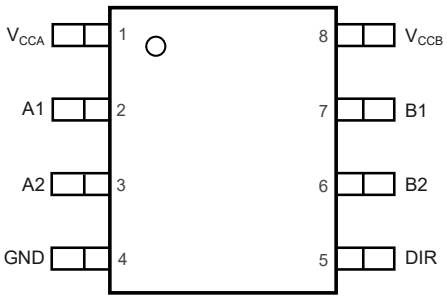


Table 1. Pin Functions: T74L2T45-VS3R

Pin		I/O	Description
No.	Name		
1	V_{CCA}	P	Side-A Supply Voltage
2	A1	I/O	Input/output A1. Referenced to V_{CCA}
3	A2	I/O	Input/output A2. Referenced to V_{CCA}
4	GND	P	Supply Ground
5	DIR	I	Direction Control
6	B2	I/O	Input/output B2. Referenced to V_{CCB}
7	B1	I/O	Input/output B1. Referenced to V_{CCB}
8	V_{CCB}	P	Side-B Supply Voltage

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CCA}	DC Reference Voltage Range, Side-A	−0.5	6.5	V
V_{CCB}	DC Reference Voltage Range, Side-B	−0.5	6.5	V
I_{IK}	Input Clamp Current, V_I < 0		50	mA
I_{OK}	Output Clamp Current, $V_{I/O}$ < 0		50	mA
V_I	Input Voltage Range	−0.5	6.5	V
I_O	Output Current, V_O = 0 V or V_{CC}	−50	50	mA
I_{CC}	Continuous Current through Each V_{CCA}, V_{CCB}, or GND	−100	100	mA
P_{tot}	Total Power Dissipation		500	mW
T_J	Operating Junction Temperature		150	°C
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The values of V_{CC} are provided in the recommended operating conditions table.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1) class 3B	±8	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2) class C3	±1	kV
LU	Latch up	LU, Per JESD78, All Pins	±100	mA

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Conditions	Min	Typ	Max	Unit
V_{CCA}	Supply Voltage, Side-A		1.65		5.5	V
V_{CCB}	Supply Voltage, Side-B		1.65		5.5	V
Δt/ ΔV	Input	1.65 V to 1.95 V			20	ns/V
		2.3 V to 2.7 V			20	
		3 V to 3.6 V			10	
		4.5 V to 5.5 V			5	
V_I	Input Voltage		0		5.5	V

Parameter		Conditions	Min	Typ	Max	Unit
V_O	Output Voltage		0		V_{CCO}	V
T_A	Ambient Temperature		−40		125	°C

(1) V_{CCO} is the supply voltage of the output side-A or side-B port.

Electrical Characteristics

All test conditions: V_{CCA} = 1.65 V to 5.5 V, V_{CCB} = 1.65 V to 5.5 V, T_A = −40°C to 125°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	Input Logic High (Data Input)	V_{CCI} = 1.65 V to 1.95 V	0.65 * V_{CCI}			V
		V_{CCI} = 2.3 V to 2.7 V	1.7			V
		V_{CCI} = 3.0 V to 3.6 V	2			V
		V_{CCI} = 4.5 V to 5.5 V	0.7 * V_{CCI}			V
	Input Logic High (DIR Input)	V_{CCA} = 1.65 V to 1.95 V	0.72 * V_{CCA}			V
		V_{CCA} = 2.3 V to 2.7 V	1.7			V
		V_{CCA} = 3.0 V to 3.6 V	2			V
		V_{CCA} = 4.5 V to 5.5 V	0.7 * V_{CCA}			V
V_{IL}	Input Logic Low (Data Input)	V_{CCI} = 1.65 V to 1.95 V			0.35 * V_{CCI}	V
		V_{CCI} = 2.3 V to 2.7 V			0.7	V
		V_{CCI} = 3.0 V to 3.6 V			0.8	V
		V_{CCI} = 4.5 V to 5.5 V			0.3 * V_{CCI}	V
	Input Logic Low (DIR input)	V_{CCA} = 1.65 V to 1.95 V			0.35 * V_{CCA}	V
		V_{CCA} = 2.3 V to 2.7 V			0.7	V
		V_{CCA} = 3.0 V to 3.6 V			0.8	V
		V_{CCA} = 4.5 V to 5.5 V			0.3 * V_{CCA}	V
V_{OH}	High-Level Output Voltage (Data Output)	V_{CCO} = 1.65 V, I_O = −8 mA	1.2			V
		V_{CCO} = 2.3 V, I_O = −12 mA	1.9			V
		V_{CCO} = 3.0 V, I_O = −24 mA	2.35			V
		V_{CCO} = 4.5 V, I_O = −32 mA	3.78			V
V_{OL}	Low-Level Output Voltage (Data Output)	V_{CCO} = 1.65 V, I_O = 8 mA			0.45	V
		V_{CCO} = 2.3 V, I_O = 12 mA			0.3	V
		V_{CCO} = 3.0 V, I_O = 24 mA			0.55	V
		V_{CCO} = 4.5 V, I_O = 32 mA			0.6	V
I_I	Input Leakage Current	DIR Input, V_I = 0 V to 5.5 V, V_{CCI} = 1.65 V to 5.5 V	−10		10	μA
I_{OZ}	OFF-state Output Current	A or B Port, V_O = 0 V or V_{CCO}, V_{CCO} = 1.65 V to 5.5 V	−10		10	μA
I_{off}	Power-off Leakage Current	A Port, V_I or V_O = 0 V to 5.5 V, V_{CCA} = 0 V, V_{CCB} = 1.65 V to 5.5 V	−10		10	μA
		B Port, V_I or V_O = 0 V to 5.5 V, V_{CCB} = 0 V, V_{CCA} = 1.65 V to 5.5 V	−10		10	μA

Parameter		Conditions	Min	Typ	Max	Unit
I_{CCA}	Supply Current	A port, V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCA} = 1.65 V to 5.5 V, V_{CCB} = 1.65 V to 5.5 V			20	μA
		A port, V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCA} = 5.5 V, V_{CCB} = 0 V			20	μA
		A port, V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCB} = 5.5 V, V_{CCA} = 0 V	−4			μA
I_{CCB}	Supply Current	B port, V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCA} = 1.65 V to 5.5 V, V_{CCB} = 1.65 V to 5.5 V			20	μA
		B port, V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCB} = 5.5 V, V_{CCA} = 0 V	−4			μA
		B port, V_I = 0 V or V_{CCI}, I_O = 0 A, V_{CCA} = 5.5 V, V_{CCB} = 0 V			20	μA
I_{CCA} + I_{CCB}	Combined Supply Current	A plus B port, I_O = 0 A, V_I = 0 V or V_{CCI}, V_{CCA} = 1.65 V to 5.5 V, V_{CCB} = 1.65 V to 5.5 V			30	μA
ΔICC	Additional Supply Current	A Port, A Port at V_{CCA} - 0.6 V, DIR at V_{CCA}, B Port Open			75	μA
		DIR Input, DIR at V_{CCA} - 0.6 V, A Port at V_{CCA}or GND, B Port Open			75	μA
		B Port, B Port at V_{CCB} - 0.6 V, DIR at GND, A Port Open			75	μA
C_I(1)	Input Capacitance	DIR, V_{CCI} = 0 V or 5.5 V, V_{CCA} = 5.5 V, V_{CCB} = 5.5 V		6		pF
C_{IO}(1)	Input/output Capacitance	A or B Port, V_{CCO} = 5.5 V or 0 V, V_{CCA} = 5.5 V, V_{CCB} = 5.5 V		10		pF

(1) Test data based on bench tests and design simulation, NOT test in production.

AC Timing Requirements — V_{CCA} = 1.8 V

All test conditions: T_A = −40°C to +125°C, V_{CCA} = 1.8 V ± 0.15 V, the data is based on bench test and design simulation, NOT test in production, unless otherwise noted.

t_{en} includes t_{PZL} and t_{PZH}, t_{dis} includes t_{PLZ} and t_{PHZ}.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay	A-to-B push-pull driving	1.8 V ± 0.15 V	1.0		25.9	ns
			2.5 V ± 0.2 V	1.0		13.2	ns
			3.3 V ± 0.3 V	1.0		11.4	ns
			5 V ± 0.5 V	1.0		11.1	ns
		B-to-A push-pull driving	1.8 V ± 0.15 V	1.0		28.8	ns
			2.5 V ± 0.2 V	1.0		27.6	ns
			3.3 V ± 0.3 V	1.0		27.4	ns
			5 V ± 0.5 V	1.0		27.4	ns
t_{en}	Enable Time	DIR-to-A	1.8 V ± 0.15 V	1.0		28	ns
			2.5 V ± 0.2 V	1.0		27.8	ns
			3.3 V ± 0.3 V	1.0		27.7	ns
			5 V ± 0.5 V	1.0		27.7	ns
		DIR-to-B	1.8 V ± 0.15 V	1.0		40	ns
			2.5 V ± 0.2 V	1.0		20	ns
			3.3 V ± 0.3 V	1.0		16.6	ns
			5 V ± 0.5 V	1.0		14.8	ns
t_{dis}	Disable Time	DIR-to-A	1.8 V ± 0.15 V	1.0		33.6	ns
			2.5 V ± 0.2 V	1.0		33.4	ns
			3.3 V ± 0.3 V	1.0		33.3	ns
			5 V ± 0.5 V	1.0		33.2	ns
		DIR-to-B	1.8 V ± 0.15 V	1.0		36.2	ns
			2.5 V ± 0.2 V	1.0		17.1	ns
			3.3 V ± 0.3 V	1.0		16	ns
			5 V ± 0.5 V	1.0		14.3	ns
C_{PD}(1)	Power Dissipation Capacitance	A port, A-to-B	1.8 V		1		pF
		A port, B-to-A			17		pF
		B port, A-to-B			17		pF
		B port, B-to-A			1		pF

(1) Tested at V_{CCA} = 1.8 V, T_A = 25°C.

AC Timing Requirements — V_{CCA} = 2.5 V

All test conditions: T_A = −40°C to +125°C, V_{CCA} = 2.5 V ± 0.2 V, the data is based on bench test and design simulation, NOT test in production, unless otherwise noted.

t_{en} includes t_{PZL} and t_{PZH}, t_{dis} includes t_{PLZ} and t_{PHZ}.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay	A-to-B push-pull driving	1.8 V ± 0.15 V	1.0		25.4	ns
			2.5 V ± 0.2 V	1.0		13	ns
			3.3 V ± 0.3 V	1.0		10.2	ns
			5 V ± 0.5 V	1.0		8.8	ns
		B-to-A push-pull driving	1.8 V ± 0.15 V	1.0		13.3	ns
			2.5 V ± 0.2 V	1.0		13.1	ns
			3.3 V ± 0.3 V	1.0		12.9	ns
			5 V ± 0.5 V	1.0		12.8	ns
t_{en}	Enable Time	DIR-to-A	1.8 V ± 0.15 V	1.0		17.2	ns
			2.5 V ± 0.2 V	1.0		17.2	ns
			3.3 V ± 0.3 V	1.0		17.2	ns
			5 V ± 0.5 V	1.0		17.2	ns
		DIR-to-B	1.8 V ± 0.15 V	1.0		32.2	ns
			2.5 V ± 0.2 V	1.0		18.1	ns
			3.3 V ± 0.3 V	1.0		14.1	ns
			5 V ± 0.5 V	1.0		11.2	ns
t_{dis}	Disable Time	DIR-to-A	1.8 V ± 0.15 V	1.0		13	ns
			2.5 V ± 0.2 V	1.0		13	ns
			3.3 V ± 0.3 V	1.0		13	ns
			5 V ± 0.5 V	1.0		13	ns
		DIR-to-B	1.8 V ± 0.15 V	1.0		33.6	ns
			2.5 V ± 0.2 V	1.0		15	ns
			3.3 V ± 0.3 V	1.0		14.3	ns
			5 V ± 0.5 V	1.0		10.9	ns
C_{PD}(1)	Power Dissipation Capacitance	A port, A-to-B	2.5 V		1		pF
		A port, B-to-A			18		pF
		B port, A-to-B			18		pF
		B port, B-to-A			1		pF

(1) Tested at V_{CCA} = 2.5 V, T_A = 25°C.

AC Timing Requirements — V_{CCA} = 3.3 V

All test conditions: T_A = −40°C to +125°C, V_{CCA} = 3.3 V ± 0.3 V, the data is based on bench test and design simulation, NOT test in production, unless otherwise noted.

t_{en} includes t_{PZL} and t_{PZH}, t_{dis} includes t_{PLZ} and t_{PHZ}.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay	A-to-B push-pull driving	1.8 V ± 0.15 V	1.0		25.2	ns
			2.5 V ± 0.2 V	1.0		12.8	ns
			3.3 V ± 0.3 V	1.0		10.3	ns
			5 V ± 0.5 V	1.0		10.4	ns
		B-to-A push-pull driving	1.8 V ± 0.15 V	1.0		11.2	ns
			2.5 V ± 0.2 V	1.0		10.2	ns
			3.3 V ± 0.3 V	1.0		10.1	ns
			5 V ± 0.5 V	1.0		10	ns
t_{en}	Enable Time	DIR-to-A	1.8 V ± 0.15 V	1.0		14.1	ns
			2.5 V ± 0.2 V	1.0		13.6	ns
			3.3 V ± 0.3 V	1.0		13.2	ns
			5 V ± 0.5 V	1.0		13.2	ns
		DIR-to-B	1.8 V ± 0.15 V	1.0		31.7	ns
			2.5 V ± 0.2 V	1.0		18.4	ns
			3.3 V ± 0.3 V	1.0		12.9	ns
			5 V ± 0.5 V	1.0		10.9	ns
t_{dis}	Disable Time	DIR-to-A	1.8 V ± 0.15 V	1.0		12.2	ns
			2.5 V ± 0.2 V	1.0		12.2	ns
			3.3 V ± 0.3 V	1.0		12.2	ns
			5 V ± 0.5 V	1.0		12.2	ns
		DIR-to-B	1.8 V ± 0.15 V	1.0		33	ns
			2.5 V ± 0.2 V	1.0		14.3	ns
			3.3 V ± 0.3 V	1.0		12.6	ns
			5 V ± 0.5 V	1.0		10.3	ns
C_{PD}(1)	Power Dissipation Capacitance	A port, A-to-B	3.3 V		1		pF
		A port, B-to-A			19		pF
		B port, A-to-B			19		pF
		B port, B-to-A			1		pF

(1) Tested at V_{CCA} = 3.3 V, T_A = 25°C.

AC Timing Requirements — V_{CCA} = 5 V

All test conditions: T_A = −40°C to +125°C, V_{CCA} = 5 V ± 0.5 V, the data is based on bench test and design simulation, NOT test in production, unless otherwise noted.

t_{en} includes t_{PZL} and t_{PZH}, t_{dis} includes t_{PLZ} and t_{PHZ}.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay	A-to-B push-pull driving	1.8 V ± 0.15 V	1.0		25.4	ns
			2.5 V ± 0.2 V	1.0		12.8	ns
			3.3 V ± 0.3 V	1.0		10	ns
			5 V ± 0.5 V	1.0		8.2	ns
		B-to-A push-pull driving	1.8 V ± 0.15 V	1.0		11	ns
			2.5 V ± 0.2 V	1.0		8.8	ns
			3.3 V ± 0.3 V	1.0		8.5	ns
			5 V ± 0.5 V	1.0		8.3	ns
t_{en}	Enable Time	DIR-to-A	1.8 V ± 0.15 V	1.0		10.9	ns
			2.5 V ± 0.2 V	1.0		10.9	ns
			3.3 V ± 0.3 V	1.0		10.9	ns
			5 V ± 0.5 V	1.0		10.9	ns
		DIR-to-B	1.8 V ± 0.15 V	1.0		31.6	ns
			2.5 V ± 0.2 V	1.0		18.4	ns
			3.3 V ± 0.3 V	1.0		13.0	ns
			5 V ± 0.5 V	1.0		10.7	ns
t_{dis}	Disable Time	DIR-to-A	1.8 V ± 0.15 V	1.0		9.4	ns
			2.5 V ± 0.2 V	1.0		9.4	ns
			3.3 V ± 0.3 V	1.0		9.4	ns
			5 V ± 0.5 V	1.0		9.4	ns
		DIR-to-B	1.8 V ± 0.15 V	1.0		32.7	ns
			2.5 V ± 0.2 V	1.0		13.7	ns
			3.3 V ± 0.3 V	1.0		12	ns
			5 V ± 0.5 V	1.0		9.7	ns
C_{PD}(1)	Power Dissipation Capacitance	A port, A-to-B	5 V		1		pF
		A port, B-to-A			22		pF
		B port, A-to-B			22		pF
		B port, B-to-A			1		pF

(1) Tested at V_{CCA} = 5 V, T_A = 25°C.

Detailed Description

Overview

The T74L2T45 contains a 2-bit transceiver, with the transmission direction controlled by the DIR pin, the DIR (Direction Control) pin is referenced to V_{CCA}.

- When DIR is low, the device transmits data from the B inputs to the A outputs.
- When DIR is high, the device transmits data from the A inputs to the B outputs.

Functional Block Diagram

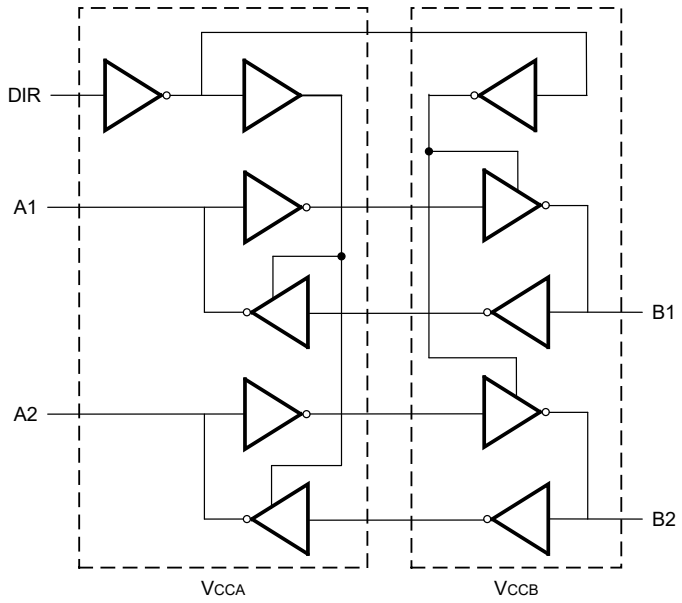


Figure 1. Functional Block Diagram

Feature Description

Fully configurable dual-rail design

Both V_{CCA} and V_{CCB} can be powered at any voltage between 1.65 V and 5.5 V, making the device suitable for translation between any voltage nodes (1.8 V, 2.5 V, 3.3 V and 5 V).

Supports high-speed level translation

The T74L2T45 supports high data rate applications. When translating signals from 3.3 V to 5 V, the translated signal can achieve data rates of up to 420 Mbps.

I_{off} Feature

The I_{off} feature ensures safe operation when V_{CCA} or V_{CCB} is powered down. It automatically disables all outputs in a high-impedance state, preventing any damaging backflow current from flowing through the unpowered device. This allows the bus to remain active while protecting both the chip and connected components.

Direction Function

Table 2. Device Function Table

V_{CCA}, V_{CCB}	Input DIR	Translator Function
1.65 V to 5.5 V	L	B => A
1.65 V to 5.5 V	H	A => B
0 V	X	Hi-Z

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The T74L2T45 is designed for asynchronous communication between two data buses. The logic level of the direction control (DIR) input activates either Port B or Port A output. When Port B output is activated, the device transmits data from Bus A to Bus B, and when Port A output is activated, it transmits data from Bus B to Bus A. The input circuits on Port A and Port B are always active and must be driven to a logic high or low level to prevent excessive I_{CC} and I_{CCZ}.

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer Handsets
- Industrial Automation

Typical Application

A typical application is shown in Figure 2.

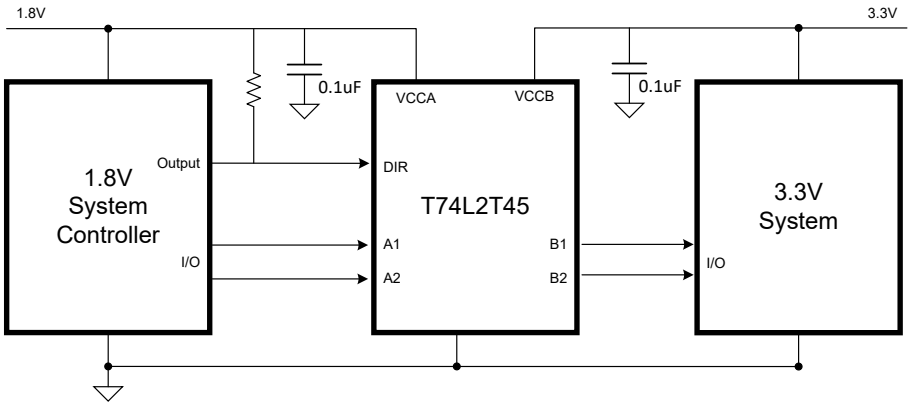


Figure 2. Typical Application Circuit

Layout

Layout Example

Reflections and matching are closely related to loop antenna theory but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in the width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they have to turn corners. Below are progressively better techniques for rounding corners. Only the last example (BEST) maintains a constant trace width and minimizes reflections.

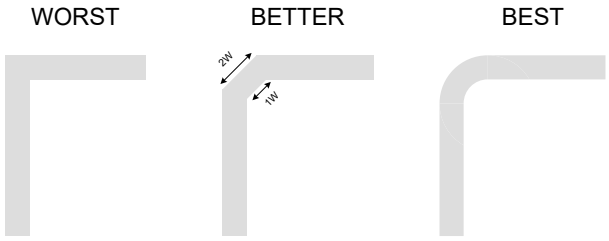


Figure 3. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

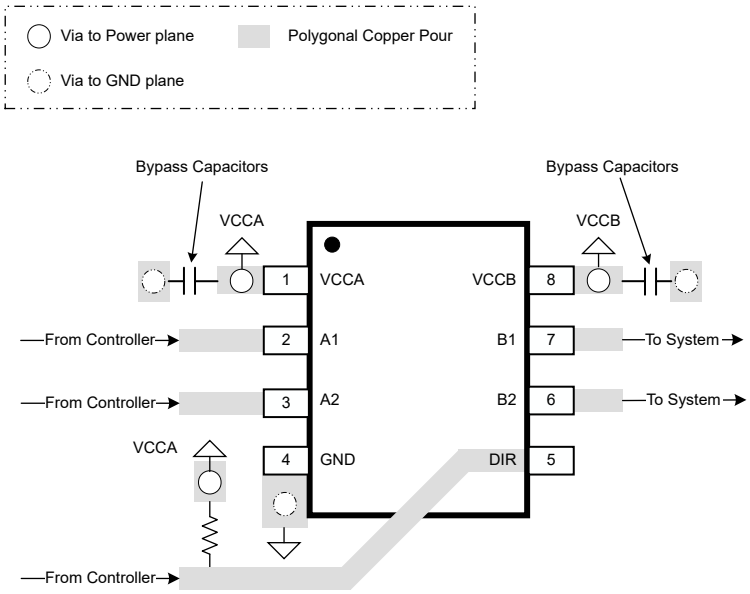
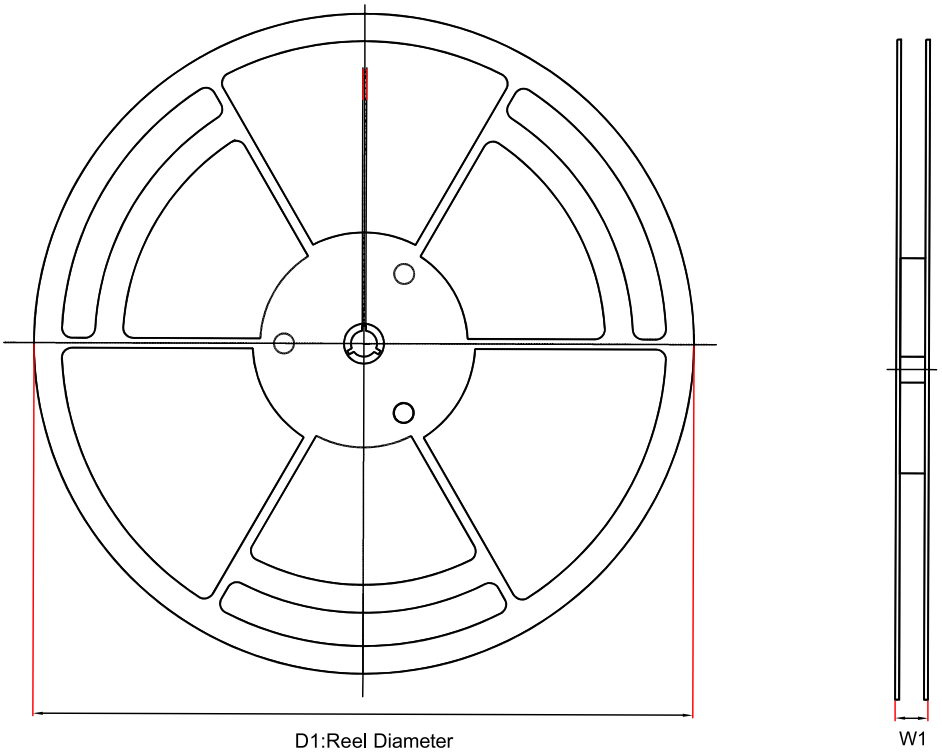
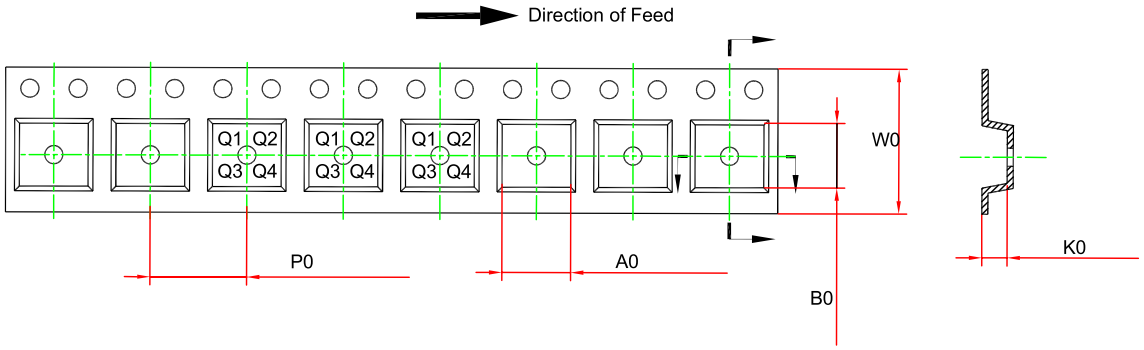


Figure 4. Layout Example

Tape and Reel Information



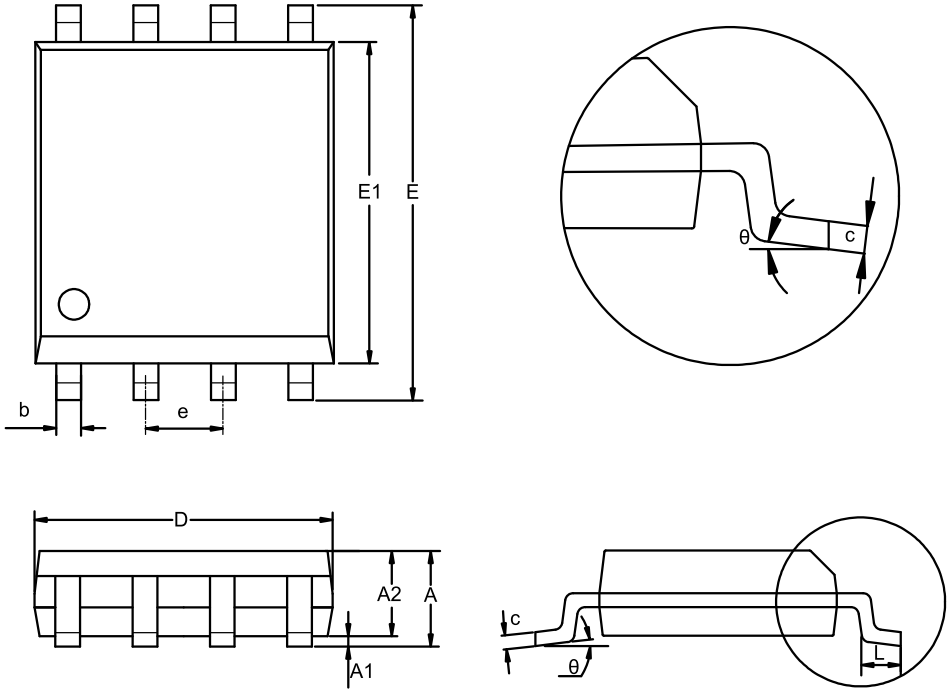


Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
T74L2T45-VS3R	VSSOP8	178	2.25	1.05	8	11.4	3.35	4	Q3

Package Outline Dimensions

VSSOP8

Package Outline Dimensions VS3(VSSOP-8-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	1.000	0.028	0.039
A1	0.000	0.150	0.000	0.006
A2	0.600	0.850	0.024	0.033
b	0.170	0.270	0.007	0.011
c	0.080	0.230	0.003	0.009
D	1.900	2.100	0.075	0.083
E	3.000	3.200	0.118	0.126
E1	2.200	2.400	0.087	0.094
e	0.500 BSC		0.020 BSC	
L	0.150	0.400	0.006	0.016
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
T74L2T45-VS3R	−40 to 125°C	VSSOP8	V45	MSL3	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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