

Features

- Wide Supply Voltage Range from 1.65 V to 5.5 V
- I/O Tolerance Inputs to 5.5 V
- All Inputs with Schmitt-Trigger Action
- CMOS Low Power Dissipation
- I_{OFF} Supports Partial Power-down Protection
- ESD Protection: ±4-kV HBM, ±1-kV CDM
- Latch-up Performance Exceeds 100 mA per JESD 78, Class II

Applications

- Computing
- Tablet PC
- Television
- Wearable Device
- Server
- Industrial Equipment

Description

The T74L2G125 is a dual 3-State output Buffer/Line Drivers with the V_{CC} supply from 1.65 V to 5.5 V. Schmitt-Trigger action with slower rise-and-fall times and better noise immunity. I_{OFF} circuits can prevent backflow current during power-down, thus supporting partial power-down protection. The outputs are disabled when the OE input is high.

The T74L2G125 is available in the DFN1.4X1-8 package and is characterized from -40°C to 125°C.

Device Table

Device	Package	Body Size
T74L2G125-DFSRR	DFN1.4X1-8	1.4 mm x 1 mm

Typical Application Circuit

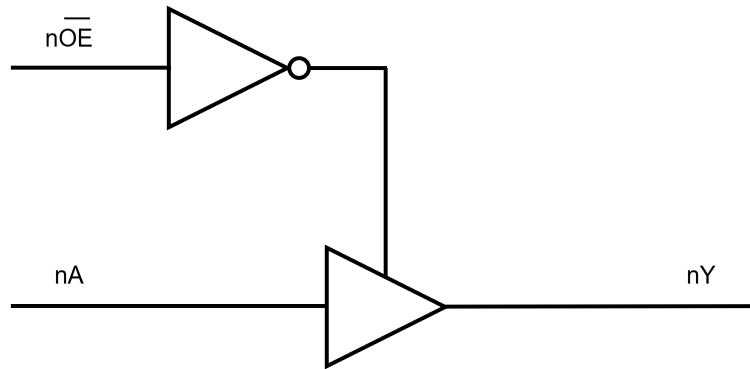


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Revision History

Date	Revision	Notes
2025-08-11	Rev.Pre.0	Initial version.
2026-08-03	Rev.A.0	Released version.

Pin Configuration and Functions

T74L2G125
DFN1.4X1-8
Top View

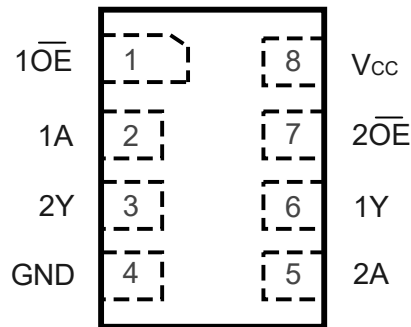


Table 1. Pin Functions

Pin No.	Name	I/O	Description
1	1OE	I	Output 1Y enable input
2	1A	I	Input 1A
3	2Y	O	Output 2Y
4	GND	Power	Ground
5	2A	I	Input 2A
6	1Y	O	Output 1Y
7	2OE	I	Output 2Y enable input
8	VCC	Power	Supply pin

Function Table

Table 2. Truth Table

Input		Output
nOE	nA	nY
L	L	L
L	H	H
H	X	Z

(1) H = High voltage level.

(2) L = Low voltage level.

(3) X = Don't care.

(4) Z = High-impedance.

Dual Bus Buffer/Line Drivers with 3-State Output

Specifications

Absolute Maximum Ratings ⁽¹⁾

Parameter		Min	Max	Unit
V _{CC}	Supply Voltage	-0.5	6.5	V
V _I	Input Voltage ⁽²⁾	-0.5	6.5	V
V _O	Output Voltage, in Power-off Mode ⁽²⁾	-0.5	6.5	V
V _O	Output Voltage, in Active Mode ⁽²⁾	-0.5	V _{CC} + 0.5	V
I _O	Continuous Output Current	-50	50	mA
I _{IK}	Input Clamp Current, V _I < 0	-50		mA
I _{OK}	Output Clamp Current, V _O < 0	-50		mA
	Continuous Current through V _{CC} or GND	-100	100	mA
T _J	Junction Temperature		150	°C
T _{STG}	Storage Temperature	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±4,000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002, all pins ⁽²⁾	±1,000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	1.65		5.5	V
V _I	Input Voltage	0		5.5	V
V _O	Output Voltage	0		V _{CC}	V
T _A	Ambient Temperature	-40		125	°C
Δt/ΔV	Input Transition Rise-and-Fall Rate, V _{CC} = 1.65 V to 2.7 V			20	ns/V
	Input Transition Rise-and-Fall Rate, V _{CC} = 2.7 V to 5.5 V			10	ns/V

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
DFN1.4X1-8	330.2	213.3	°C/W

Dual Bus Buffer/Line Drivers with 3-State Output

Electrical Characteristics – DC Parameter

All test conditions: $T_A = -40^{\circ}\text{C}$ to 125°C , all typical values are measured at $T_A = 25^{\circ}\text{C}$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.7V_{CC}$			V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7			V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2			V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7V_{CC}$			V
V_{IL}	Low-Level Input Voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$			$0.3V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$			0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$			0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$			$0.3V_{CC}$	V
V_{OH}	High-Level Output Voltage	$I_{OH} = -100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to }5.5\text{ V}$	$V_{CC} - 0.1$			V
		$I_{OH} = -4\text{ mA}; V_{CC} = 1.65\text{ V}$	0.95			V
		$I_{OH} = -8\text{ mA}; V_{CC} = 2.3\text{ V}$	1.7			V
		$I_{OH} = -12\text{ mA}; V_{CC} = 2.7\text{ V}$	1.9			V
		$I_{OH} = -24\text{ mA}; V_{CC} = 3\text{ V}$	2			V
		$I_{OH} = -32\text{ mA}; V_{CC} = 4.5\text{ V}$	3.4			V
V_{OL}	Low-Level Output Voltage	$I_{OL} = 100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to }5.5\text{ V}$			0.1	V
		$I_{OL} = 4\text{ mA}; V_{CC} = 1.65\text{ V}$			0.7	V
		$I_{OL} = 8\text{ mA}; V_{CC} = 2.3\text{ V}$			0.45	V
		$I_{OL} = 12\text{ mA}; V_{CC} = 2.7\text{ V}$			0.6	V
		$I_{OL} = 24\text{ mA}; V_{CC} = 3\text{ V}$			0.8	V
		$I_{OL} = 32\text{ mA}; V_{CC} = 4.5\text{ V}$			0.8	V
I_I	Input Leakage Current	$V_I = \text{GND or }5.5\text{ V}; V_{CC} = 0\text{ V to }5.5\text{ V}$	-1	± 0.1	1	μA
I_{OZ}	OFF-state Output Current	$V_I = V_{IH}\text{ or }V_{IL}; V_{CC} = 3.6\text{ V}; V_O = \text{GND or }5.5\text{ V}$	-1	± 0.1	1	μA
I_{OFF}	Power-off Leakage Current	$V_I\text{ or }V_O = 5.5\text{ V}; V_{CC} = 0\text{ V}$	-1	± 0.1	1	μA
I_{CC}	Supply Current	$V_I = \text{GND or }V_{CC}; I_O = 0\text{ A}; V_{CC} = 1.65\text{ V to }5.5\text{ V}$		0.1	2	μA
ΔI_{CC}	Additional Supply Current	$V_I = V_{CC} - 0.6\text{ V}; I_O = 0\text{ A}; V_{CC} = 2.3\text{ V to }5.5\text{ V}$		0.1	10	μA
$C_i^{(1)}$	Input Capacitance			2.5		pF

(1) Spec limit is based on bench characterization and design simulation, not tested in production.

Electrical Characteristics – AC Parameter

All test conditions: $T_A = -40^{\circ}\text{C}$ to 125°C , all typical values are measured at $T_A = 25^{\circ}\text{C}$, unless otherwise noted.

Symbol ⁽¹⁾	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PD}^{(2)}$	Propagation Delay at 30-pF C_{LOAD}	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	3.9	9.5	16.2	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2.6	6.2	9.9	ns
	Propagation Delay at 50-pF C_{LOAD}	$V_{CC} = 2.7\text{ V}$	3	6.1	9.3	ns
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	2.4	5.6	8.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2	4.5	6.7	ns
$t_{en}^{(3)}$	Propagation Delay at 30-pF C_{LOAD} Enable Time	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	4.2	9.4	16.2	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2.2	6.1	9.6	ns
	Propagation Delay at 50-pF C_{LOAD} Enable Time	$V_{CC} = 2.7\text{ V}$	2.6	5.6	8.8	ns
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	2	5.2	8	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	1.6	4.2	6	ns
$t_{dis}^{(4)}$	Propagation Delay at 30-pF C_{LOAD} Disable Time	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	4.3	9.5	16.5	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2.2	6.2	9.6	ns
	Propagation Delay at 50-pF C_{LOAD} Disable Time	$V_{CC} = 2.7\text{ V}$	3.5	5.8	9.3	ns
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	2.6	5.3	8.3	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	1.8	4.5	6.4	ns
$C_{PD}^{(5)}$	Power Dissipation Capacitance	$f = 10\text{ MHz}; V_{CC} = 3.3\text{ V}$ Output enable		13		pF
		$f = 10\text{ MHz}; V_{CC} = 3.3\text{ V}$ Output disable		3		pF

(1) Spec limit is based on bench characterization and design simulation, not tested in production.

(2) t_{PD} is the same as t_{PLH} and t_{PHL} .

(3) t_{en} is the same as t_{PZH} and t_{PZL} .

(4) t_{dis} is the same as t_{PHZ} and t_{PLZ} .

(5) C_{PD} is used to determine the dynamic power dissipation (PD in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

Where:

f_i = Input frequency in MHz;

f_o = Output frequency in MHz;

C_L = Output load capacitance in pF;

V_{CC} = Supply voltage in Volts;

N = Number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of the outputs.

Parameter Measurement Waveforms

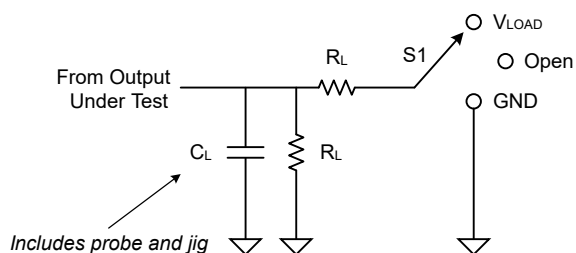


Figure 1. Timing Measurement Load Circuit

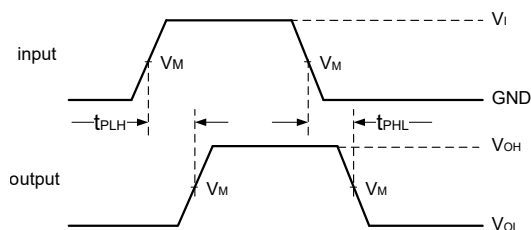


Figure 2. Propagation Delay Times

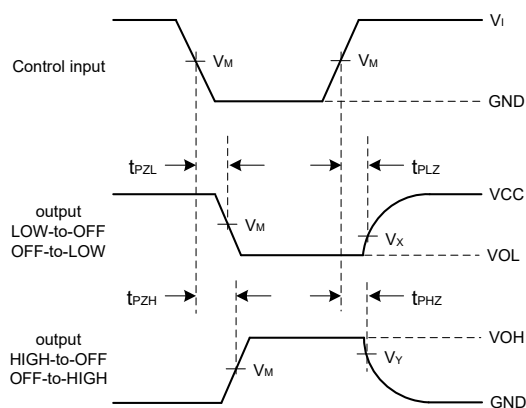


Figure 3. Enable and Disable Times

Table 3. Test Data

V _{CC}	Inputs		C _L	R _L	V _M	V _X	V _Y	S1		
	V _I	t _r /t _f						t _{PHL} /t _{PLH}	t _{PZH} /t _{PHZ}	t _{PZL} /t _{PLZ}
1.65 V to 1.95 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	0.5V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V	Open	GND	2V _{CC}
2.3 V to 2.7 V	V _{CC}	≤ 2 ns	30 pF	500 Ω	0.5V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V	Open	GND	2V _{CC}
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V	Open	GND	6 V
3 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V	Open	GND	6 V
4.5 V to 5.5 V	V _{CC}	≤ 2.5 ns	50 pF	500 Ω	0.5V _{CC}	V _{OL} + 0.3 V	V _{OH} - 0.3 V	Open	GND	2V _{CC}

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

Figure 4 shows the typical application schematic.

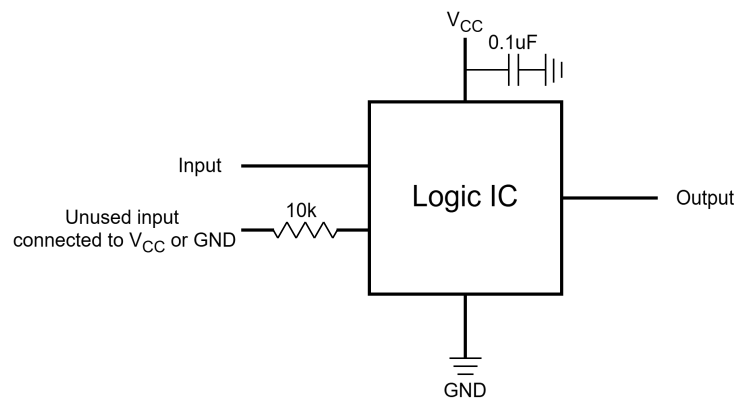
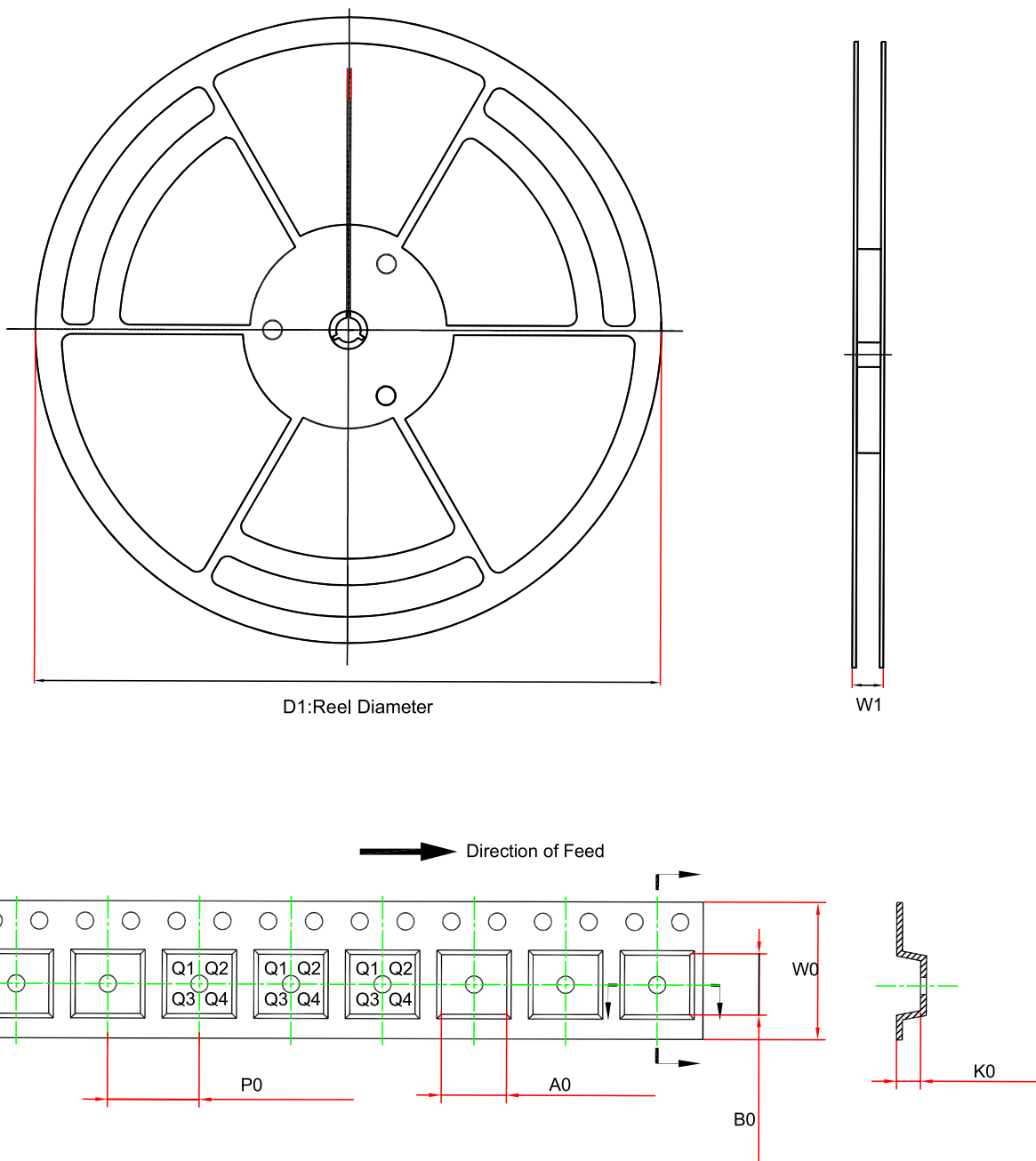


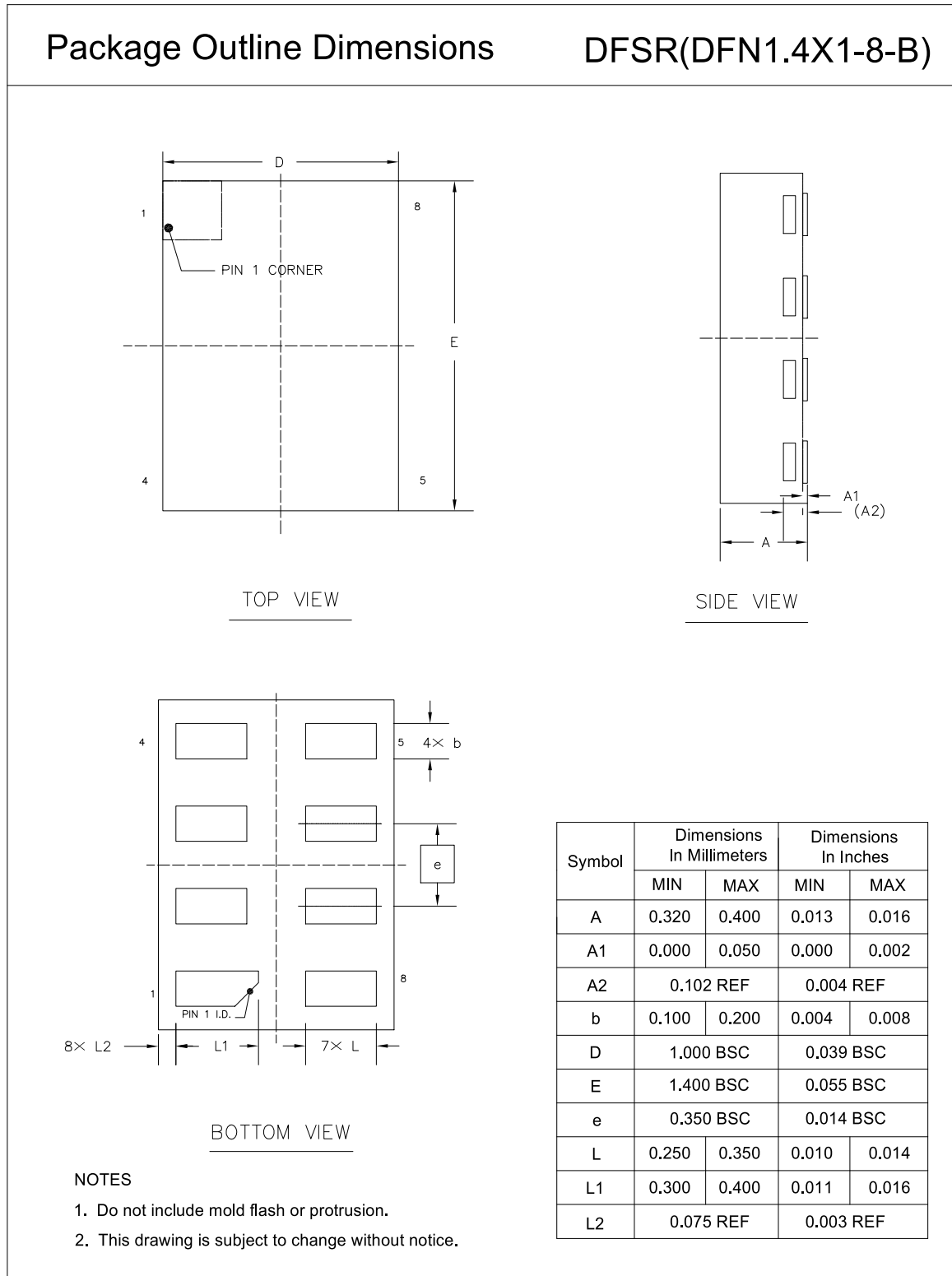
Figure 4. Typical Application Circuit

Tape and Reel Information



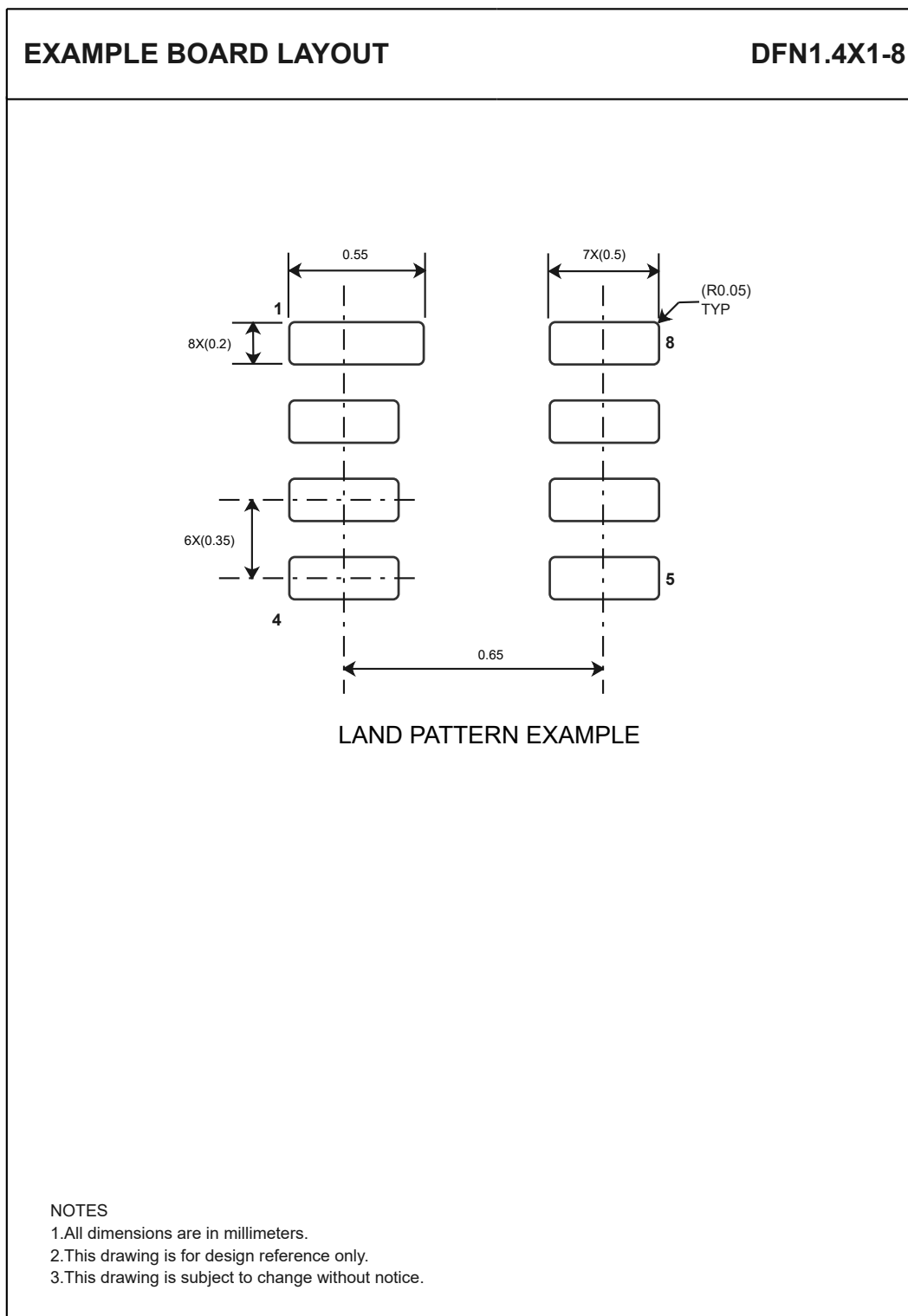
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
T74L2G125-DFSRR	DFN1.4X1-8	180	13.1	1.15	1.6	0.5	4	8	Q1

Package Outline Dimensions

DFN1.4X1-8


Example Board Layout

DFN1.4X1-8



Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
T74L2G125-DFSRR	-40 to 125°C	DFN1.4X1-8	VM	MSL3	Tape and Reel, 4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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