Features

- Used as Two 4-bit Buffers or One 8-bit Buffer
- Supply Voltage: 1.65 V to 5.5 V
- ESD Protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 Class 3B Exceeds 8000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 Class C3 Exceeds 1000 V
- Latch-up Performance Exceeds 100 mA Per JESD 78 Class II
- Specified from −40 °C to +125 °C

Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer Handsets
- Industrial Automation

Description

The T74L244 can be configured as two 4-bit buffers or one 8-bit buffer, featuring two output enable pins (1$\overline{OE}$ and 2$\overline{OE}$), each controlling four of the 3-state outputs. A high level on n$\overline{OE}$ (where n denotes 1 or 2) forces the outputs into a high-impedance state.

The T74L244 is available in the TSSOP20 package and is characterized from −40°C to +125°C.

Typical Application

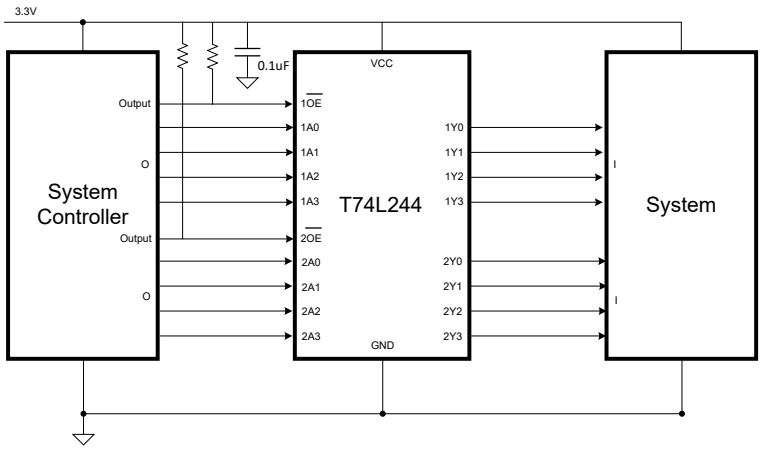


Table of Contents

Revision History

Date	Revision	Notes
2025-06-16	Rev.Pre.0	Initial version
2026-01-22	Rev.A.0	Release version

Pin Configuration and Functions

T74L244-TS4R
TSSOP20
Top View

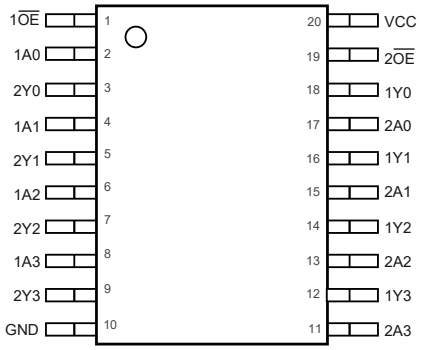


Table 1. Pin Functions: T74L244-TS4R

Pin		I/O	Description
No.	Name		
1	1$\overline{OE}$	I	Active-low Enable Input
2	1A0	I	Input 1A0
3	2Y0	O	Output 2Y0
4	1A1	I	Input 1A1
5	2Y1	O	Output 2Y1
6	1A2	I	Input 1A2
7	2Y2	O	Output 2Y2
8	1A3	I	Input 1A3
9	2Y3	O	Output 2Y3
10	GND	P	Supply Ground
11	2A3	I	Input 2A3
12	1Y3	O	Output 1Y3
13	2A2	I	Input 2A2
14	1Y2	O	Output 1Y2
15	2A1	I	Input 2A1
16	1Y1	O	Output 1Y1
17	2A0	I	Input 2A0
18	1Y0	O	Output 1Y0
19	2$\overline{OE}$	I	Active-low Enable Input
20	VCC	P	Supply Power

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CC}	DC Reference Voltage Range	−0.5	7	V
V_I	Input Voltage	−0.5	7	V
V_O	Output Voltage	−0.5	V_{CC} + 0.5	V
I_{IK}	Input Clamp Current, V_I < 0		−50	mA
I_{OK}	Output Clamp Current, V_O < 0 or V_I > V_{CC}		−50	mA
I_O	Output Current, V_O = 0 V or VCC	−50	50	mA
I_{CC}	Continuous Current through V_{CC}		100	mA
I_{GND}	Continuous Current through GND	−100		mA
P_{tot}	Total Power Dissipation		500	mW
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 class 3B (1)	±8	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 class C3 (2)	±1	kV
LU	Latch up	LU, per JESD78, All Pins	±100	mA

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Conditions	Min	Max	Unit
V_{CC}	Supply Voltage		1.65	5.5	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage		0	V_{CC}	V
T_{amb}	Operating Ambient Temperature		−40	125	°C
Δt/ΔV	Input Transition Rise and Fall Rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	ns/V

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP20	99.9	61.7	°C/W

Electrical Characteristics

All test conditions: T_A = −40 ℃ to 125 ℃, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	Input Logic High	V_{CC} = 1.65 V to 1.95 V	V_{CC} x 0.65			V
		V_{CC} = 2.3 V to 2.7 V	1.7			V
		V_{CC} = 2.7 V to 3.6 V	2			V
		V_{CC} = 4.5 V to 5.5 V	V_{CC} x 0.7			V
V_{IL}	Input Logic Low	V_{CC} = 1.65 V to 1.95 V			V_{CC} x 0.35	V
		V_{CC} = 2.3 V to 2.7 V			0.7	V
		V_{CC} = 2.7 V to 3.6 V			0.8	V
		V_{CC} = 4.5 V to 5.5 V			V_{CC} x 0.3	V
V_{OH}	High-level Output Voltage	I_O = −100 μA, V_{CC} = 1.65 V	V_{CC} - 0.3			V
		I_O = −4.0 mA, V_{CC} = 1.65 V	1.05			V
		I_O = −8.0 mA, V_{CC} = 2.3 V	1.55			V
		I_O = −12.0 mA, V_{CC} = 2.7 V	2.05			V
		I_O = −12.0 mA, V_{CC} = 3 V	2.25			V
		I_O = −24.0 mA, V_{CC} = 3 V	2			V
		I_O = −24.0 mA, V_{CC} = 5 V	V_{CC} - 0.8			V
		I_O = −32.0 mA, V_{CC} = 4.5 V	V_{CC} - 0.9			V
V_{OL}	Low-level Output Voltage	I_O = 100 μA, V_{CC} = 1.65 V			0.3	V
		I_O = 4.0 mA, V_{CC} = 1.65 V			0.65	V
		I_O = 8.0 mA, V_{CC} = 2.3 V			0.8	V
		I_O = 12.0 mA, V_{CC} = 2.7 V			0.6	V
		I_O = 24.0 mA, V_{CC} = 3 V			0.8	V
		I_O = 24.0 mA, V_{CC} = 5 V			0.8	V
		I_O = 32.0 mA, V_{CC} = 4.5 V			0.9	V
I_I	Input Leakage Current	V_I = 0 V or 5.5 V, V_{CC} = 5.5 V	−20.0		20.0	μA
I_{off}	Power-off Leakage Current	V_I or V_O = 5.5 V, V_{CC}= 0 V	−20.0		20.0	uA
I_{OZ}	OFF-state Output Current	V_O = 0 to 5.5 V, V_{CC} = 5.5 V	−20.0		20.0	μA
I_{CC}	Supply Current	V_I = GND or V_{CC}, I_O = 0 A, V_{CC} = 5.5 V			100.0	uA
ΔI_{CC}	Additional Supply Current	V_I = V_{CC} - 0.6 V, I_O = 0 A, V_{CC} = 2.7 V to 5.5 V			2.0	mA
C_I (1)	Input Capacitance	V_I = V_{CC} or GND			10	pF
C_O (1)	Output Capacitance	V_O = V_{CC} or GND			10	pF

(1) Test data based on bench tests and design simulation, NOT test in production.

AC Timing Requirements

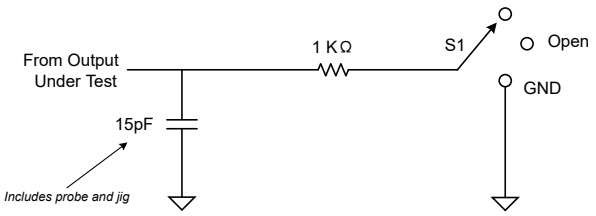
All test conditions: T_A = −40°C to 125°C, the data is based on bench test and design simulation, not test in production, unless otherwise noted.

t_{en} includes t_{PZL} and t_{PHL}, t_{dis} includes t_{PLZ} and t_{PHZ}.

Parameter		Conditions	Min	Typ	Max	Unit
t_{pd}	Propagation Delay	C_{load} = 30 pF, V_{CC} = 1.8 V ± 0.15 V			15.8	ns
		C_{load} = 30 pF, V_{CC}= 2.5 V ± 0.2 V			8.2	ns
		C_{load} = 50 pF, V_{CC}= 2.7 V			9.0	ns
		C_{load} = 50 pF, V_{CC}= 3.3 V ± 0.3 V			7.5	ns
		C_{load} = 50 pF, V_{CC} = 5 V ± 0.5 V			7.1	ns
t_{en}	Enable Time	C_{load} = 30 pF, V_{CC} = 1.8 V ± 0.15 V			20.0	ns
		C_{load} = 30 pF, V_{CC}= 2.5 V ± 0.2 V			11.0	ns
		C_{load} = 50 pF, V_{CC}= 2.7 V			11.0	ns
		C_{load} = 50 pF, V_{CC}= 3.3 V ± 0.3 V			9.5	ns
		C_{load} = 50 pF, V_{CC} = 5 V ± 0.5 V			9.1	ns
t_{dis}	Disable Time	C_{load} = 30 pF, V_{CC} = 1.8 V ± 0.15 V			11.3	ns
		C_{load} = 30 pF, V_{CC}= 2.5 V ± 0.2 V			7.4	ns
		C_{load} = 50 pF, V_{CC}= 2.7 V			8.5	ns
		C_{load} = 50 pF, V_{CC}= 3.3 V ± 0.3 V			7.5	ns
		C_{load} = 50 pF, V_{CC} = 5 V ± 0.5 V			7.1	ns
t_{SK}	Output Skew Time	C_{load} = 50 pF, V_{CC} = 5 V ± 0.5 V			2	ns
C_{PD} (1)	Power Dissipation Capacitance	Output enable, f_i = 10 MHz, V_{CC} = 5.5 V			44	pF
		Output disable, f_i = 10 MHz, V_{CC} = 5.5 V			2	pF

(1) T_A = 25 ℃.

Parameter Measurement Waveforms



Test	S1
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	Vcc
t_{PHZ} / t_{PZH}	GND
Open Drain	Vcc

Figure 1. Test Circuit for Measuring Switching Times

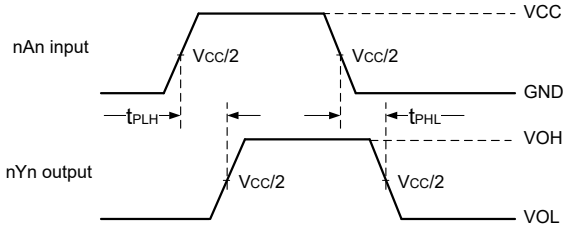


Figure 2. Propagation Delay Input to Output

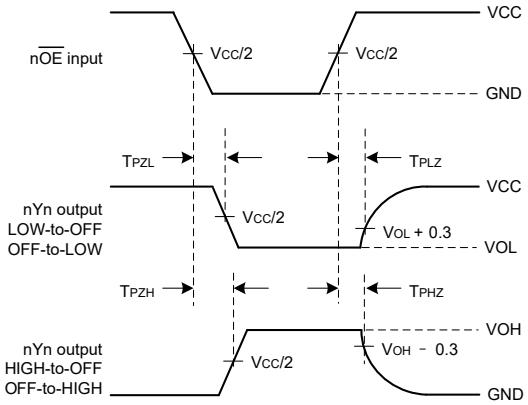


Figure 3. Enable and Disable Times

Detailed Description

Overview

The T74L244 device consists of two independent 4-bit buffers/line drivers, each with its own output-enable input.

- When $\overline{OE}$ is low, the device transmits data from the A inputs to the Y outputs.
- When $\overline{OE}$ is high, the outputs enter a high-impedance state.

To ensure the high-impedance state is maintained during power-up or power-down, $\overline{OE}$ should be connected to V_{CC} through a pull-up resistor. The minimum resistor value is determined by the driver's current-sinking capability.

Functional Block Diagram

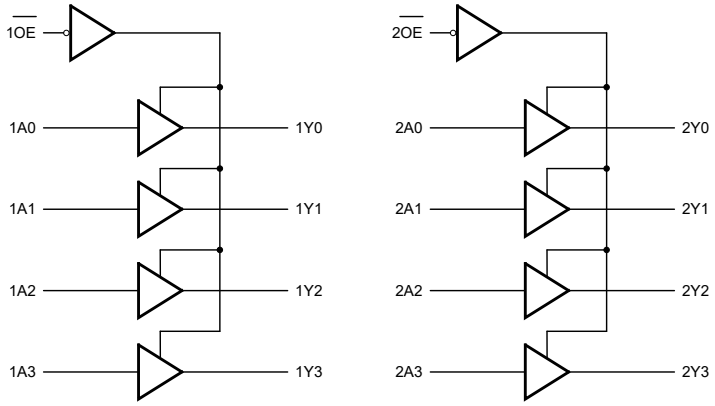


Figure 4. Functional Block Diagram

Feature Description

I_{off} Feature

The I_{off} feature ensures safe operation when the chip is powered down (V_{CC} = 0 V). It automatically disables all outputs in a high-impedance state, preventing any damaging backflow current from flowing through the unpowered device. This allows the bus to remain active while protecting both the chip and connected components.

Enable ($\overline{OE}$)

The output enable ($\overline{OE}$) is a critical chip function that manages output states. When $\overline{OE}$ is high, all output ports enter a high-impedance state, when $\overline{OE}$ is low, the chip operates normally.

Table 2. Device Function Table

V_{CC}	Input $\overline{OE}$	Input A	Output Y
1.65 V to 5 V	L	H	H
1.65 V to 5 V	L	L	L
1.65 V to 5 V	H	X	Z
0 V	X	X	Z

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The T74L244 can be configured as two 4-bit buffers or one 8-bit buffer, featuring two output enable pins (1$\overline{OE}$ and 2$\overline{OE}$), each controlling four of the 3-state outputs. A high level on n$\overline{OE}$ (where n denotes 1 or 2) forces the outputs into a high-impedance state.

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer Handsets
- Industrial Automation

Typical Application

A typical application is shown in Figure 5.

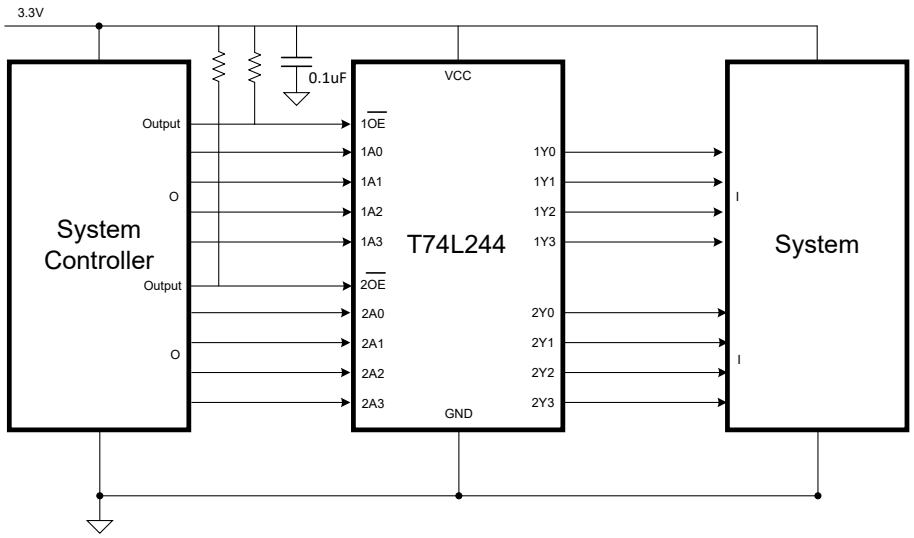


Figure 5. Typical Application Circuit

Layout

Layout Example

Reflections and matching are closely related to loop antenna theory but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in the width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they have to turn corners. Below are progressively better techniques for rounding corners. Only the last example (BEST) maintains a constant trace width and minimizes reflections.

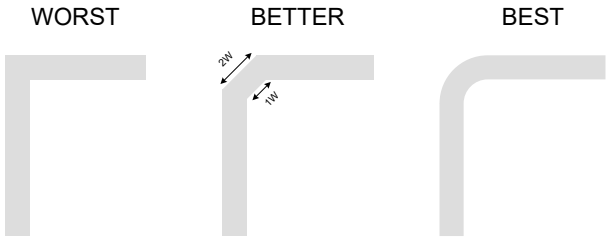


Figure 6. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

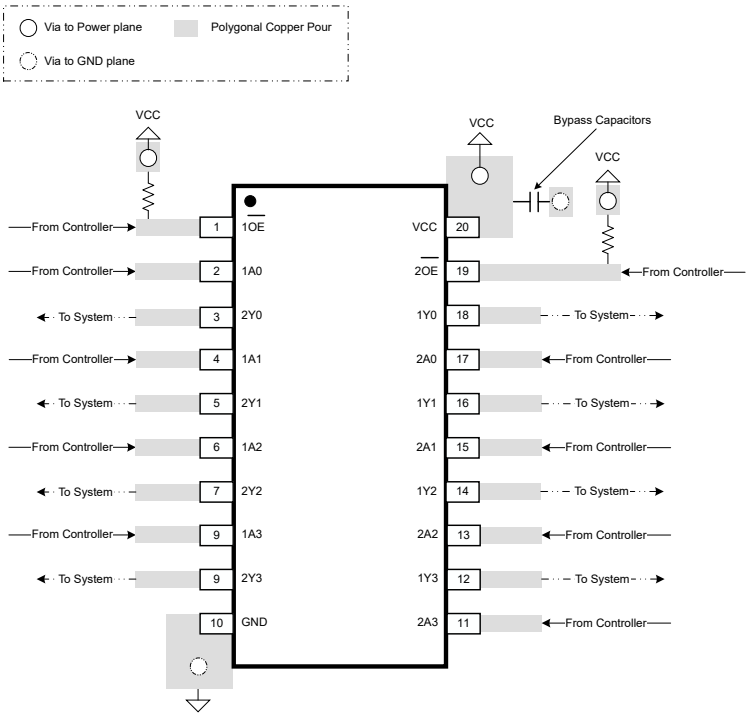
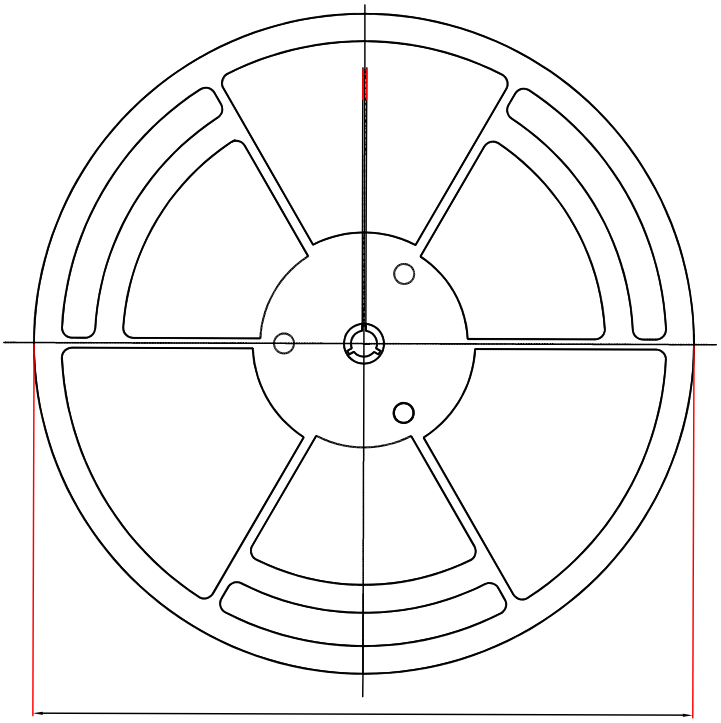
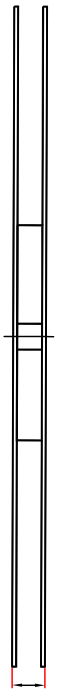
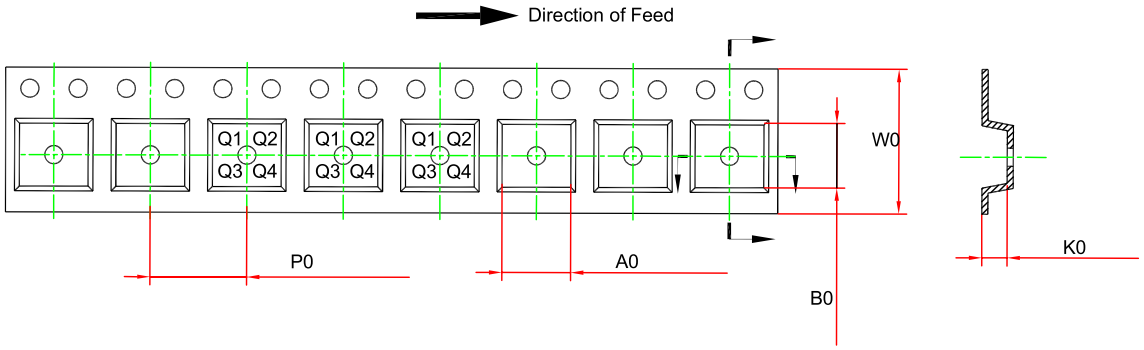


Figure 7. Layout Example

Tape and Reel Information





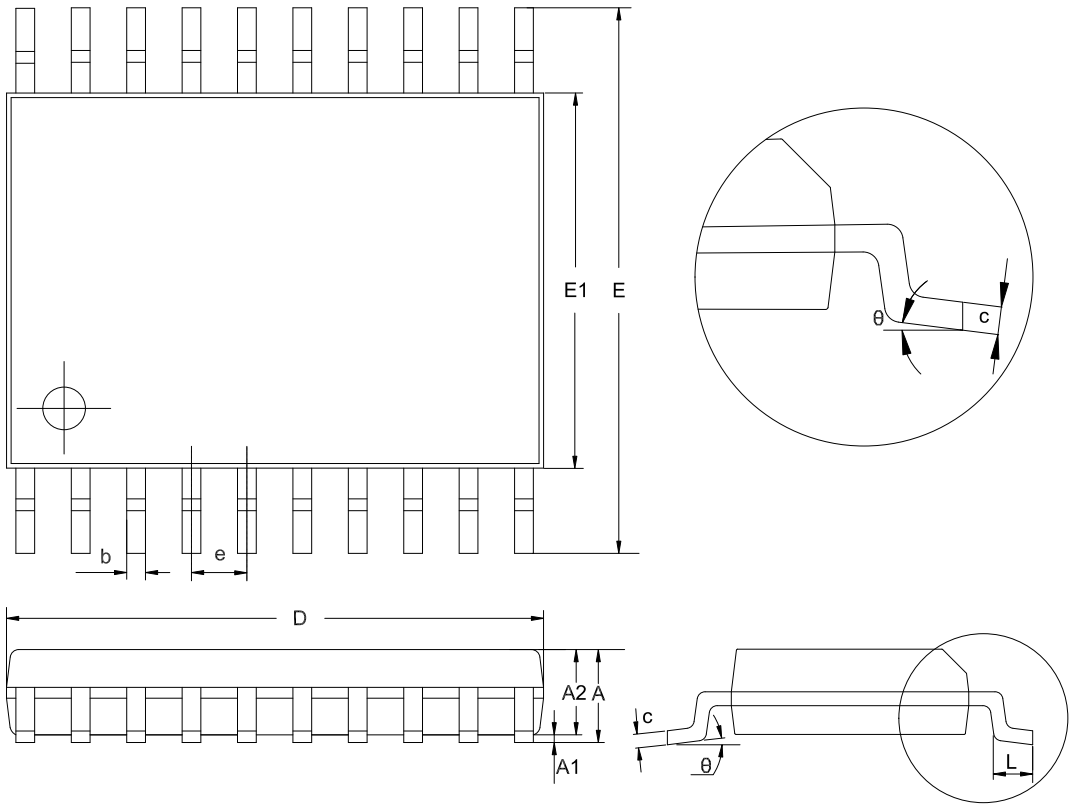


Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
T74L244-TS4R	TSSOP20	330	6.95	1.6	16	20.4	7.1	8.0	Q1

Package Outline Dimensions

TSSOP20

Package Outline Dimensions TS4(TSSOP-20-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	6.400	6.600	0.252	0.260
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
T74L244-TS4R	−40 to 125°C	TSSOP20	LVC244	MSL3	Tape and Reel,4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

IMPORTANT NOTICE AND DISCLAIMER

Trademarks. Any of the 思瑞浦 or 3PEAK trade names, trademarks, graphic marks, and domain names contained in this document /material are the property of 3PEAK. You may NOT reproduce, modify, publish, transmit or distribute any Trademark without the prior written consent of 3PEAK.

Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

Disclaimer. 3PEAK provides technical and reliability data (including data sheets), design resources (including reference designs), application or other design recommendations, networking tools, security information and other resources "As Is". 3PEAK makes no warranty as to the absence of defects, and makes no warranties of any kind, express or implied, including without limitation, implied warranties as to merchantability, fitness for a particular purpose or non-infringement of any third-party's intellectual property rights. Unless otherwise specified in writing, products supplied by 3PEAK are not designed to be used in any life-threatening scenarios, including critical medical applications, automotive safety-critical systems, aviation, aerospace, or any situations where failure could result in bodily harm, loss of life, or significant property damage. 3PEAK disclaims all liability for any such unauthorized use.