Single D-type Flip-Flop with Set and Reset

Features

- Wide Supply Voltage Range from 1.65 V to 5.5 V
- I/O Tolerance Inputs to 5.5 V
- All Inputs with Schmitt-Trigger Action
- CMOS Low Power Dissipation
- I_{OFF} Supports Partial Power-down Protection
- ESD Protection: ±4-kV HBM Model, ±1-kV CDM Model
- Latch-up Performance Exceeds 100 mA per JESD 78, Class II

Applications

- Clock Divider Circuit
- Counter
- Edge Detection

Description

The T74L1G74 is a single positive edge-trigger D-type flip-flop with the V_{CC} supply from 1.65 V to 5.5 V. Schmitt-Trigger action with slower rise-and-fall times and better noise immunity. I_{OFF} circuits can prevent backflow current during power-down, thus supporting partial power-down protection. A LOW level at the $\overline{SD}$ and $\overline{RD}$ to set and reset the output.

The T74L1G74 is available in VSSOP8 and DFN1.4X1-8 packages and is characterized from –40°C to 125°C.

Device Table

Device	Package	Body Size
T74L1G74-VS3R	VSSOP8	2 mm x 2.3 mm
T74L1G74-DFSRR	DFN1.4X1-8	1.4 mm x 1 mm

Typical Application Circuit

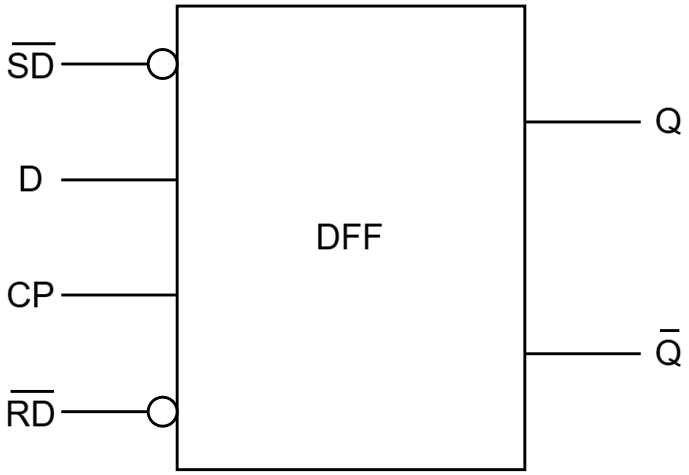


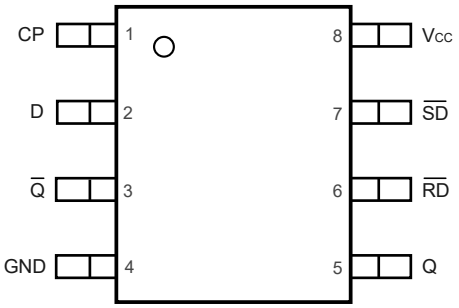
Table of Contents

Revision History

Date	Revision	Notes
2025-07-16	Rev.Pre.0	Initial version.
2026-03-01	Rev.A.0	Released version.

Pin Configuration and Functions

T74L1G74
VSSOP8
Top View



T74L1G74
DFN1.4X1-8
Top View

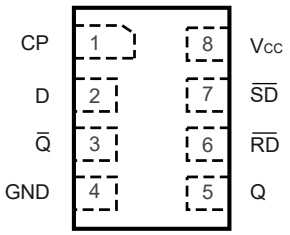


Table 1. Pin Functions

Pin No.	Name	I/O	Description
1	CP	I	Clock input (Positive edge-trigger)
2	D	I	Data input
3	$\overline{Q}$	O	Inverted Flip-flop output
4	GND	Power	Ground
5	Q	O	Flip-flop output
6	$\overline{RD}$	I	Reset direct input (active LOW)
7	$\overline{SD}$	I	Set direct input (active LOW)
8	V_{CC}	Power	Supply pin

Function Table

Table 2. Truth Table

Input				Output			
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$	Q_{n+1}	$\overline{Q}_{n+1}$
L	H	X	X	H	L	-	-
H	L	X	X	L	H	-	-
L	L	X	X	H	H	-	-
H	H	↑	L	-	-	L	H
H	H	↑	H	-	-	H	L

(1) H = High voltage level.
(2) L = Low voltage level.
(3) X = Don't care.
(4) ↑ = Positive edge-trigger clock transition

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	–0.5	6.5	V
V_I	Input Voltage (2)	–0.5	6.5	V
V_O	Output Voltage, in Power-off Mode (2)	–0.5	6.5	V
V_O	Output Voltage, in Active Mode (2)	–0.5	V_{CC} + 0.5	V
I_O	Continuous Output Current	−50	50	mA
I_{IK}	Input Clamp Current, V_I < 0	−50		mA
I_{OK}	Output Clamp Current, V_O < 0	−50		mA
	Continuous Current through V_{CC} or GND	−100	100	mA
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001, all pins (1)	±4,000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002, all pins (2)	±1,000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	1.65		5.5	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage	0		V_{CC}	V
T_A	Ambient Temperature	−40		125	℃
Δt/ΔV	Input Transition Rise-and-Fall Rate, V_{CC} = 1.65 V to 2.7 V			20	ns/V
	Input Transition Rise-and-Fall Rate, V_{CC} = 2.7 V to 5.5 V			10	ns/V

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
VSSOP8	265.6	110.3	°C/W
DFN1.4X1-8	330.2	213.3	°C/W

Electrical Characteristics – DC Parameter

All test conditions: T_A = −40℃ to 125℃, all typical values are measured at T_A = 25℃, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage	V_{CC} = 1.65 V to 1.95 V	0.7V_{CC}			V
		V_{CC} = 2.3 V to 2.7 V	1.7			V
		V_{CC} = 2.7 V to 3.6 V	2			V
		V_{CC} = 4.5 V to 5.5 V	0.7V_{CC}			V
V_{IL}	Low-Level Input Voltage	V_{CC} = 1.65 V to 1.95 V			0.3V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V			0.7	V
		V_{CC} = 2.7 V to 3.6 V			0.8	V
		V_{CC} = 4.5 V to 5.5 V			0.3V_{CC}	V
V_{OH}	High-Level Output Voltage	I_{OH} = −100 μA; V_{CC} = 1.65 V to 5.5 V	V_{CC} − 0.1			V
		I_{OH} = −4 mA; V_{CC} = 1.65 V	0.95			V
		I_{OH} = −8 mA; V_{CC} = 2.3 V	1.7			V
		I_{OH} = −12 mA; V_{CC} = 2.7 V	1.9			V
		I_{OH} = −24 mA; V_{CC} = 3 V	2			V
		I_{OH} = −32 mA; V_{CC} = 4.5 V	3.4			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 100 μA; V_{CC} = 1.65 V to 5.5 V			0.1	V
		I_{OL} = 4 mA; V_{CC} = 1.65 V			0.7	V
		I_{OL} = 8 mA; V_{CC} = 2.3 V			0.45	V
		I_{OL} = 12 mA; V_{CC} = 2.7 V			0.6	V
		I_{OL} = 24 mA; V_{CC} = 3 V			0.8	V
		I_{OL} = 32 mA; V_{CC} = 4.5 V			0.8	V
I_I	Input Leakage Current	V_I = GND or 5.5 V; V_{CC} = 0 V to 5.5 V	−1	±0.1	1	μA
I_{OFF}	Power-off Leakage Current	V_I or V_O = 5.5 V; V_{CC} = 0 V	−1	±0.1	1	μA
I_{CC}	Supply Current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 1.65 V to 5.5 V		0.1	2	μA
ΔI_{CC}	Additional Supply Current	V_I = V_{CC} − 0.6 V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V		0.1	10	μA
C_I (1)	Input Capacitance			2.1		pF

(1) Spec limit is based on bench characterization and design simulation, not tested in production.

Electrical Characteristics – AC Parameter

All test conditions: T_A = −40℃ to 125℃, all typical values are measured at T_A = 25℃, unless otherwise noted.

Symbol (1)	Parameter	Conditions	Min	Typ	Max	Unit
t_{PD} (2)	Propagation Delay	CP to Q, $\overline{Q}$				
		C_{LOAD} = 15 pF; V_{CC} = 1.65 V to 1.95 V	2.7	10.1	15.2	ns
		C_{LOAD} = 15 pF; V_{CC} = 2.3 V to 2.7 V	1.6	6.4	9.1	ns
		C_{LOAD} = 15 pF; V_{CC} = 2.7 V	2	6.2	8.7	ns
		C_{LOAD} = 50 pF; V_{CC} = 3 V to 3.6 V	1.6	5.3	8.1	ns
		C_{LOAD} = 50 pF; V_{CC} = 4.5 V to 5.5 V	1.2	4.2	6.5	ns
		$\overline{SD}$,$\overline{RD}$ to Q, $\overline{Q}$				
		C_{LOAD} = 15 pF; V_{CC} = 1.65 V to 1.95 V	5.8	11	24.5	ns
		C_{LOAD} = 15 pF; V_{CC} = 2.3 V to 2.7 V	3.8	7.2	14.5	ns
		C_{LOAD} = 15 pF; V_{CC} = 2.7 V	4.1	6.9	12.9	ns
		C_{LOAD} = 50 pF; V_{CC} = 3 V to 3.6 V	3.2	5.9	11.7	ns
		C_{LOAD} = 50 pF; V_{CC} = 4.5 V to 5.5 V	2.5	4.9	8.8	ns
f_{max}	Maximum Frequency	V_{CC} = 1.65 V to 1.95 V			70	MHz
		V_{CC} = 2.3 V to 2.7 V			130	MHz
		V_{CC} = 2.7 V			160	MHz
		V_{CC} = 3 V to 3.6 V			170	MHz
		V_{CC} = 4.5 V to 5.5 V			190	MHz
t_w	Pulse Width	CP HIGH or LOW; $\overline{SD}$, $\overline{RD}$ LOW				
		V_{CC} = 1.65 V to 1.95 V	7.2			ns
		V_{CC} = 2.3 V to 2.7 V	3.9			ns
		V_{CC} = 2.7 V	3.2			ns
		V_{CC} = 3 V to 3.6 V	3			ns
		V_{CC} = 4.5 V to 5.5 V	2.7			ns
t_{su}	Setup Time	D to CP				
		V_{CC} = 1.65 V to 1.95 V	5.9			ns

Symbol (1)	Parameter	Conditions	Min	Typ	Max	Unit
		V_{CC} = 2.3 V to 2.7 V	3.7			ns
		V_{CC} = 2.7 V	3.7			ns
		V_{CC} = 3 V to 3.6 V	3.3			ns
		V_{CC} = 4.5 V to 5.5 V	3.1			ns
t_h	Hold Time	D to CP				
		V_{CC} = 1.65 V to 1.95 V	2.5			ns
		V_{CC} = 2.3 V to 2.7 V	2			ns
		V_{CC} = 2.7 V	2			ns
		V_{CC} = 3 V to 3.6 V	2			ns
		V_{CC} = 4.5 V to 5.5 V	2			ns
t_{rec}	Recovery Time	$\overline{RD}$ to CP				
		V_{CC} = 1.65 V to 1.95 V	2.9			ns
		V_{CC} = 2.3 V to 2.7 V	2.4			ns
		V_{CC} = 2.7 V	2.3			ns
		V_{CC} = 3 V to 3.6 V	2.2			ns
		V_{CC} = 4.5 V to 5.5 V	2			ns
C_{PD} (3)	Power Dissipation Capacitance	f = 10 MHz; V_I = GND to V_{CC}		13		pF

(1) Spec limit is based on bench characterization and design simulation, not tested in production.

(2) t_{PD} is the same as t_{PLH} and t_{PHL}.

(3) C_{PD} is used to determine the dynamic power dissipation (PD in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$

Where:

f_i = Input frequency in MHz;

f_o = Output frequency in MHz;

C_L = Output load capacitance in pF;

V_{CC} = Supply voltage in Volts;

N = Number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of the outputs.

Parameter Measurement Waveforms

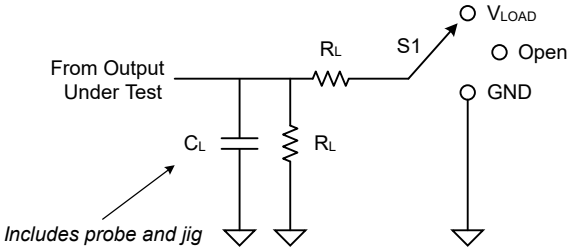


Figure 1. Timing Measurement Load Circuit

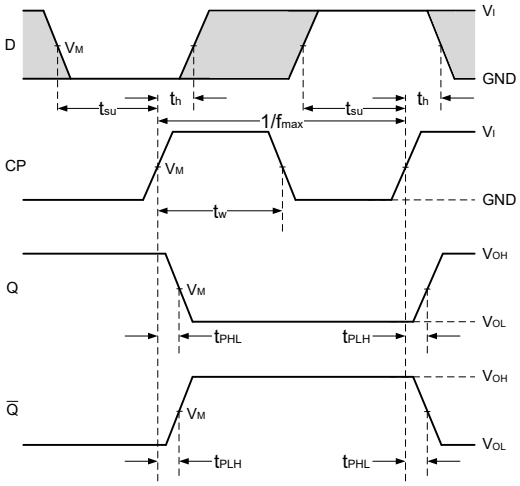


Figure 2. Clock Propagation Delay Times

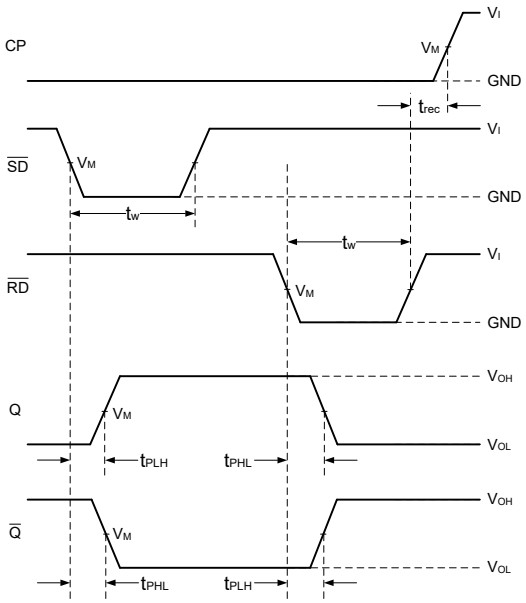


Figure 3. Set and Reset Propagation Delay Times

Table 3. Test Data

V_{CC}	Inputs		C_L	R_L	V_M	S1
	V_I	t_r/t_f				t_{PHL}/t_{PLH}
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	$0.5V_{CC}$	Open
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	$0.5V_{CC}$	Open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	1.5 V	Open
3 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	1.5 V	Open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	$0.5V_{CC}$	Open

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

Figure 4 shows the functional block diagram.

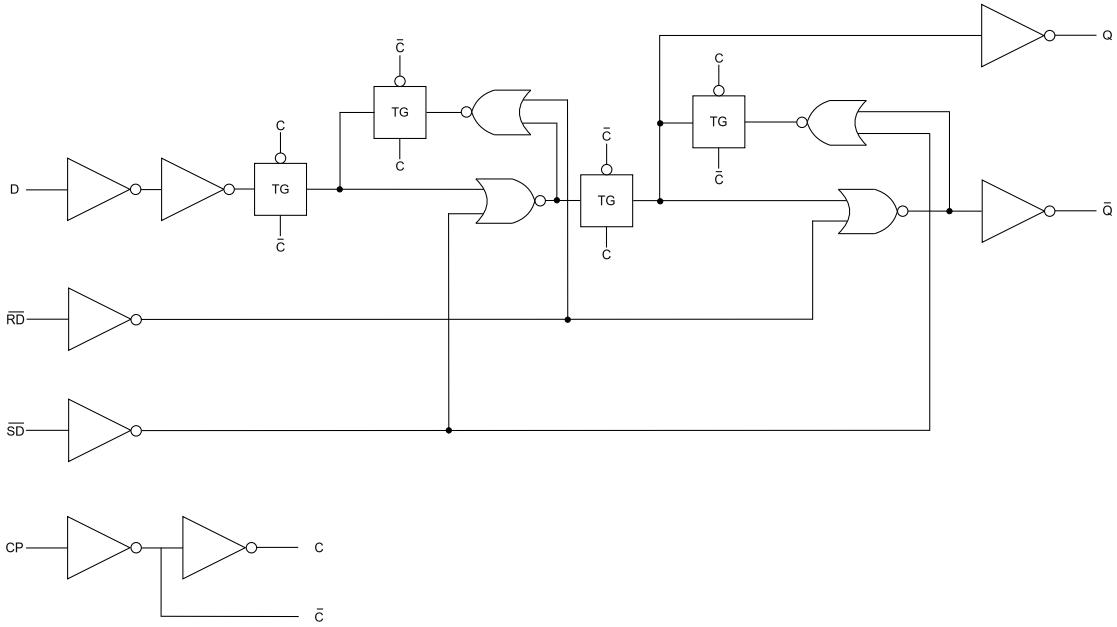
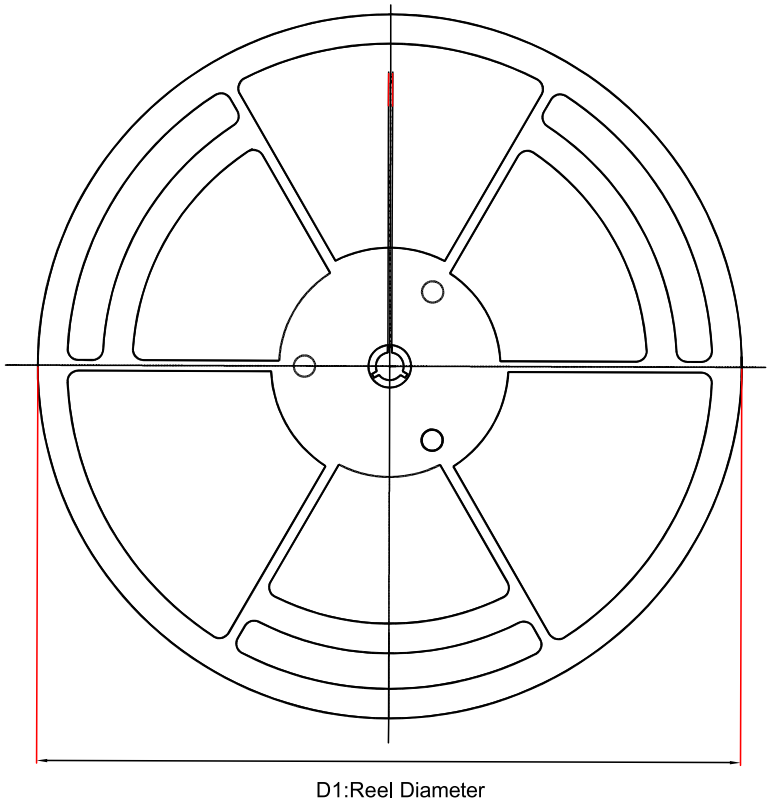
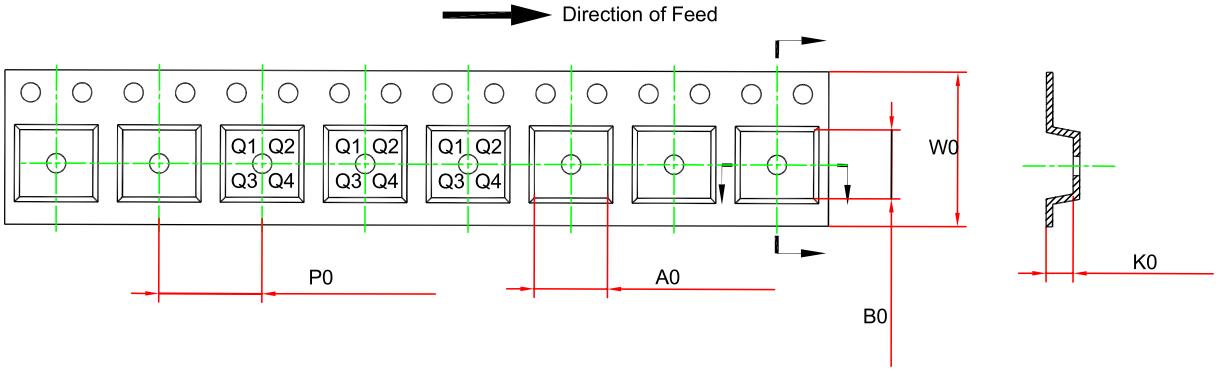


Figure 4. Functional Block Diagram

Tape and Reel Information



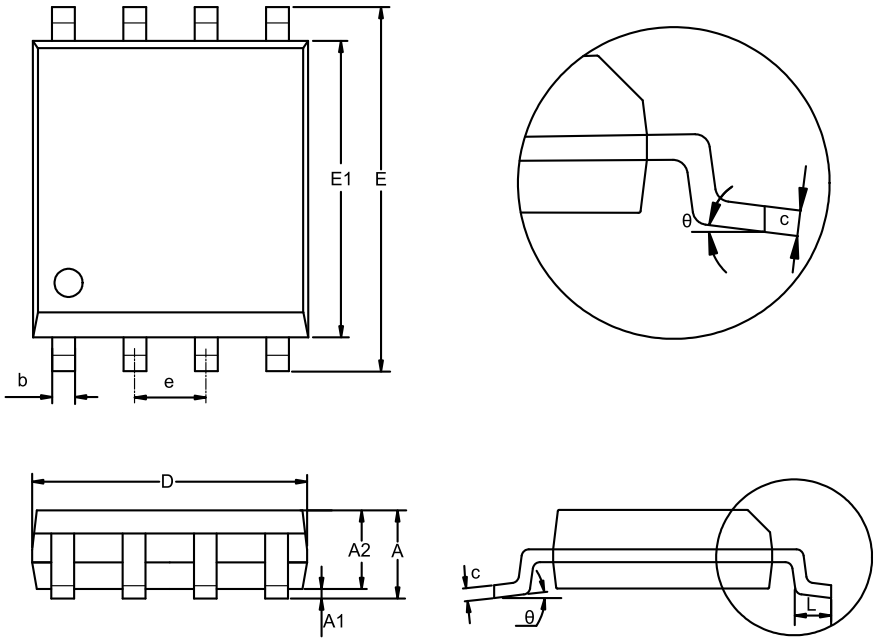


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
T74L1G74-VS3R	VSSOP8	178	11.4	2.25	3.35	1.05	4	8	Q3
T74L1G74-DFSRR	DFN1.4X1-8	180	13.1	1.15	1.6	0.5	4	8	Q1

Package Outline Dimensions

VSSOP8

Package Outline Dimensions VS3(VSSOP-8-A)



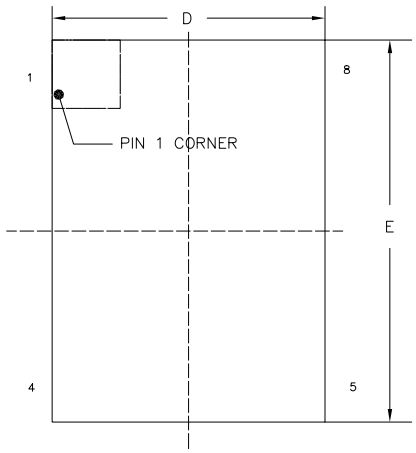
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	1.000	0.028	0.039
A1	0.000	0.150	0.000	0.006
A2	0.600	0.850	0.024	0.033
b	0.170	0.270	0.007	0.011
c	0.080	0.230	0.003	0.009
D	1.900	2.100	0.075	0.083
E	3.000	3.200	0.118	0.126
E1	2.200	2.400	0.087	0.094
e	0.500 BSC		0.020 BSC	
L	0.150	0.400	0.006	0.016
θ	0	8°	0	8°

NOTES

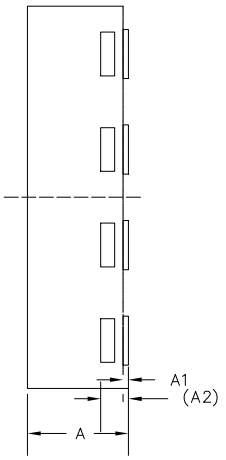
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

DFN1.4X1-8

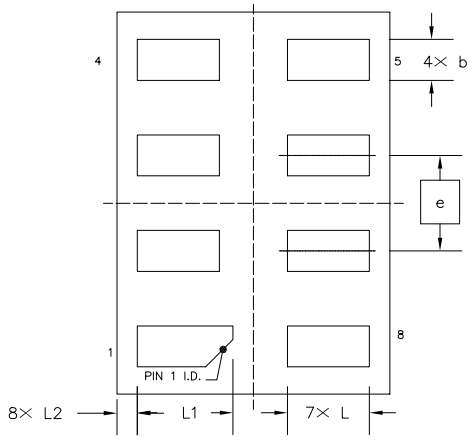
Package Outline Dimensions DFSR(DFN1.4X1-8-B)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

NOTES

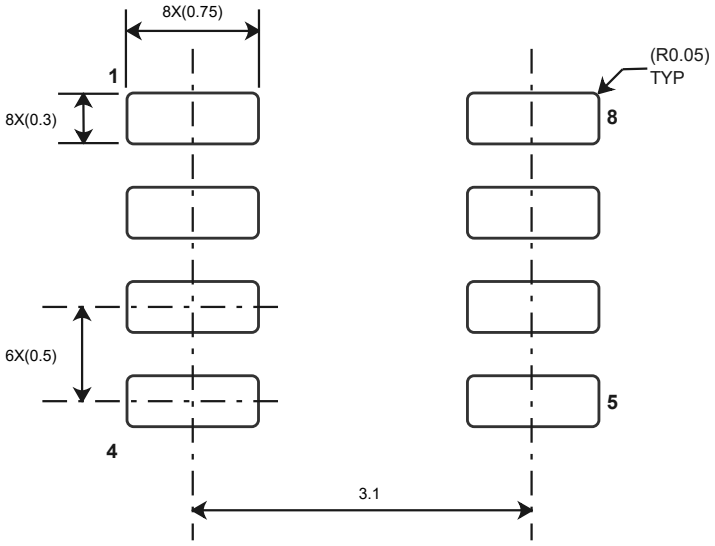
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.320	0.400	0.013	0.016
A1	0.000	0.050	0.000	0.002
A2	0.102 REF		0.004 REF	
b	0.100	0.200	0.004	0.008
D	1.000 BSC		0.039 BSC	
E	1.400 BSC		0.055 BSC	
e	0.350 BSC		0.014 BSC	
L	0.250	0.350	0.010	0.014
L1	0.300	0.400	0.011	0.016
L2	0.075 REF		0.003 REF	

Land Pattern

VSSOP8

EXAMPLE BOARD LAYOUT **VSSOP8**

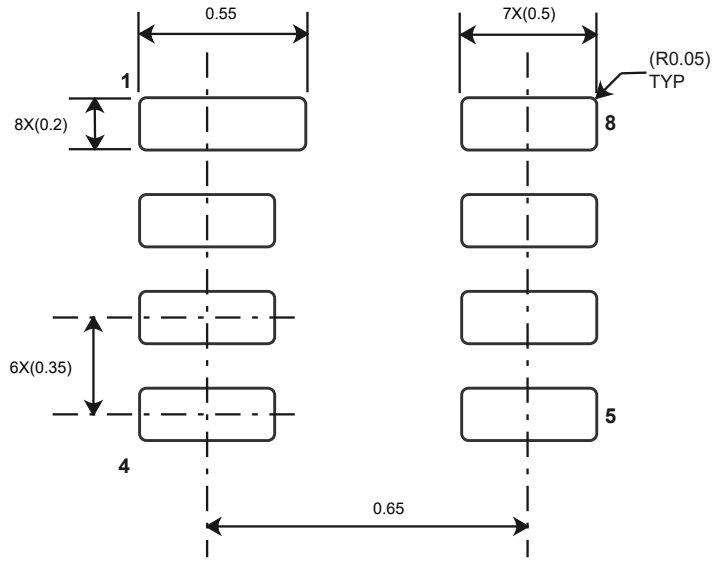


LAND PATTERN EXAMPLE

NOTES
1.All dimensions are in millimeters.
2.This drawing is for design reference only.
3.This drawing is subject to change without notice.

DFN1.4X1-8

EXAMPLE BOARD LAYOUT — DFN1.4X1-8



LAND PATTERN EXAMPLE

NOTES
1.All dimensions are in millimeters.
2.This drawing is for design reference only.
3.This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
T74L1G74-VS3R	−40 to 125℃	VSSOP8	V74	MSL3	Tape and Reel,3000	Green
T74L1G74-DFSRR	−40 to 125℃	DFN1.4X1-8	Y4	MSL3	Tape and Reel,4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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