

Features

- Used as Two 4-bit Buffers or One 8-bit Buffer
- Supply Voltage: 1.65 V to 5.5 V
- ESD Protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 Class 3B Exceeds 8000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 Class C3 Exceeds 1000 V
- Latch-up Performance Exceeds 100 mA Per JESD 78 Class II
- Specified from -40 °C to +125 °C

Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer Handsets
- Industrial Automation

Description

The T74A244 can be configured as two 4-bit buffers or one 8-bit buffer, featuring two output enable pins ($\overline{1OE}$ and $\overline{2OE}$), each controlling four of the 3-state outputs. A high level on $n\overline{OE}$ (where n denotes 1 or 2) forces the outputs into a high-impedance state.

The T74A244 is available in the TSSOP20 package and is characterized from -40°C to +125°C.

Typical Application

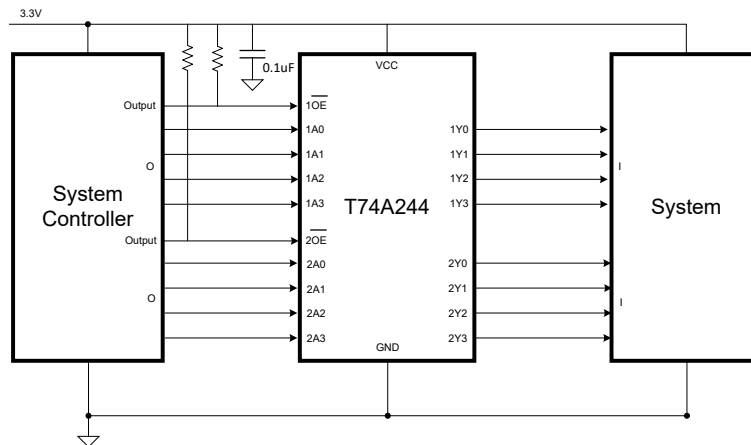


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Revision History

Date	Revision	Notes
2025-06-16	Rev.P.0	Initial version
2026-01-22	Rev.A.0	Release version

Pin Configuration and Functions

T74A244-TS4R
TSSOP-20
Top View

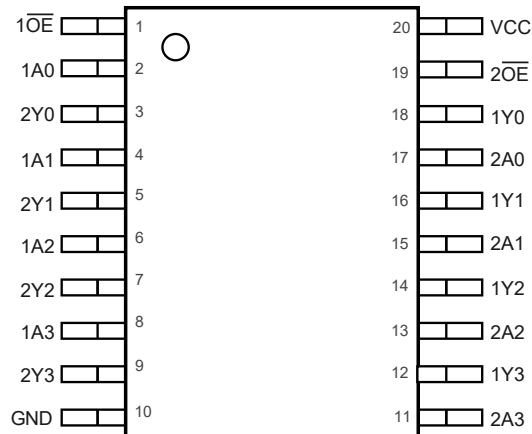


Table 1. Pin Functions: T74A244-TS4R

Pin		I/O	Description
No.	Name		
1	1 \overline{OE}	I	Active-low Enable Input
2	1A0	I	Input 1A0
3	2Y0	O	Output 2Y0
4	1A1	I	Input 1A1
5	2Y1	O	Output 2Y1
6	1A2	I	Input 1A2
7	2Y2	O	Output 2Y2
8	1A3	I	Input 1A3
9	2Y3	O	Output 2Y3
10	GND	P	Supply Ground
11	2A3	I	Input 2A3
12	1Y3	I	Output 1Y3
13	2A2	I	Input 2A2
14	1Y2	O	Output 1Y2
15	2A1	I	Input 2A1
16	1Y1	O	Output 1Y1
17	2A0	I	Input 2A0
18	1Y0	O	Output 1Y0
19	2 \overline{OE}	I	Active-low Enable Input

Octal Buffer Driver; 3-state

Pin		I/O	Description
No.	Name		
20	VCC	P	Supply Power

Specifications

Absolute Maximum Ratings ⁽¹⁾

Parameter		Min	Max	Unit
V _{CC}	DC Reference Voltage Range	-0.5	7	V
V _I	Input Voltage	-0.5	7	V
V _O	Output Voltage	-0.5	V _{CC} + 0.5	V
I _{IK}	Input Clamp Current, V _I < 0	-20		mA
I _{OK}	Output Clamp Current, V _O < 0 or V _I > V _{CC}	-20	20	mA
I _O	Output Current, V _O = 0 V or V _{CC}	-25	25	mA
I _{CC}	Continuous Current through V _{CC}		75	mA
I _{GND}	Continuous Current through GND	-75		mA
P _{tot}	Total Power Dissipation		500.0	mW
T _{STG}	Storage Temperature Range	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the recommended operating conditions table.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 class 3B (1)	±8	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 class C3 (2)	±1	kV
LU	Latch up	JESD 78 Class II	±100	mA

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Conditions	Min	Max	Unit
V _{CC}	Supply Voltage		1.65	5.5	V
V _I	Input Voltage		0	5.5	V
V _O	Output Voltage		0	V _{CC}	V
T _{amb}	Operation Free-air Temperature		-40	125	°C
Δt/ΔV	Input Transition Rise and Fall Rate	V _{CC} = 3.3 V ± 0.3 V		100	ns/V
		V _{CC} = 5 V ± 0.5 V		20	ns/V

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP20	99.9	61.7	°C/W

Electrical Characteristics

All test conditions : $T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$, unless otherwise.

Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	Input Logic High	$V_{CC} = 2.0\text{ V}$	1.5			V
		$V_{CC} = 3.0\text{ V}$	2.1			V
		$V_{CC} = 5.5\text{ V}$	2.9			V
V_{IL}	Input Logic Low	$V_{CC} = 2.0\text{ V}$			0.5	V
		$V_{CC} = 3.0\text{ V}$			0.9	V
		$V_{CC} = 5.5\text{ V}$			1.65	V
V_{OH}	High-level Output Voltage	$I_O = -50\text{ }\mu\text{A}$, $V_{CC} = 2.0\text{ V}$	1.9			V
		$I_O = -50\text{ }\mu\text{A}$, $V_{CC} = 3.0\text{ V}$	2.9			V
		$I_O = -50\text{ }\mu\text{A}$, $V_{CC} = 4.5\text{ V}$	4.4			V
		$I_O = -4.0\text{ mA}$, $V_{CC} = 3.0\text{ V}$	2.4			V
		$I_O = -8.0\text{ mA}$, $V_{CC} = 4.5\text{ V}$	3.7			V
V_{OL}	Low-level Output Voltage	$I_O = 50\text{ }\mu\text{A}$, $V_{CC} = 2.0\text{ V}$			0.1	V
		$I_O = 50\text{ }\mu\text{A}$, $V_{CC} = 3.0\text{ V}$			0.1	V
		$I_O = 50\text{ }\mu\text{A}$, $V_{CC} = 4.5\text{ V}$			0.1	V
		$I_O = 4.0\text{ mA}$, $V_{CC} = 3.0\text{ V}$			0.55	V
		$I_O = 8.0\text{ mA}$, $V_{CC} = 4.5\text{ V}$			0.55	V
I_i	Input Leakage Current	$V_I = 0\text{ V}$ to 5.5 V , $V_{CC} = 0\text{ V}$ to 5.5 V	-2.0		2.0	μA
I_{OZ}	OFF-state Output Current	$V_I = V_{IH}$ or V_{IL} , $V_O = V_{CC}$ or GND , $V_{CC} = 5.5\text{ V}$	-10.0		10.0	μA
I_{OFF}	Power-off Leakage Current	V_I or $V_O = 5.5\text{ V}$, $V_{CC} = 0\text{ V}$	-10.0		10.0	μA
I_{CC}	Supply Current	$V_I = \text{GND}$ or V_{CC} , $I_O = 0\text{ A}$, $V_{CC} = 5.5\text{ V}$			80.0	μA
$C_i^{(1)(2)}$	Input Capacitance	$V_I = V_{CC}$ or GND		6		pF
$C_o^{(1)(2)}$	Output Capacitance	$V_O = V_{CC}$ or GND		6.8		pF

(1) Test data based on bench tests and design simulation, NOT test in production.

(2) $T_A = 25\text{ }^\circ\text{C}$.

AC Timing Requirements

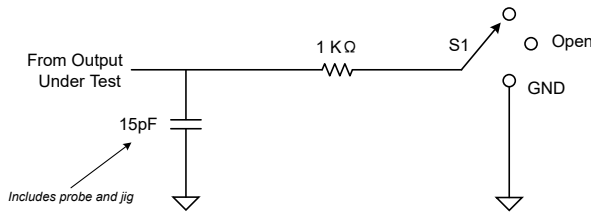
All test conditions: $T_A = -40^{\circ}\text{C}$ to 125°C , the data is based on bench test and design simulation, not test in production, unless otherwise noted.

t_{en} includes t_{PZL} and t_{PHL} , t_{dis} includes t_{PLZ} and t_{PHZ} .

Parameter		Conditions	Min	Typ	Max	Unit
t_{pd}	Propagation Delay	$C_{load} = 15 \text{ pF}, V_{CC} = 3.0 \text{ V} \pm 0.3 \text{ V}$			10.5	ns
		$C_{load} = 50 \text{ pF}, V_{CC} = 3.0 \text{ V} \pm 0.3 \text{ V}$			15.0	ns
		$C_{load} = 15 \text{ pF}, V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$			7.0	ns
		$C_{load} = 50 \text{ pF}, V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$			9.5	ns
t_{en}	Enable Time	$C_{load} = 15 \text{ pF}, V_{CC} = 3.0 \text{ V} \pm 0.3 \text{ V}$			13.5	ns
		$C_{load} = 50 \text{ pF}, V_{CC} = 3.0 \text{ V} \pm 0.3 \text{ V}$			18.0	ns
		$C_{load} = 15 \text{ pF}, V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$			9.5	ns
		$C_{load} = 50 \text{ pF}, V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$			12.0	ns
t_{en}	Disable Time	$C_{load} = 30 \text{ pF}, V_{CC} = 3.0 \text{ V} \pm 0.3 \text{ V}$			12.5	ns
		$C_{load} = 30 \text{ pF}, V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$			17.5	ns
		$C_{load} = 50 \text{ pF}, V_{CC} = 3.0 \text{ V} \pm 0.3 \text{ V}$			9.0	ns
		$C_{load} = 50 \text{ pF}, V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$			11.5	ns
$C_{PD}^{(1)}$	Power Dissipation Capacitance	$f_i = 1 \text{ MHz}, V_i = \text{GND to } V_{CC}$		11.0		pF

(1) $T_A = 25^{\circ}\text{C}$.

Parameter Measurement Waveforms



Test	S1
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	Vcc
t_{PHZ} / t_{PZH}	GND
Open Drain	Vcc

Figure 1. Test Circuit for Measuring Switching Times

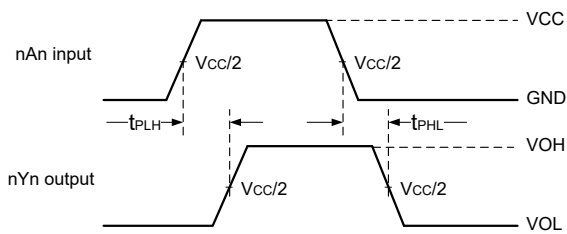


Figure 2. Propagation Delay Input To Output

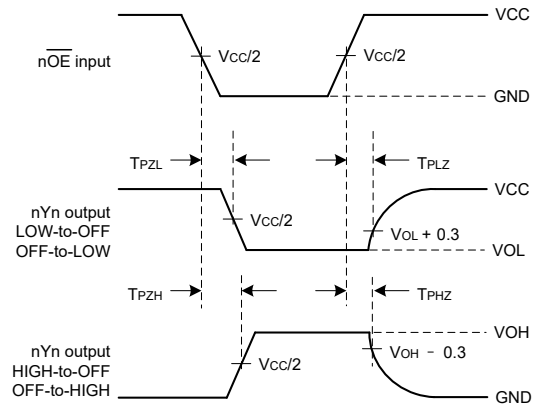


Figure 3. Enable and Disable Times

Detailed Description

Overview

The T74A244 device consists of two independent 4-bit buffers/line drivers, each with its own output-enable input.

- When \overline{OE} is low, the device transmits data from the A inputs to the Y outputs.
- When \overline{OE} is high, the outputs enter a high-impedance state.

To ensure the high-impedance state is maintained during power-up or power-down, \overline{OE} should be connected to V_{CC} through a pull-up resistor. The minimum resistor value is determined by the driver's current-sinking capability.

Functional Block Diagram

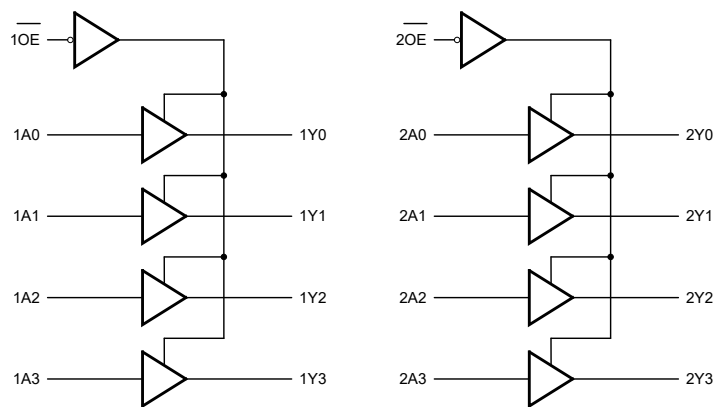


Figure 4. Functional Block Diagram

Feature Description

I_{off} Feature

The I_{off} feature ensures safe operation when the chip is powered down ($V_{CC} = 0\text{ V}$). It automatically disables all outputs in a high-impedance state, preventing any damaging backflow current from flowing through the unpowered device. This allows the bus to remain active while protecting both the chip and connected components.

Enable (\overline{OE})

The output enable (\overline{OE}) is a critical chip function that manages output states. When \overline{OE} is high, all output ports enter a high-impedance state, when \overline{OE} is low, the chip operates normally.

Table 2. Device Function Table

V_{CC}	Input \overline{OE}	Input A	Output Y
1.65 V to 5 V	L	H	H
1.65 V to 5 V	L	L	L
1.65 V to 5 V	H	X	ALL Outputs Hi-Z
0 V	X	X	ALL Outputs Hi-Z

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The T74A244 can be configured as two 4-bit buffers or one 8-bit buffer, featuring two output enable pins ($\overline{1OE}$ and $\overline{2OE}$), each controlling four of the 3-state outputs. A high level on $n\overline{OE}$ (where n denotes 1 or 2) forces the outputs into a high-impedance state.

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer Handsets
- Industrial Automation

Typical Application

A typical application is shown in [Figure 5](#).

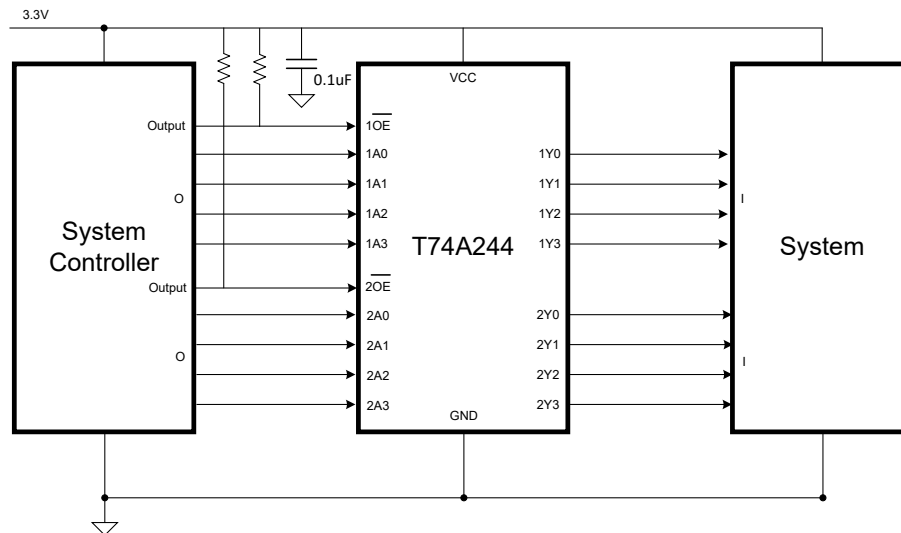


Figure 5. Typical Application Circuit

Layout

Layout Example

Reflections and matching are closely related to loop antenna theory but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in the width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they have to turn corners. Below are progressively better techniques for rounding corners. Only the last example (BEST) maintains a constant trace width and minimizes reflections.

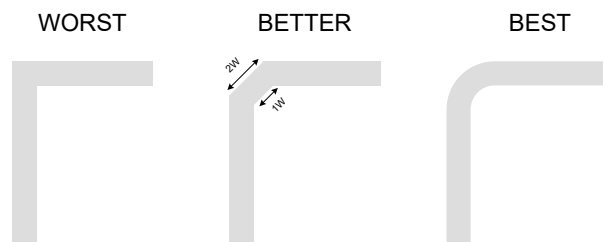


Figure 6. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

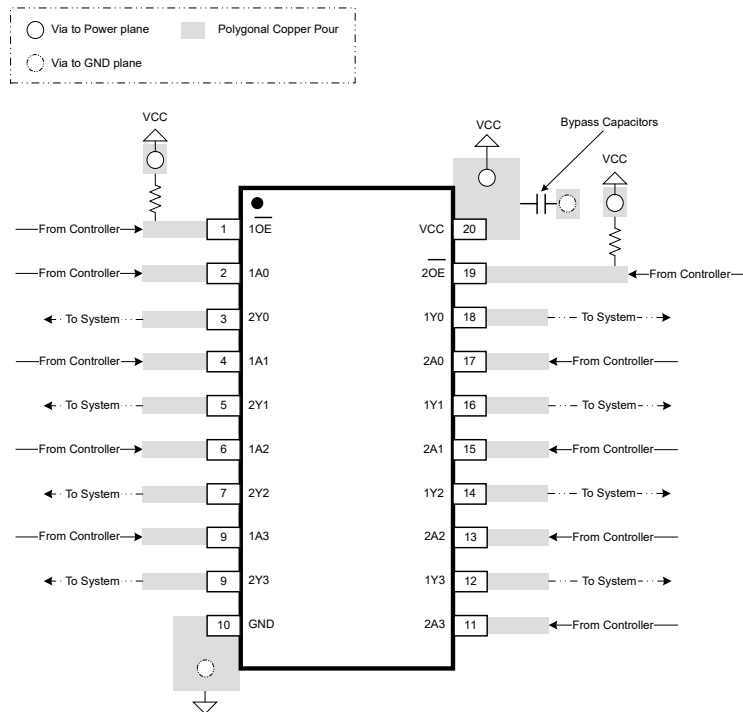
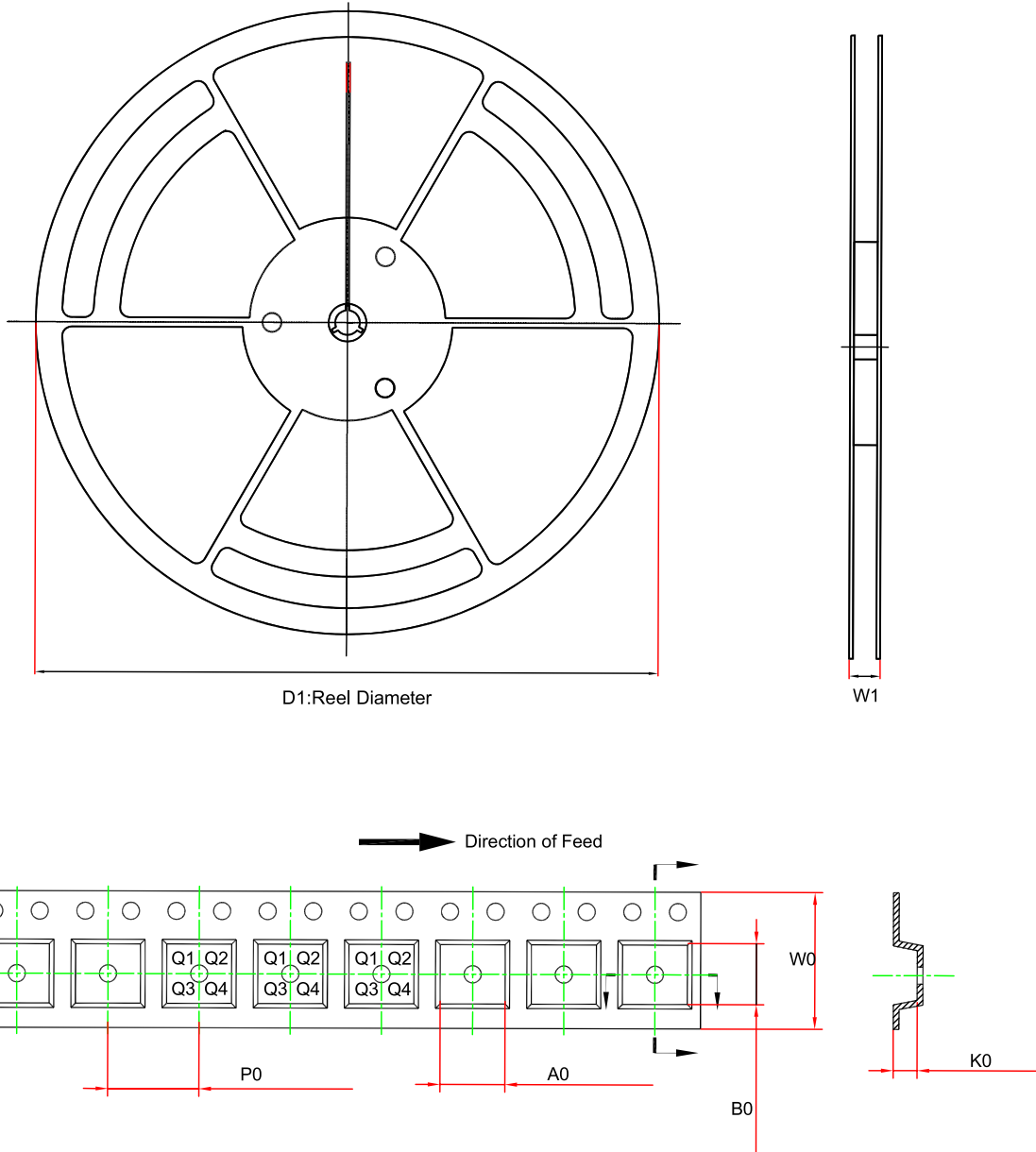
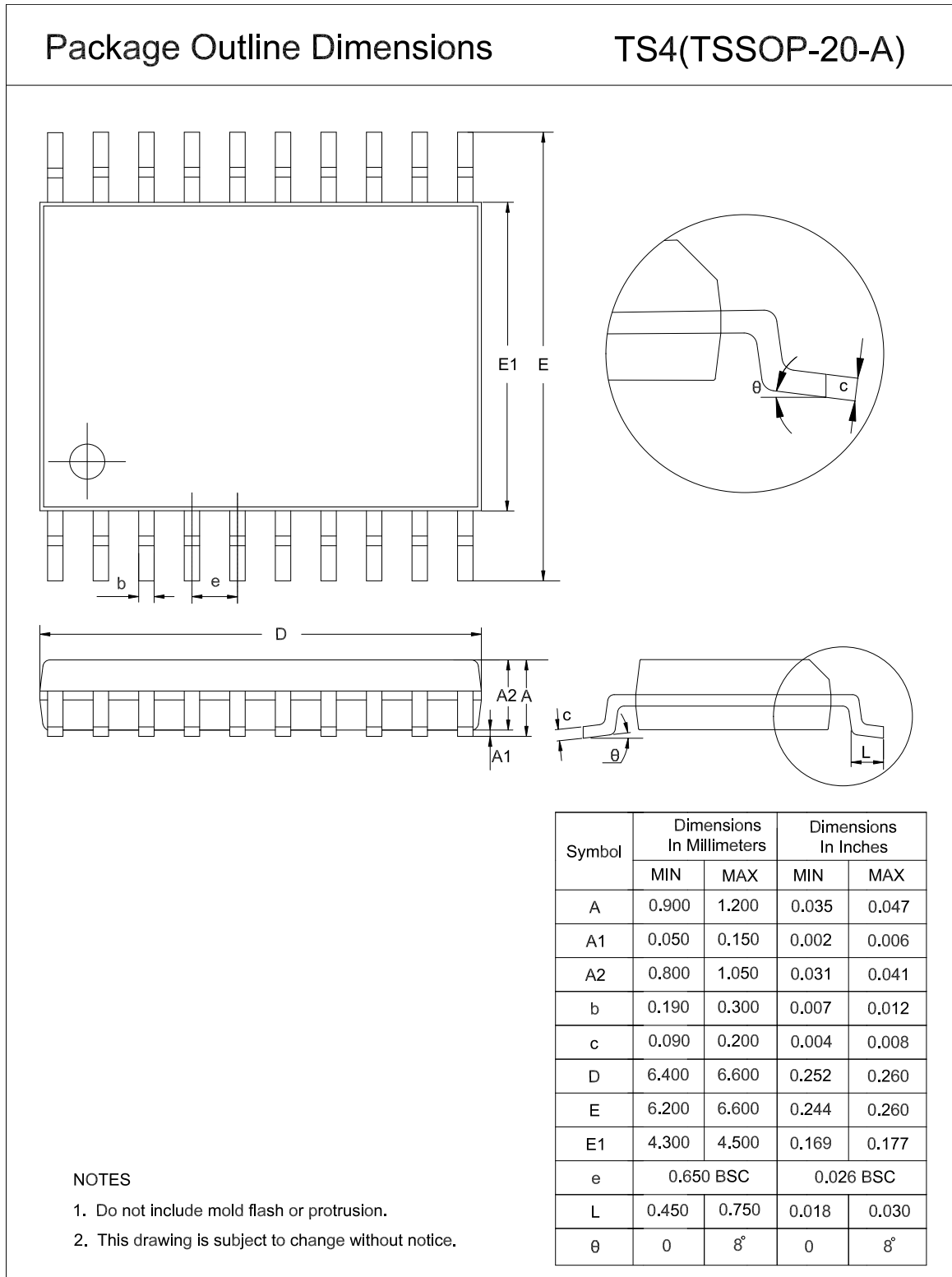


Figure 7. Layout Example

Tape and Reel Information



Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
T74A244-TS4R	TSSOP20	330	6.95	1.6	16	20.4	7.1	8.0	Q1

Package Outline Dimensions
TSSOP20


Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
T74A244-TS4R	-40 to 125°C	TSSOP20	AHC244	MSL3	Tape and Reel,4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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