8-Bit CMOS Digital-to-Analog Converter

Features

- 125-MSPS Update Rate
- 8-Bit Resolution
- Linearity:
  - DNL: 1/4 LSB
  - INL: 1/4 LSB
- Differential Current Outputs
- SINAD @ 5-MHz Output: 50 dB
- Power Dissipation: 175 mW @ 5 V to 45 mW @ 3 V
- Power-down Mode: 20 mW @ 5 V
- On-Chip 1.10-V Reference
- Single-Supply Operation: +5 V or +3 V
- Package: TSSOP28
- Edge-Triggered Latches
- Fast Settling: 35-ns Full-Scale Settling to 0.1%

Applications

- Communications
- Signal Reconstruction
- Instrumentation
- Video Re-Construction

Highlights

- Manufactured on a CMOS process, the 3PD9708(E) uses a proprietary switching technique that enhances dynamic performance well beyond 8- and 10-bit video DACs.
- The on-chip, edge-triggered input CMOS latches readily the interface to 3-V and 5-V CMOS logic families. The 3PD9708(E) supports update rates up to 125 MSPS.
- A flexible single-supply operating range from +2.7 V to +5.5 V and a wide full-scale current adjustment span from 2 mA to 20 mA allows the 3PD9708(E) to operate at reduced power levels (i.e., 45 mW) without any degradation in dynamic performance.
- A temperature-compensated, 1.10-V bandgap reference is included on-chip providing a complete DAC solution. An external reference may be used.
- The current output(s) of the 3PD9708(E) can easily be configured for various single-ended or differential applications.

Description

The 3PD9708(E) offers exceptional AC and DC performance while supporting update rates up to 125 MSPS. Its flexible single-supply operating range from +2.7 V to +5.5 V and low power dissipation are well suited for portable and low-power applications. Its power dissipation can be reduced to 45 mW, without a significant degradation in performance, by lowering the full-scale current output. In addition, a power-down mode reduces the standby power dissipation to approximately 20 mW.

The 3PD9708(E) is manufactured on an advanced CMOS process. A segmented current source architecture is combined with a proprietary switching technique to reduce spurious components and enhance dynamic performance. The edge-triggered input latches, and a temperature-compensated bandgap reference is integrated to provide a complete monolithic DAC solution. Flexible supply options support 3-V and 5-V CMOS logic families.

The 3PD9708(E) is a current-output DAC with a nominal full-scale output current of 20 mA and an output impedance of > 100 kΩ.

Differential current outputs are provided to support single-ended or differential applications. The current outputs may be directly tied to an output resistor to provide two complementary, single-ended voltage outputs. The output voltage compliance range is 1.25 V. The 3PD9708(E) contains a 1.1-V on-chip reference and a reference control amplifier, which allows the full-scale output current to be simply set by a single resistor. The 3PD9708(E) can be driven by a variety of external reference voltages.

The full-scale current of the 3PD9708(E) can be adjusted over the range from 2 mA to 20 mA without any degradation in dynamic performance. Thus, the 3PD9708(E) may operate at reduced power levels or be adjusted over a 20-dB range to provide additional gain ranging capabilities. The 3PD9708(E) is available in the TSSOP28 package. It is specified for operation over the industrial temperature range.

Typical Application Circuit

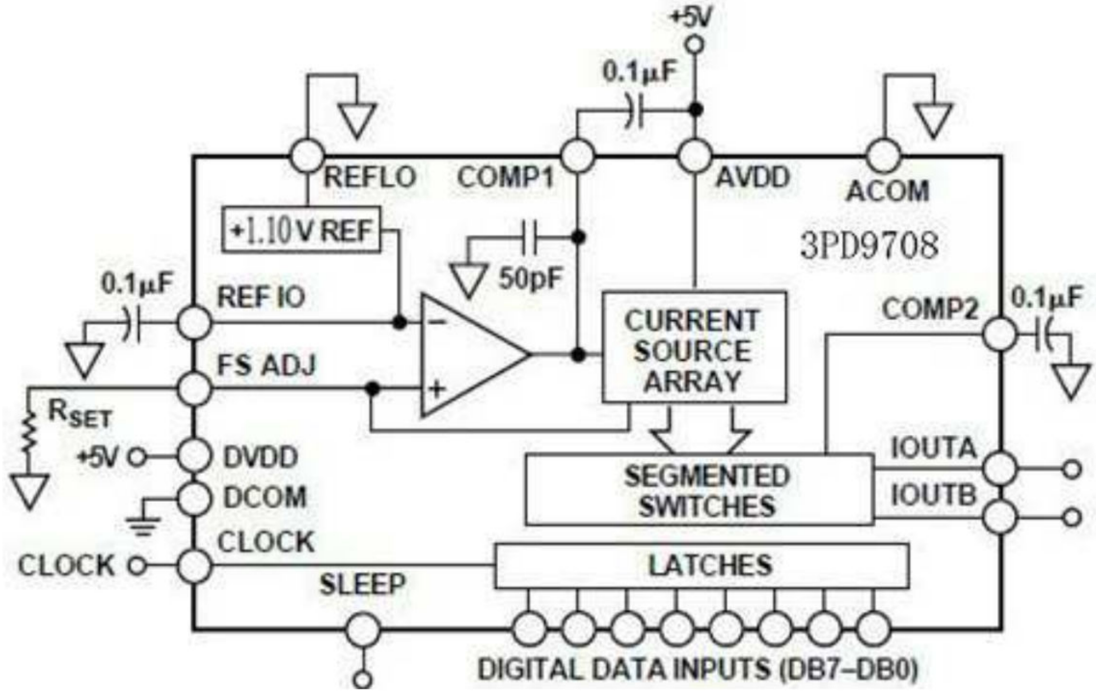


Table of Contents

Revision History

Date	Revision	Notes
2024-12-30	Rev.A.1	Updated to a new datasheet format. Updated the Thermal Information. Added the Tape and Reel Information.

Pin Configuration and Functions

3PD9708(E)
TSSOP28
Top View

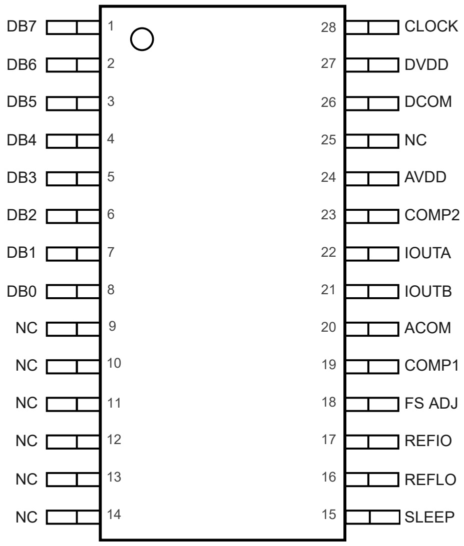


Table 1. Pin Functions

Pin No.	Name	Description
1	DB7	Most significant data bit (MSB).
2-9	DB6-DB1	Data bits 1-6.
10	DB0	Least significant data bit (LSB).
11-14, 25	NC	No internal connection.
15	SLEEP	Power-down control input. Active high. Contain a active pull-down circuit, thus may be left unterminated if not used.
16	REFLO	Reference ground when using a 1.1-V internal reference. Connect to AVDD to disable the internal reference.
17	REFIO	Reference input/output. Serve as a reference input when the internal reference is disabled (i.e., tie REFLO to AVDD). Serve as a 1.1-V reference output when the internal reference is activated (i.e., tie REFLO to ACOM). Require a 0.1-F capacitor to ACOM when the internal reference is activated.
18	FS ADJ	Full-scale current output adjust.
19	COMP1	Bandwidth/noise reduction node. Add 0.1 F to AVDD for optimum performance.
20	ACOM	Analog common.
21	IOUTB	Complementary DAC current output. Full-scale current when all data bits are 0 s.
22	IOUTA	DAC current output. Full-scale current when all data bits are 1 s.
23	COMP2	Internal bias node for the switch driver circuitry. Decouple to ACOM with a 0.1-F capacitor.
24	AVDD	Analog supply voltage (+2.7 V to+5.5 V).

Pin No.	Name	Description
26	DCOM	Digital common.
27	DVDD	Digital supply voltage (+2.7 V to+5.5 V).
28	CLOCK	Clock input. Data latched on the negative edge of the clock of the 3PD9708, and the positive edge of the clock of the 3PD9708E.

Specifications

Absolute Maximum Ratings (1)

Parameter		With Respect to	Min	Max	Unit
	AVDD	ACOM	–0.3	6.5	V
	DVDD	DCOM	–0.3	6.5	V
	ACOM	DCOM	–0.3	0.3	V
	AVDD	DVDD	−6.5	6.5	V
	CLOCK, SLEEP	DCOM	–0.3	DVDD + 0.3	V
	Digital Inputs	DCOM	–0.3	DVDD + 0.3	V
	IOUTA, IOUTB	ACOM	–1.0	AVDD + 0.3	V
	COMP1, COMP2	ACOM	–0.3	AVDD + 0.3	V
	REFIO, FSADJ	ACOM	–0.3	AVDD + 0.3	V
	REFLO	ACOM	–0.3	0.3	V
T_J	Maximum Junction Temperature			150	°C
T_{STG}	Storage Temperature Range		–65	150	°C
T_L	Lead Temperature (10 sec)			300	°C

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. The functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP28	97.9	14.0	°C/W

Electrical Specifications—DC Specifications

All test conditions: T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	Resolution		8			Bits
	Monotonicity		Guaranteed over Specified Temperature Range			
DC Accuracy (1)						
INL	Integral Linearity Error		–1	±1/2	1	LSB
DNL	Differential Nonlinearity		–1/2	±1/4	1/2	LSB
Analog Output						
OE	Offset Error		–0.025		0.025	% of FSR
GE	Gain Error (without Internal Reference)		–10	±2	10	% of FSR
GE	Gain Error (with Internal Reference)		–10	±1	10	% of FSR
	Full-Scale Output Current (2)		2		20.0	mA
	Output Compliance Range		–1.0		1.25	V
	Output Resistance			100		kΩ
C_{OUT}	Output Capacitance			5		pF
Reference Output						
	Reference Voltage		1.08	1.1	1.12	V
	Reference Output Current (3)			100		nA
Reference Input						
	Input Compliance Range		0.1		1.25	V
	Reference Input Resistance			1		M
	Small-Signal Bandwidth (w/o CCOMP1) (4)			1.4	1.4	MHz
Temperature Coefficients						
	Offset Drift			0		ppm of FSR/°C
	Gain Drift (without Internal Reference)			±50		ppm of FSR/°C
	Gain Drift (with Internal Reference)			±100		ppm of FSR/°C
	Reference Voltage Drift			±50		ppm/°C
Power Supply						
	Supply Voltages					
	AVDD (5)		2.7	5	5.5	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	DVDD		2.7	5	5.5	V
I_{AVDD}	Analog Supply Current			25	30	mA
I_{DVDD}	Digital Supply Current (6)			3	6	mA
I_{OUTB}	Supply Current Sleep Mode				8.5	μA
	Power Dissipation (6)	5 V, I_{OUTFS} = 20 mA		140	175	mW
	Power Dissipation (7)	5 V, I_{OUTFS} = 20 mA		190		mW
	Power Dissipation (7)	3 V, I_{OUTFS} = 2 mA		45	45	mW
PSRR	Power Supply Rejection Ratio—AVDD		–0.4		0.4	% of FSR/V
	Power Supply Rejection Ratio—DVDD		–0.025		0.025	% of FSR/V
	Operating Range		–40		85	°C

(1) Measured at I_{OUTA}, driving a virtual ground.
(2) The nominal full-scale current, I_{OUTFS}, is 32 × I_{REF}.
(3) Use an external buffer amplifier to drive any external load.
(4) Reference bandwidth is a function of an external cap at COMP1 pin.
(5) For operation below 3 V, it is recommended that the output current be reduced to 12 mA or less to maintain optimum performance.
(6) Measured at f_{CLOCK} = 50 MSPS and f_{OUT} = 1.0 MHz.
(7) Measured as the unbuffered voltage output into 50. R_{LOAD} at I_{OUTA} and I_{OUTB}, f_{CLOCK} = 100 MSPS and f_{OUT} = 40 MHz. Specifications are subject to change without notice.

Electrical Specifications—Dynamic Specifications

All test conditions: T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, single-ended output, I_{OUTA}, 50-V doubly terminated, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Dynamic Performance						
f_{CLOCK}	Maximum Output Update Rate		100		125	MSPS
t_{ST}	Output Settling Time (1)	To 0.1%		35		ns
t_{PD}	Output Propagation Delay			1		ns
	Glitch Impulse			5		pV-s
	Output Rise Time (1)	10% to 90%		2.5		ns
	Output Fall Time (1)	10% to 90%		2.5		ns
	Output Noise	I_{OUTFS} = 20 mA		50		pA/√Hz
		I_{OUTFS} = 2 mA		30		pA/√Hz
AC Linearity to Nyquist						
SINAD	Signal-to-Noise and Distortion Ratio	f_{CLOCK} = 10 MSPS; f_{OUT} = 1.00 MHz		50		dB
		f_{CLOCK} = 50 MSPS; f_{OUT} = 1.00 MHz		50		dB
		f_{CLOCK} = 50 MSPS; f_{OUT} = 12.51 MHz		48		dB
		f_{CLOCK} = 100 MSPS; f_{OUT} = 5.01 MHz		50		dB
		f_{CLOCK} = 100 MSPS; f_{OUT} = 25.01 MHz		45		dB
THD	Total Harmonic Distortion	f_{CLOCK} = 10 MSPS; f_{OUT} = 1.00 MHz		−67		dBc
		f_{CLOCK} = 50 MSPS; f_{OUT} = 1.00 MHz		−72		dBc
		f_{CLOCK} = 50 MSPS; f_{OUT} = 12.51 MHz		−59		dBc
		f_{CLOCK} = 100 MSPS; f_{OUT} = 5.01 MHz		−64		dBc
		f_{CLOCK} = 100 MSPS; f_{OUT} = 25.01 MHz		−48		dBc

(1) Measured single ended into 50-Ω load.
(2) Specifications are subject to change without notice.

Electrical Specifications—Digital Specifications

All test conditions: T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Digital Inputs						
	Logic "1" Voltage	@ DVDD = +5 V	3.5	5		V
		@ DVDD = +3 V	2.1	3		V
	Logic "0" Voltage	@ DVDD = +5 V		0	1.3	V
		@ DVDD = +3 V		0	0.9	V
	Logic "1" Current		–10		10	μA
	Logic "0" Current		–10		10	μA
C_{IN}	Input Capacitance			5		pF
t_S	Input Setup Time		2			ns
t_H	Input Hold Time		1.5			ns
t_{LPW}	Latch Pulsewidth		3.5			ns

(1) Specifications are subject to change without notice.

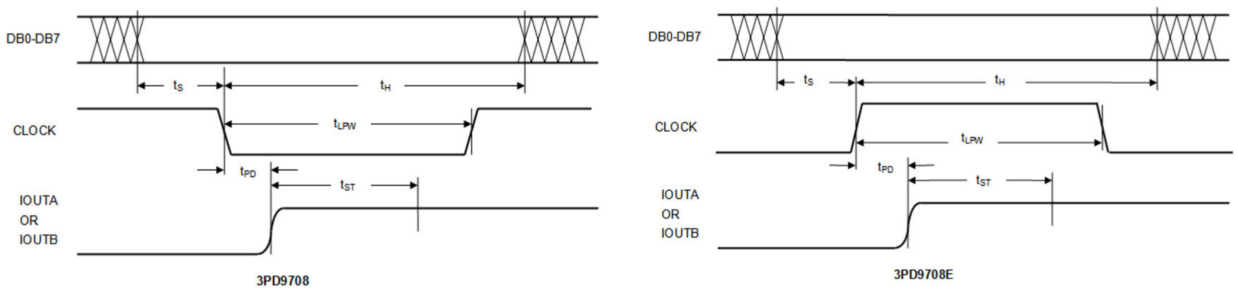


Figure 1. Timing Diagram

Definitions of Specifications

Linearity Error (Also Called Integral Nonlinearity or INL)

Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (DNL)

DNL measures the variation in the analog value, normalized to full scale, associated with a 1-LSB change in the digital input code.

Monotonicity

A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error

The deviation of the output current from the ideal of zero is called offset error. For I_{OUTA}, 0-mA output is expected when the inputs are all 0 s. For I_{OUTB}, 0-mA output is expected when all inputs are set to 1 s.

Gain Error

The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1 s minus the output when all inputs are set to 0 s.

Output Compliance Range

The range of allowable voltages at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown resulting in nonlinear performance.

Temperature Drift

Temperature drift is specified as the maximum change from the ambient (+25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection

The maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time

The settling time is required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse

Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range

The difference in dB, between the RMS amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Signal-to-Noise and Distortion (S/N+D, SINAD) Ratio

S/N+D is the ratio of the RMS value of the measured output signal to the RMS sum of all other spectral components below the Nyquist frequency, including harmonics but excluding DC. The value for S/N+D is expressed in decibels.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first six harmonic components to the RMS value of the measured output signal. It is expressed as a percentage or in decibels.

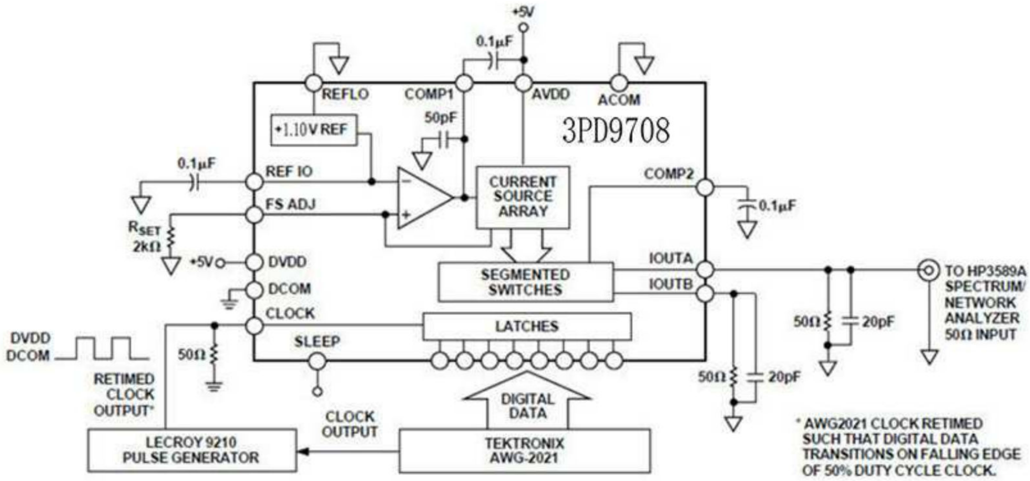


Figure 2. Basic AC Characterization Test Setup

Typical Performance Characteristics

All test conditions: AVDD = +5 V or +3 V, DVDD = +5 V or +3 V, 50-V doubly terminated load, single-ended output, I_{OUTA}, I_{OUTFS} = 20 mA, T_A = +258°C, unless otherwise noted.

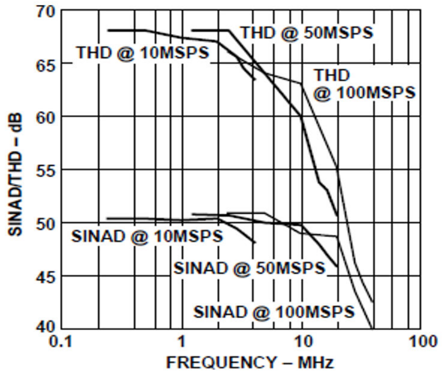


Figure 3. SINAD/THD vs. f_{OUT} (AVDD and DVDD = 5.0 V)

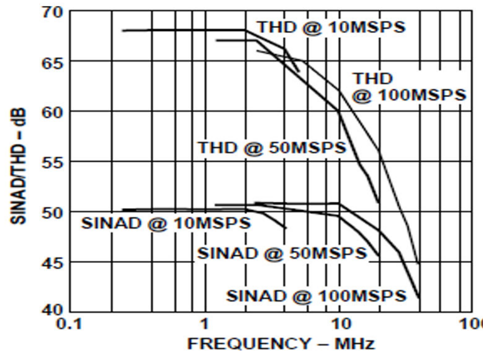


Figure 4. SINAD/THD vs. f_{OUT} (Differential Output, AVDD and DVDD = 5.0 V)

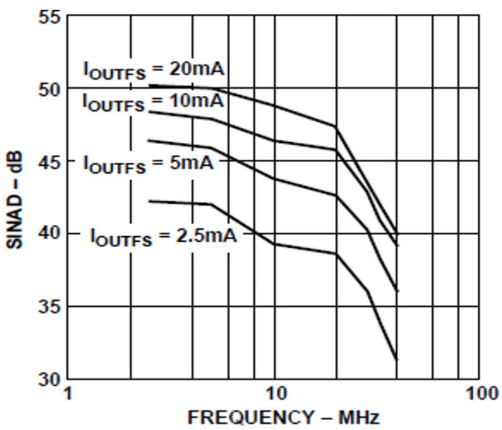


Figure 5. SINAD vs. I_{OUTFS} @ 100 MSPS

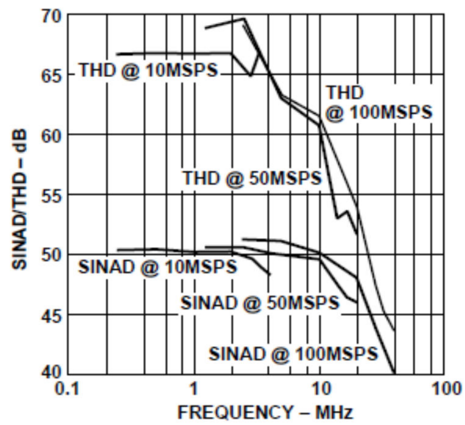


Figure 6. SINAD/THD vs. f_{OUT} (AVDD and DVDD = 3.0 V)

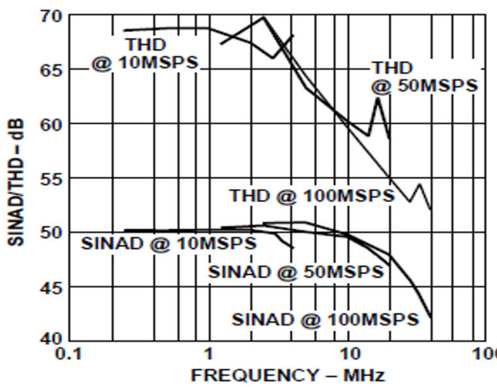


Figure 7. SINAD/THD vs. f_{OUT} (Differential Output, AVDD and DVDD = 3.0 V)

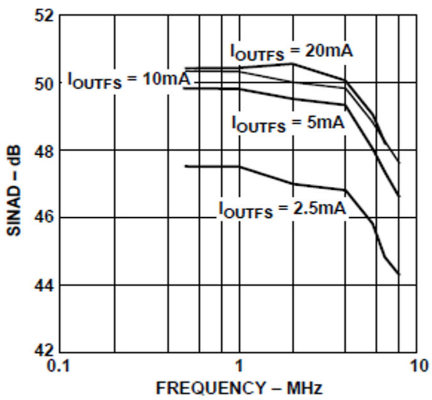


Figure 8. SINAD vs. I_{OUTFS} @ 20 MSPS

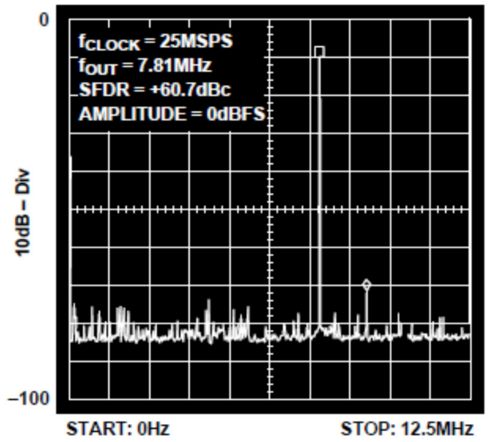


Figure 9. Single-Tone Spectral Plot @ 25 MSPS

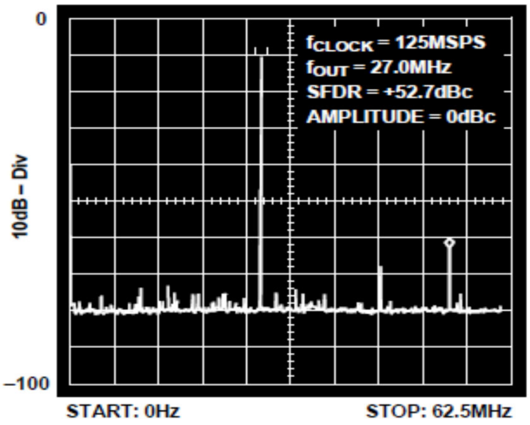


Figure 10. Single-Tone Spectral Plot @ 125 MSPS

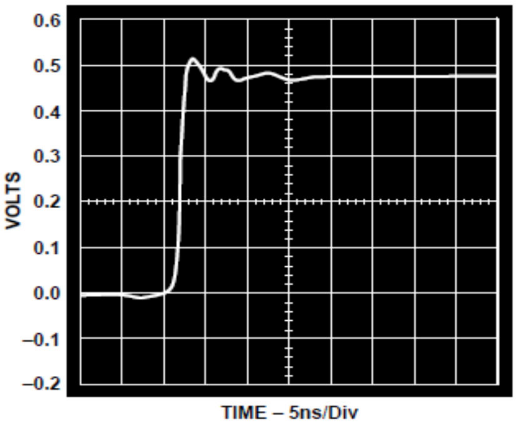


Figure 11. Step Response

Detailed Description

Functional Block Diagram

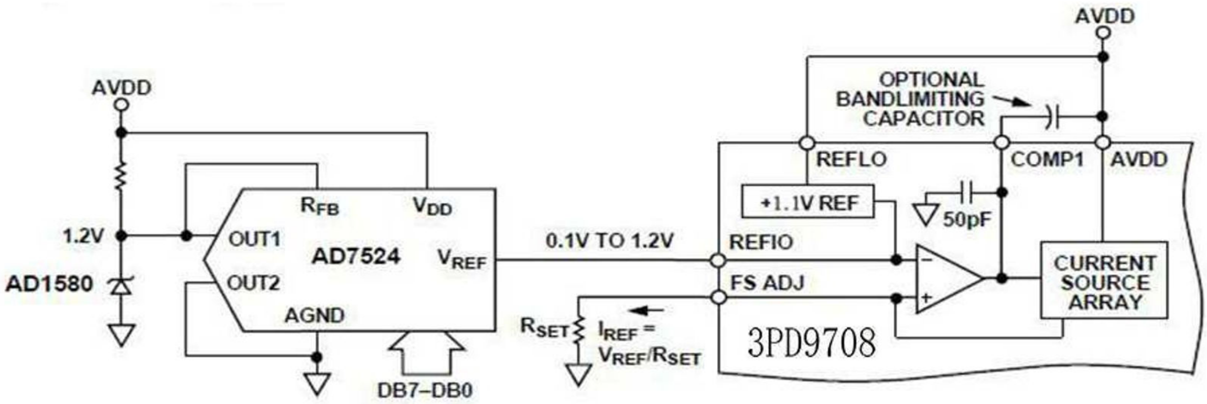


Figure 12. Functional Block Diagram

Feature Description

Functional Description

The 3PD9708(E) consists of a large PMOS current source array capable of providing up to 20-mA total current. The array is divided into 32 equal currents that make up the five most significant bits (MSBs). The remaining 3 LSBs are also implemented with equally weighted current sources whose sum total equals 7/8th of an MSB current source. Implementing the upper and lower bits with current sources helps maintain a high-output impedance of the DAC (i.e. > 100 kW). All of these current sources are switched to one or the other of the two output nodes (i.e., I_{OUTA} or I_{OUTB}) via PMOS differential current switches. The switches are based on a new architecture that drastically improves distortion performance.

The analog and digital sections of the 3PD9708(E) have separate power supply inputs (i.e., AVDD and DVDD) that can operate independently over the range from 2.7 V to 5.5 V. The digital section, which is capable of operating up to a 125-MSPS clock rate, consists of edge-triggered latches and a segment decoding logic circuitry. The analog section includes PMOS current sources, associated differential switches, a 1.10-V bandgap voltage reference, and a reference control amplifier.

The full-scale output current is regulated by the reference control amplifier, and can be set from 2 mA to 20 mA via an external resistor, R_{SET}. The external resistor, in combination with both the reference control amplifier and voltage reference V_{REFIO}, sets the reference current, I_{REF}, which is mirrored over to the segmented current sources with a proper scaling factor. The full-scale current, I_{OUTFS}, is thirty-two times the value of I_{REF}.

DAC Transfer Function

The 3PD9708(E) provides complementary current outputs, I_{OUTA} and I_{OUTB}. I_{OUTA} provides a near full-scale current output, I_{OUTFS}, when all bits are high (i.e., DAC CODE = 255), while I_{OUTB}, the complementary output, provides no current. The current output at I_{OUTA} and I_{OUTB} are a function of both the input code and I_{OUTFS}, and can be expressed as:

$$I_{OUTA} = (\text{DAC CODE}/256) * I_{OUTFS} \quad (1)$$

$$I_{OUTB} = (255 - \text{DAC CODE})/256 * I_{OUTFS} \quad (2)$$

Where, DAC CODE = 0 to 255 (i.e., Decimal Representation).

As mentioned previously, I_{OUTFS} is a function of the reference current (I_{REF}), which is nominally set by a reference voltage (V_{REFIO}) and an external resistor (R_{SET}). It can be expressed as:

$$I_{OUTFS} = 32 * I_{REF} \quad (3)$$

Where

$$I_{REF} = V_{REFIO}/R_{SET} \quad (4)$$

The two current outputs typically drive a resistive load directly. If DC coupling is required, I_{OUTA} and I_{OUTB} should be directly connected to matching resistive loads, R_{LOAD}, which are tied to analog common, ACOM. Note, R_{LOAD} may represent the equivalent load resistance seen by I_{OUTA} or I_{OUTB} as would be the case in a doubly terminated 50-W or 75-W cable. The single-ended voltage output at the I_{OUTA} and I_{OUTB} nodes is simply:

$$V_{OUTA} = I_{OUTA} * R_{LOAD} \quad (5)$$
$$V_{OUTB} = I_{OUTB} * R_{LOAD} \quad (6)$$

Note, the full-scale value of V_{OUTA} and V_{OUTB} should not exceed the specified output compliance range to maintain specified distortion and linearity performance.

The differential voltage, V_{DIFF}, across I_{OUTA} and I_{OUTB} is:

$$V_{DIFF} = (I_{OUTA} - I_{OUTB}) * R_{LOAD} \quad (7)$$

Substitute the values of I_{OUTA}, I_{OUTB}, and I_{REF}; V_{DIFF} can be expressed as:

$$V_{DIFF} = \{(2\ DAC\ CODE - 255)/256\}/ * (32\ R_{LOAD}/R_{SET}) * V_{REFIO} \quad (8)$$

Voltage Reference and Control Amplifier

The 3PD9708(E) contains an internal 1.10-V bandgap reference that can be easily disabled and overridden by an external reference. REFIO serves as either an input or output depending on whether the internal or external reference is selected. If REFLO is tied to ACOM, as shown in Figure 13, the internal reference is activated, and REFIO provides a 1.10-V output. In this case, the internal reference must be compensated externally with a ceramic chip capacitor of 0.1 mF or greater from REFIO to REFLO. Note that REFIO is not designed to drive any external load. It should be buffered with an external amplifier having an input bias current less than 100 nA if any additional loading is required.

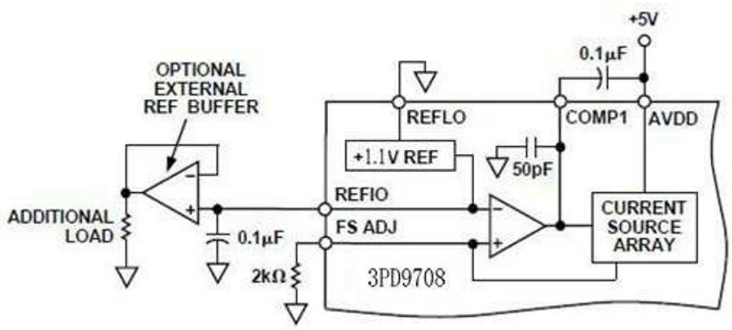


Figure 13. Internal Reference Configuration

The internal reference can be disabled by connecting REFLO to AVDD. In this case, an external reference may be applied to REFIO as shown in Figure 14. The external reference may provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. Note that the 0.1-mF compensation capacitor is not required since the internal reference is disabled, and the high-input impedance (i.e., 1 MW) of REFIO minimizes any loading of the external reference.

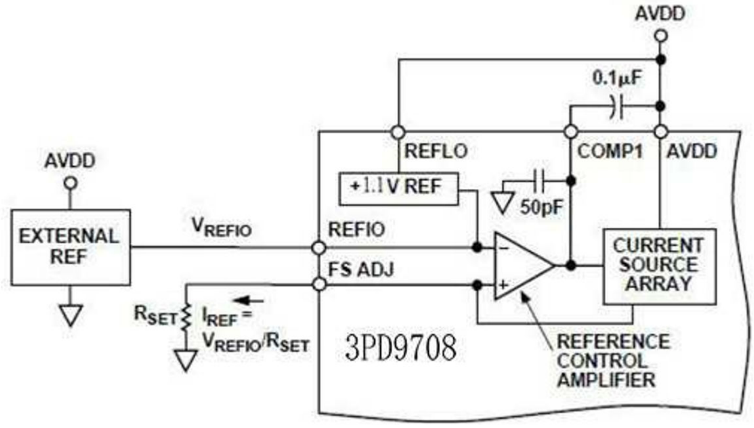


Figure 14. External Reference Configuration

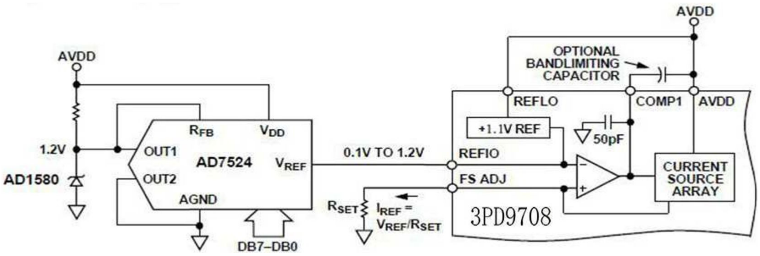


Figure 15. Single-Supply Gain Control Circuit

The small-signal bandwidth of the reference control amplifier is approximately 1.8 MHz, and can be reduced by connecting an external capacitor between COMP1 and AVDD. The output of the control amplifier, COMP1, is internally compensated by a 50-pF capacitor that limits the control amplifier small-signal bandwidth and reduces its output impedance. Any additional external capacitance limits the bandwidth, and acts as a filter to reduce the noise contribution from the reference amplifier. If I_{REF} is fixed for an application, a 0.1-mF ceramic chip capacitor is recommended.

I_{REF} can be varied for a fixed R_{SET} by disabling the internal reference and varying the common-mode voltage over its compliance range from 1.25 V to 0.10 V. REFIO can be driven by a single-supply amplifier or DAC, allowing I_{REF} to be varied for a fixed R_{SET}. Since the input impedance of REFIO is approximately 1 MW, a simple R-2R ladder DAC configured in the voltage mode topology may be used to control the gain. This circuit is shown in Figure 15 using the AD7524 and an external 1.2-V reference, the AD1580. Note, another 3PD9708(E) can also be used as the gain control DAC because it can also provide a programmable unipolar output up to 1.2 V.

Analog Outputs and Output Configurations

The 3PD9708(E) produces two complementary current outputs, I_{OUTA} and I_{OUTB}, which may be converted into complementary single-ended voltage outputs, V_{OUTA} and V_{OUTB}, via a load resistor, R_{LOAD}, as described in the DAC Transfer Function. Figure 17 shows the 3PD9708(E) configured to provide a positive unipolar output range of approximately 0 V to 0.5 V for a double terminated 50-W cable for a nominal full-scale current, I_{OUTFS}, of 20 mA. In this case, R_{LOAD} represents the equivalent load resistance seen by I_{OUTA} or I_{OUTB}, and is equal to 25 W. The unused output (I_{OUTA} or I_{OUTB}) can be connected to ACOM directly or via a matching R_{LOAD}. Different values of I_{OUTFS} and R_{LOAD} can be selected as long as the positive compliance range is adhered to.

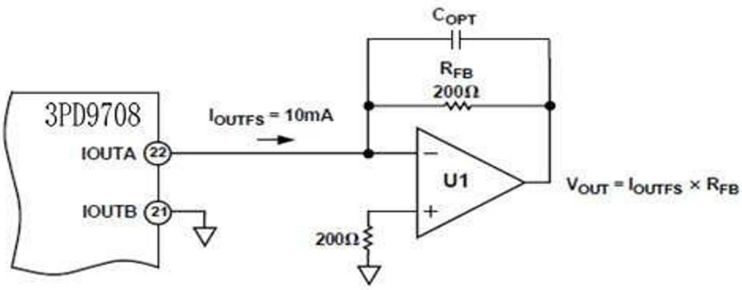


Figure 16. Unipolar Buffered Voltage Output

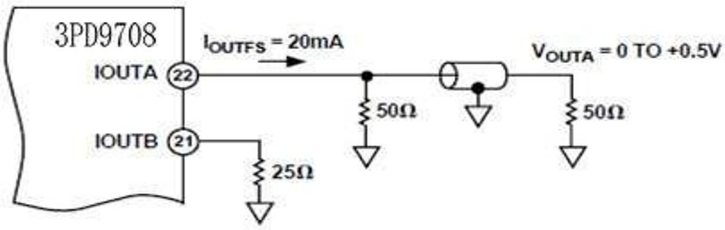


Figure 17. 0-V to 0.5-V Unbuffered Voltage Output

Alternatively, an amplifier can be configured as an I-V converter to convert I_{OUTA} or I_{OUTB} into a negative unipolar voltage. Figure 16 shows a buffered singled-ended output configuration in which the op amp, U1, performs an I-V conversion on the 3PD9708(E) output current. U1 provides a negative unipolar output voltage, and its full-scale output voltage is simply the product of RFB and I_{OUTFS}. The full-scale output should be set within the voltage output swing capabilities of U1 by scaling I_{OUTFS} and/or RFB. The improvement of AC distortion performance may result in a reduced I_{OUTFS}, because the signal current U1 is required to sink and is subsequently reduced. Note, the AC distortion performance of this circuit at higher DAC update rates may be limited by the slewing capabilities of U1.

I_{OUTA} and I_{OUTB} also have a negative and positive voltage compliance range that must be adhered to for optimum performance. The positive output compliance range slightly depends on the full-scale output current, I_{OUTFS}. It degrades slightly from its nominal 1.25 V for I_{OUTFS} = 20 mA to 1.00 V for I_{OUTFS} = 2 mA. Applications requiring the output of the 3PD9708(E) (i.e., V_{OUTA} and/or V_{OUTB}) to extend up to its output compliance range should size R_{LOAD} accordingly. Operation beyond this compliance range adversely affects the linearity of the 3PD9708(E). The differential voltage, V_{DIFF}, existing between V_{OUTA} and V_{OUTB} may also be converted to a single-ended voltage via a transformer or differential amplifier configuration. Refer to the following sections for more about differential output configuration.

Digital Inputs

The digital input of the 3PD9708(E) consists of eight data input pins and a clock input pin. The 8-bit parallel data inputs follow a standard positive binary coding where DB7 is the most significant bit (MSB) and DB0 is the least significant bit (LSB). The digital interface is implemented using an edge-triggered master slave latch. The 3PD9708 output is updated following the falling edge of the clock, while the 3PD9708E output is updated following the rising edge as shown in Figure 1 and is designed to support a clock rate as high as 125 MSPS. The clock can be operated at any duty cycle that meets the specified latch pulsewidth. The setup-and-hold time can also be varied within the clock cycle as long as the specified minimum time is met, although the location of these transition edges may affect digital feedthrough and distortion performance.

The digital inputs are CMOS compatible with logic thresholds, $V_{THRESHOLD}$, set to approximately half the digital positive supply (DVDD), or

$$V_{THRESHOLD} = DVDD/2(\pm 20\%) \quad (9)$$

Figure 18 shows the equivalent digital input circuit for the data and clock inputs. The sleep mode input is similar, except that it contains an active pull-down circuit, thus ensuring that the D9708 remains enabled if this input is left disconnected. The internal digital circuitry of the 3PD9708(E) is capable of operating over a digital supply range from 2.7 V to 5.5 V. As a result, the digital inputs can also accommodate TTL levels when DVDD is set to accommodate the maximum high-level voltage, V_{OH} (Max), of the TTL drivers. A DVDD from 3 V to 3.3 V typically ensures upper compatibility of most TTL logic families.

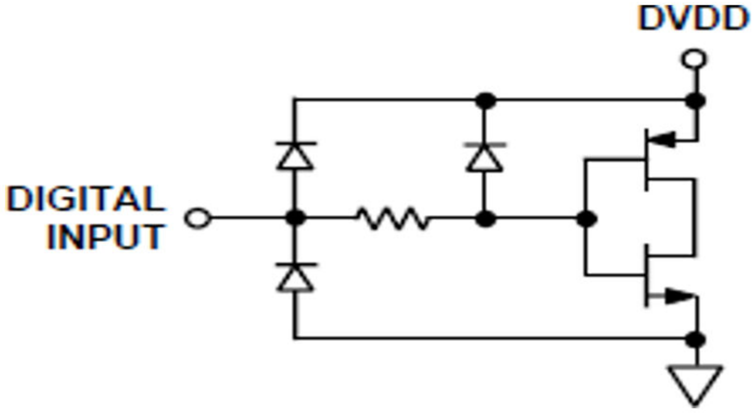


Figure 18. Equivalent Digital Input

Since the 3PD9708(E) is capable of being updated up to 125 MSPS, the quality of the clock and data input signals are important in achieving the optimum performance. The drivers of the digital data interface circuitry should be specified to meet the minimum setup-and-hold time of the 3PD9708(E) as well as its required min/max input logic level thresholds. Typically, the selection of the slowest logic family that satisfies the conditions above results in the lowest data feedthrough and noise. Digital signal paths should be kept short and run lengths matched to avoid propagation delay mismatch. The insertion of a low-value resistor network (i.e., 20 W to 100 W) between the 3PD9708(E) digital inputs and driver outputs may be helpful in reducing any overshooting and ringing at the digital inputs that contribute to data feedthrough. For longer run lengths and high data update rates, strip line techniques with proper termination resistors should be considered to maintain "clean" digital inputs. Also, operating the 3PD9708(E) with reduced logic swings and a corresponding digital supply (DVDD) also reduces data feedthrough. The external clock driver circuitry should provide the 3PD9708(E) with a low-jitter clock input meeting the min/max logic levels while providing fast edges. Fast clock edges help minimize any jitter that manifests itself as phase noise on a reconstructed waveform. However, the clock input can also be driven by via a sine wave, which is centered around the digital threshold (i.e., DVDD / 2), and meets the min/max logic threshold. This may result in a slight degradation in the phase noise, which becomes more noticeable at higher sampling rates and output frequencies. Note, at higher sampling rates, 20% tolerance of the digital logic threshold should be considered since it affects the effective clock duty cycle and subsequently cut into the required data setup-and-hold time.

Sleep Mode Operation

The 3PD9708(E) has a power-down function that turns off the output current and reduces the supply current to less than 8.5 µA over the specified supply range from 2.7 V to 5.5 V and temperature range. This mode can be activated by applying a logic level "1" to the SLEEP pin. This digital input also contains an active pull-down circuit that ensures the 3PD9708(E) remains enabled if this input is left disconnected. The SLEEP input with active pull-down requires < 40 mA of the drive current.

The power-up and power-down characteristics of the 3PD9708(E) are dependent on the value of the compensation capacitor connected to COMP2 (Pin 23). With a nominal value of 0.1 mF, the 3PD9708(E) takes less than 5 ms to power down and approximately 3.25 ms to power back.

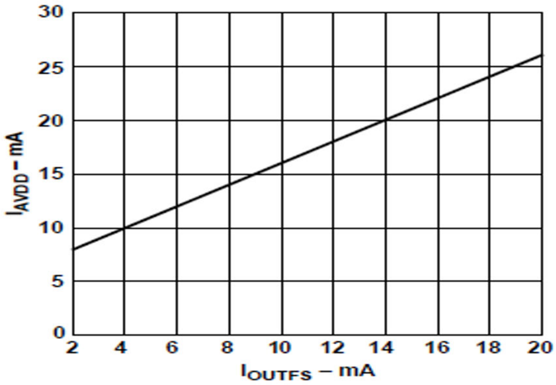


Figure 19. I_{AVDD} vs. I_{OUTFS}

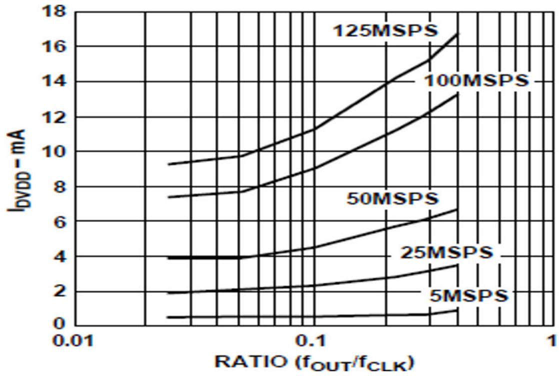


Figure 20. IDVDD vs. Ratio @ DVDD = 5 V

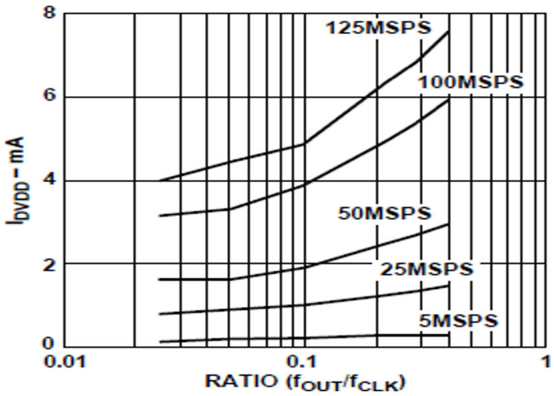


Figure 21. IDVDD vs. Ratio @ DVDD = 3 V

Power Dissipation

The power dissipation, PD, of the 3PD9708(E) is dependent on several factors, including: (1) AVDD and DVDD, the power supply voltages; (2) I_{OUTFS}, the full-scale current output; (3) f_{CLOCK}, the update rate; (4) and the reconstructed digital input waveform. The power dissipation is directly proportional to the analog supply current, I_{AVDD}, and the digital supply current, I_{DVDD}. I_{AVDD} is directly proportional to I_{OUTFS}, as shown in Figure 19, and is insensitive to f_{CLOCK}.

Conversely, I_{DVDD} is dependent on both the digital input waveform, f_{CLOCK}, and digital supply DVDD. Figure 20 and Figure 21 show I_{DVDD} as a function of full-scale sine wave output ratios (f_{OUT}/f_{CLOCK}) for various update rates with DVDD = 5 V and DVDD = 3 V, respectively. Note, I_{DVDD} is reduced by more than a factor of 2 when DVDD is reduced from 5 V to 3 V.

Applying the 3PD9708(E) Power and Grounding Considerations

In systems seeking to simultaneously achieve high speed and high performance, the implementation and construction of the printed circuit board design is often as important as the circuit design. Proper RF techniques must be used in device selection placement and routing and supply bypassing and grounding. The evaluation board for the 3PD9708(E), which uses a four-layer PC board, serves as a good example for the considerations mentioned above. The evaluation board provides an illustration of the recommended printed circuit board ground, power and signal plane layouts.

Proper grounding and decoupling should be a primary objective in any high-speed system. The 3PD9708(E) features separate analog and digital supply and ground pins to optimize the management of analog and digital ground currents in a system. In general, AVDD, the analog supply, should be decoupled to ACOM, the analog common, as close to the chip as physically possible. Similarly, DVDD, the digital supply, should be decoupled to DCOM as close as physically as possible.

For those applications requiring a single 5-V or 3-V supply for both the analog and digital supply, a clean analog supply may be generated using the circuit shown in Figure 22. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained using low ESR type electrolytic and tantalum capacitors.

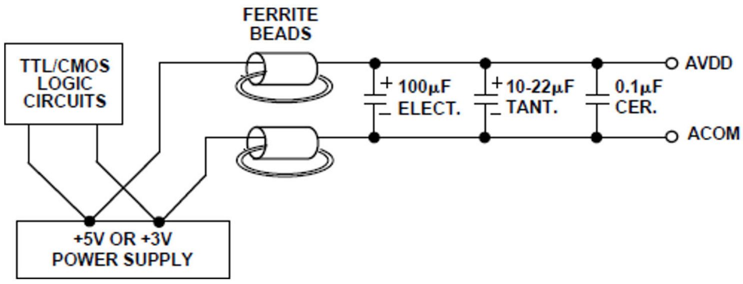


Figure 22. Differential LC Filter for Single 5-V or 3-V Applications

Maintaining low noise on power supplies and ground is critical to obtaining optimum results from the 3PD9708(E). If properly implemented, ground planes can perform a host of functions on high-speed circuit boards: bypassing, shielding, current transport, etc. In mixed signal design, the analog and digital portions of the board should be distinct from each other, with the analog ground plane confined to the areas covering the analog signal traces, and the digital ground plane confined to areas covering the digital interconnects.

All analog ground pins of the DAC, reference, and other analog components, should be tied directly to the analog ground plane. The two ground planes should be connected by a path 1/8 to 1/4 inch wide underneath or within 1/2 inch of the DAC to maintain optimum performance. Ensure that the ground plane is uninterrupted over crucial signal paths. On the digital side, this includes the digital input lines running to the DAC as well as any clock signals. On the analog side, this includes DAC output signals, reference signals, and supply feeders.

The use of wide runs or planes in the routing of power lines is also recommended. This serves to provide a low series impedance power supply to the part, and offer some "free" capacitive decoupling to the appropriate ground plane. It is essential that care be taken in the layout of signal and power ground interconnects to avoid inducing extraneous voltage drops in the signal ground paths. It is recommended that all connections be short, direct, and as physically close to the package as possible to minimize the sharing of conduction paths between different currents. When runs exceed an inch in length, strip line techniques with proper termination resistor should be considered. The necessity and value of this resistor rely on the logic family used.

For applications requiring optimum dynamic performance and/or a bipolar output swing, a differential output configuration is suggested. A differential output configuration may consist of either an RF transformer or a differential op amp configuration. The transformer configuration is well suited for AC-coupling applications. It provides optimum high-frequency performance due to its excellent rejection of common-mode distortion (i.e., even-order harmonics) and noise over a wide frequency range. It also provides electrical isolation and the ability to deliver twice the power to the load (i.e., assuming no source termination). The differential op amp configuration is suitable for applications requiring DC coupling, a bipolar output, signal gain, and/or level shifting.

Figure 23 shows the 3PD9708(E) in a typical transformer coupled output configuration. The center-tap on the primary side of the transformer must be connected to ACOM to provide a necessary DC current path for both I_{OUTA} and I_{OUTB}. The complementary voltages at I_{OUTA} and I_{OUTB} (i.e., V_{OUTA} and V_{OUTB}) swing symmetrically around ACOM, and should be maintained within the specified output compliance range of the 3PD9708(E). A differential resistor, RDIFF, may be inserted in applications in which the output of the transformer is connected to the load, R_{LOAD}, via a passive reconstruction filter or cable. R_{DIFF} is determined by the impedance ratio of the transformer, and provides proper source termination. Note that approximately half the signal power is dissipated across R_{DIFF}.

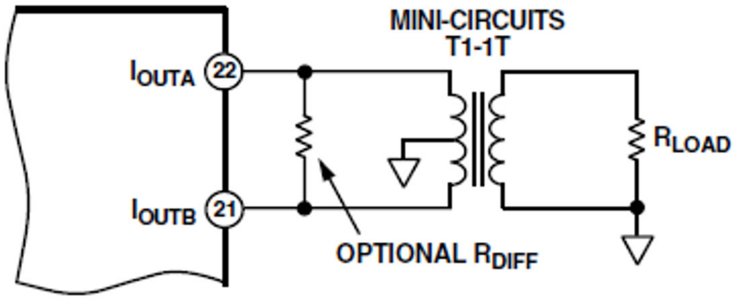


Figure 23. Differential Output Using a Transformer

An op amp can also be used to perform a differential to single-ended conversion as shown in Figure 24. The 3PD9708(E) is configured with two equal load resistors, R_{LOAD}, of 25 W. The differential voltage developed across I_{OUTA} and I_{OUTB} is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across I_{OUTA} and I_{OUTB} forming a real pole in a low-pass filter. The addition of this capacitor also enhances the op amps distortion performance by preventing the DACs high-slewing output from overloading the input of the op amp.

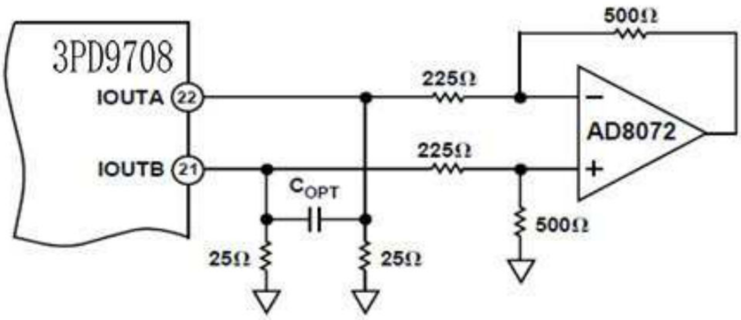


Figure 24. DC Differential Coupling Using an Op Amp

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit is configured to provide some additional signal gain. The op amp must operate off a dual supply since its output is approximately ±1.0 V. A high-speed amplifier capable of preserving the differential performance of the 3PD9708(E) while meeting other system level objectives (i.e., cost, power) should be selected. The op amps differential gain, its gain setting resistor values, and full-scale output swing capabilities should all be considered when optimizing this circuit.

The differential circuit shown in Figure 25 provides necessary level-shifting required in a single supply system. In this case, AVDD, which is the positive analog supply for both the 3PD9708(E) and the op amp, is also used to level-shift the differential output of the AD9762 to mid-supply (i.e., AVDD / 2).

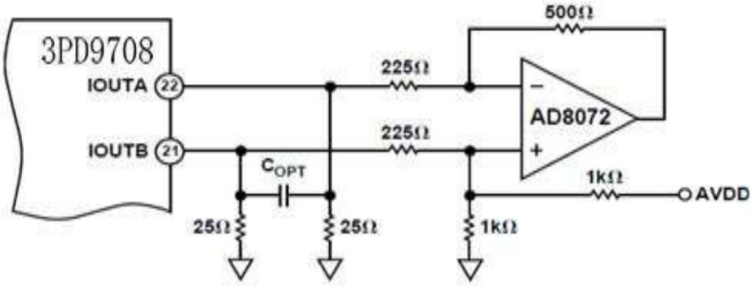
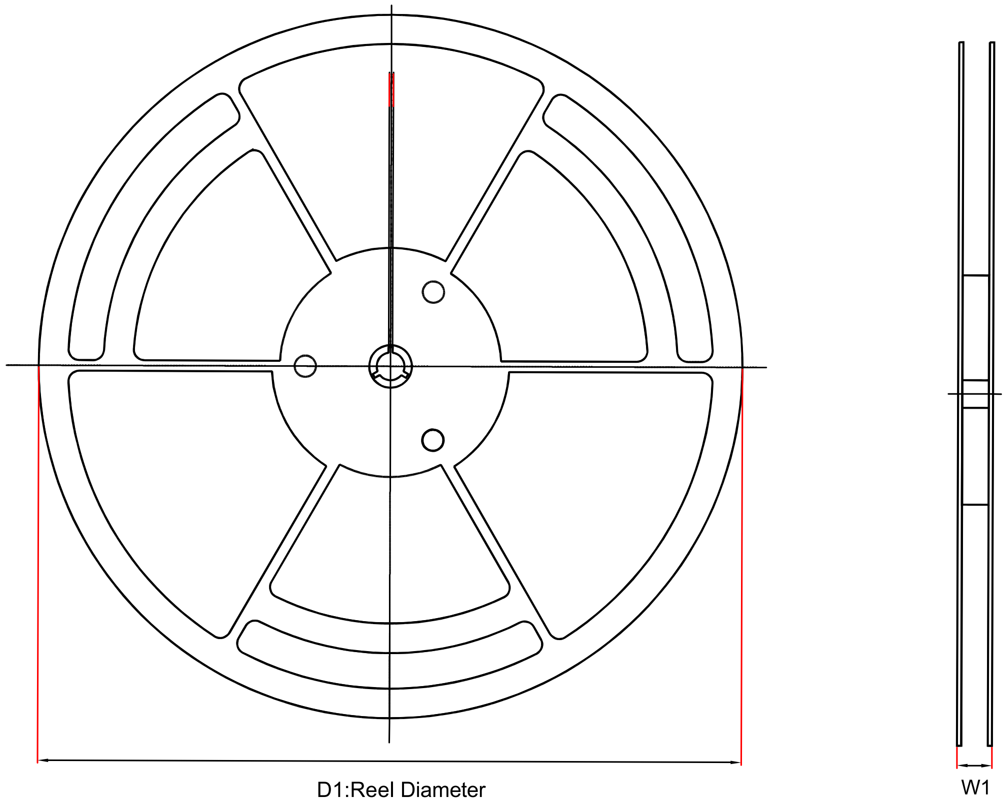
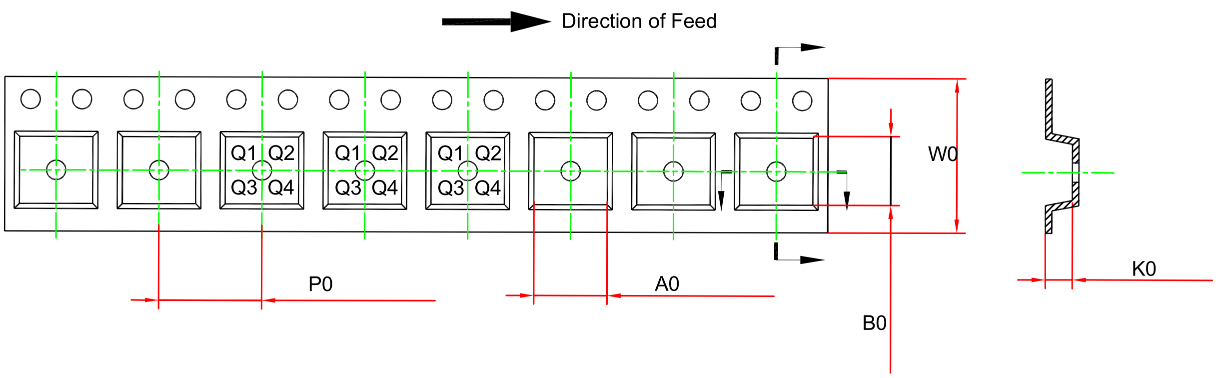


Figure 25. Single-Supply DC Differential Coupled Circuit

Tape and Reel Information



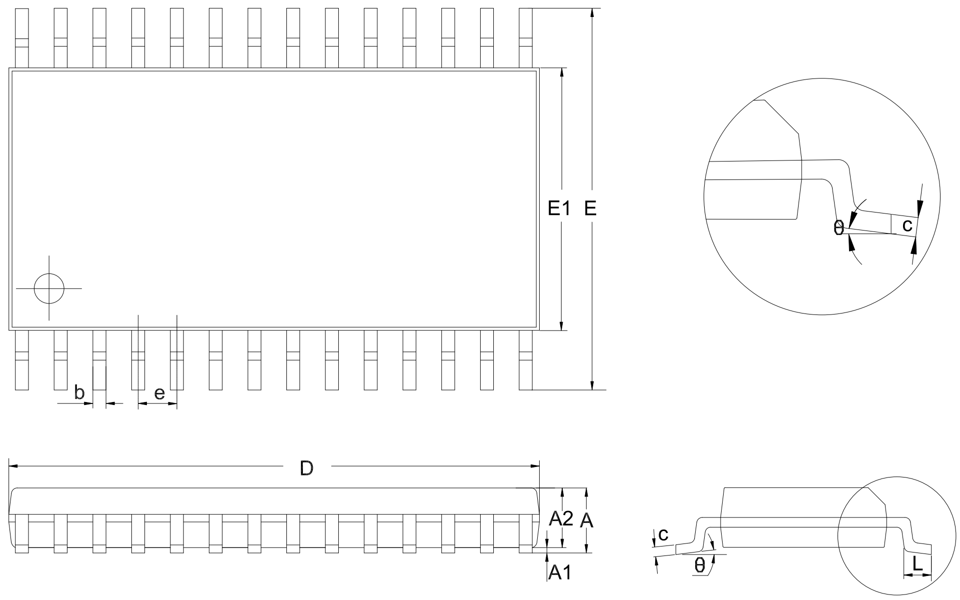


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
3PD9708E	TSSOP28	330	21.6	6.8	10.15	1.6	8	16	Q1

Package Outline Dimensions

TSSOP28

Package Outline Dimensions TS6(TSSOP-28-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
3PD9708E	−40 to 85°C	TSSOP28	3PD9708E	3	2500	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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