Features

- CMOS 8-Bit 32-MSPS Sampling A/D Converter
- Pin Compatible with AD9280
- Power Dissipation: 85 mW (3-V Supply)
- Operation between 2.7-V and 5.5-V Supply
- Differential Nonlinearity: 0.2 LSB
- Power-down (Sleep) Mode
- Three-State Outputs
- Out-of-Range Indicator
- Built-in Clamp Function (DC Restore)
- Adjustable on-Chip Voltage Reference
- IF under Sampling to 135 MHz

Highlights

- Low Power: The 3PA9280 consumes 95 mW on a 3-V supply (excluding the reference power). In sleep mode, power is reduced to below 5 mW.
- Very Small Package: The 3PA9280 is available in the SSOP28 package.
- Pin Compatible with AD9280: The 3PA9280 is pin compatible with the AD9280, allowing older designs to migrate to lower supply voltages.
- 100-MHz Onboard Sample and Hold: The versatile SHA input can be configured for either single-ended or differential inputs.
- Out-of-Range Indicator: The OTR output bit indicates when the input signal is beyond the input range of the 3PA9280.
- Built-in Clamp Function: DC restoration of video signals is allowed.

Description

The 3PA9280 is a monolithic, single-supply, 8-bit, 32-MSPS analog-to-digital converter with an on-chip sample-and-hold amplifier and a voltage reference. The 3PA9280 uses a multi-stage differential pipeline architecture at 32-MSPS data rates, and guarantees no missing codes over the full operating temperature range.

The input of the 3PA9280 is designed to ease the development of both imaging and communications systems. Users can select a variety of input ranges and offsets, and can drive the single-ended or differential input.

The sample-and-hold amplifier (SHA) is equally suited for both multiplexed systems that switch full-scale voltage levels in successive channels and sampling single-channel inputs at frequencies up to and beyond the Nyquist rate. AC-coupled input signals can be shifted to a predetermined level, with an onboard clamp circuit. The dynamic performance is excellent.

The 3PA9280 has an onboard programmable reference. An external reference can also be chosen to suit the DC accuracy and temperature drift requirements of the application.

A single clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary output format. An out-of-range signal (OTR) indicates an overflow condition which can be used with the most significant bit to determine a low or high overflow.

The 3PA9280 operates with a supply ranging from +2.7 V to +5.5 V, suited for low-power operation in high-speed applications. The 3PA9280 is specified over the industrial temperature range from –40°C to +85°C.

Functional Block Diagram

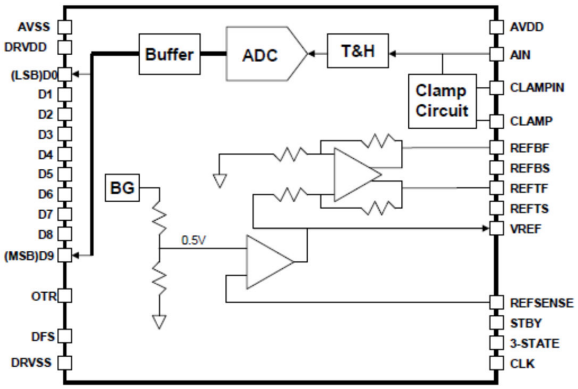


Table of Contents

Revision History

Date	Revision	Notes
2024-12-30	Rev.A.1	Updated to a new datasheet format. Updated the Order Information. Added the Tape and Reel Information.

Pin Configuration and Functions

3PA9280
SSOP28
Top View

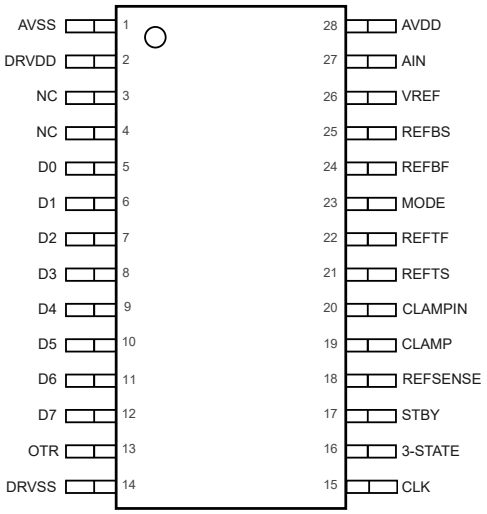


Table 1. Pin Functions

Pin No.	Name	Description
1	AVSS	Analog ground.
2	DRVDD	Digital driver supply.
3	NC	Not connect.
4	NC	Not connect.
5	D0	Bit 0.
6	D1	Bit 1.
7	D2	Bit 2.
8	D3	Bit 3.
9	D4	Bit 4.
10	D5	Bit 5.
11	D6	Bit 6.
12	D7	Bit 7 (most significant bit).
13	OTR	Out-of-range indicator.
14	DRVSS	Digital ground.
15	CLK	Clock input.
16	3-STATE	HI: High-impedance state. LO: normal operation.
17	STBY	HI: power-down mode. LO: normal operation.
18	REFSENSE	Reference select.
19	CLAMP	HI: enable clamp mode. LO: no clamp.
20	CLAMPIN	Clamp reference input.

Pin No.	Name	Description
21	REFTS	Top reference.
22	REFTF	Top reference decoupling.
23	MODE	Mode select.
24	REFBF	Bottom reference decoupling.
25	REFBS	Bottom reference.
26	VREF	Internal reference output.
27	AIN	Analog input.
28	AVDD	Analog supply.

Specifications

Absolute Maximum Ratings (1)

Parameter		With Respect to	Min	Max	Unit
	AVDD	AVSS	–0.3	6.5	V
	DRVDD	DRVSS	–0.3	6.5	V
	AVSS	DRVSS	–0.3	0.3	V
	AVDD	DRVDD	–6.5	6.5	V
	MODE	AVSS	–0.3	AVDD + 0.3	V
	CLK	AVSS	–0.3	AVDD + 0.3	V
	Digital Outputs	DRVSS	–0.3	DRVDD + 0.3	V
	AIN	AVSS	–0.3	AVDD + 0.3	V
	VREF	AVSS	–0.3	AVDD + 0.3	V
	REFSENSE	AVSS	–0.3	AVDD + 0.3	V
	REFTF, REFTB	AVSS	–0.3	AVDD + 0.3	V
	REFTS, REFBS	AVSS	–0.3	AVDD + 0.3	V
T_J	Maximum Junction Temperature			150	°C
T_{STG}	Storage Temperature Range		–65	150	°C
T_L	Lead Temperature (10 sec)			300	°C

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. The functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Electrical Specifications

All test conditions: AVDD = +3 V, DRVDD = +3 V, FS = 32 MHz (50% duty cycle), MODE = AVDD, 2-V input span from 0.5 V to 2.5 V, external reference, T_{MIN} to T_{MAX}, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	Resolution			8		Bits
FS	Conversion Rate				32	MHz
DC Accuracy						
DNL	Differential Nonlinearity	REFTS = 2.5 V, REFBS = 0.5 V		±0.2	±1.0	LSB
INL	Integral Nonlinearity			±0.3	±1.5	LSB
E_{ZS}	Offset Error			±0.2	±1.8	%FSR
E_{FS}	Gain Error			±1.2	±3.9	%FSR
Reference Voltages						
REFTF	Top Reference Voltage		0.75		1.5	V
REFBF	Bottom Reference Voltage		0.25		0.5	V
	Differential Reference Voltage		1		2	Vp-p
	Reference Input Resistance (1)	REF: REFSENSE = AVDD		10		kΩ
		Between REFTF & REFBF		1		kΩ
Analog Input						
AIN	Input Voltage Range		0		2 × (REFT − REFB)	V
C_{IN}	Input Capacitance	Switched		2		pF
t_{AP}	Aperture Delay			4		ns
t_{AJ}	Aperture Uncertainty (Jitter)			2		ps
BW	Input Bandwidth (–3 dB)					
	Full Power (0 dB)			300		MHz
	DC Leakage Current	Input = ±FS		43		μA
Internal Reference						
VREF	Output Voltage (1-V Mode)	REFSENSE = VREF		0.5		V
	Output Voltage Tolerance (1-V Mode)			±10	±25	mV
VREF	Output Voltage (2-V Mode)	REFSENSE = GND		1		V
	Load Regulation (1-V Mode)	1-mA load current		0.5	2	mV
Power Supply						
AVDD	Operating Voltage		2.7		5.5	V
DRVDD			2.7		5.5	V
I_{AVDD}	Supply Current			28		mA
P_D	Power Consumption	AVDD = 3 V, MODE = AVSS		85		mW

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	Power-Down	AVDD = DRVDD = 3 V, MODE = AVSS, STBY = AVDD, MODE and CLOCK		10		µW
PSRR	Gain Error Power Supply Rejection			1		% FS
Dynamic Performance (AIN = 0.5-dB FS)						
SINAD	Signal-to-Noise and Distortion	f = 3.58 MHz	46.4	49		dB
		f = 16 MHz		48		dB
	Effective Bits	f = 3.58 MHz		7.8		Bits
		f = 16 MHz		7.7		Bits
SNR	Signal-to-Noise	f = 3.58 MHz	47.8	49		dB
		f = 16 MHz		48		dB
THD	Total Harmonic Distortion	f = 3.58 MHz		–62	–49.5	dB
		f = 16 MHz		–58		dB
SFDR	Spurious-Free Dynamic Range	f = 3.58 MHz		66	51.4	dB
		f = 16 MHz		61		dB
DP	Differential Phase	NTSC 40 IRE Mod Ramp		0.2		°
DG	Differential Gain			0.08		%
Digital Inputs						
V_{IH}	High Input Voltage		2.4			V
V_{IL}	Low Input Voltage				0.3	V
Digital Outputs						
I_{OZ}	High-Z Leakage	Output = GND to V_{DD}	–10		10	µA
t_{OD}	Data Valid Delay	C_L = 20 pF		25		ns
t_{DEN}	Data Enable Delay			25		ns
t_{DHZ}	Data High-Z Delay			13		ns
Logic Output (with DRVDD = 3 V)						
V_{OH}	High-Level Output Voltage	I_{OH} = 50 mA	2.95			V
		I_{OH} = 0.5 mA	2.8			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 1.6 mA			0.4	V
		I_{OL} = 50 mA			0.05	V
Logic Output (with DRVDD = 5 V)						
V_{OH}	High-Level Output Voltage	I_{OH} = 50 mA	4.5			V
		I_{OH} = 0.5 mA	2.4			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 1.6 mA			0.4	V
		I_{OL} = 50 mA			0.1	V
Clocking						
t_{CH}	Clock Pulsewidth High		14.7			ns
t_{CL}	Clock Pulsewidth Low		14.7			ns

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	Pipeline Latency		3			Cycles
Clamp						
E_{OC}	Clamp Error Voltage	CLAMPIN = 0.5 V to 2.0 V,		±60	±80	mV
		RIN = 10 Ω				
t_{CPW}	Clamp Pulsewidth	CIN = 1 µF (Period = 63.5 µs)		2		µs

(1) See Figures 1a and 1b.
(2) Specifications are subject to change without notice.

Definitions of Specifications

Integral Nonlinearity (INL)

Integral nonlinearity refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line.

Differential Nonlinearity (DNL, No Missing Codes)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. It is often specified in terms of the resolution because no missing codes (NMC) are guaranteed.

Offset Error

Transition should occur at a level 1 LSB above "zero". Offset is defined as the deviation of the actual first code transition from that point.

Gain Error

The first code transition should occur for an analog value 1 LSB above the nominal negative full scale. The last transition should occur for an analog value 1 LSB below the nominal positive full scale. Gain Error is the deviation of the actual difference between first and last code transitions and the ideal difference between the first and last code transitions.

Pipeline Delay (Latency)

The number of clock cycles between conversion initiation and the associated output data being made available. New output data is provided every rising.

Typical Performance Characteristics

All test conditions: AVDD = +3 V, DRVDD = +3 V, FS = 32 MHz (50% duty cycle), MODE = AVDD, 2-V input span from 0.5 V to 2.5 V, external reference, unless otherwise noted.

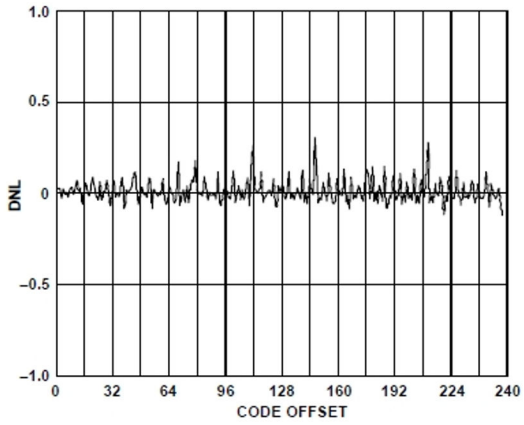


Figure 1. Typical DNL

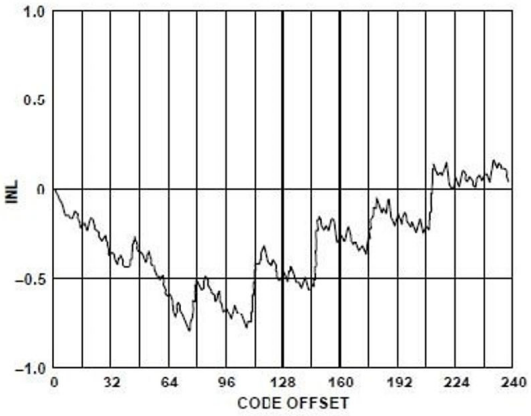


Figure 2. Typical INL

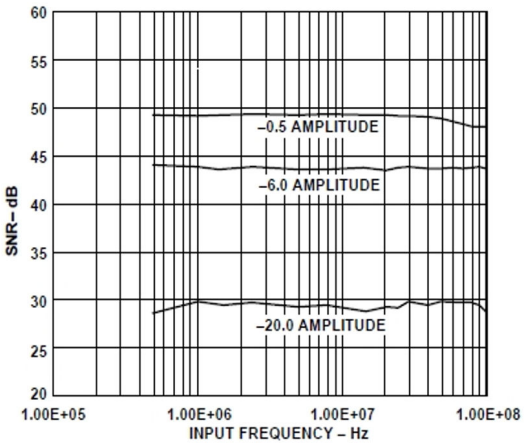


Figure 3. SNR vs. Input Frequency

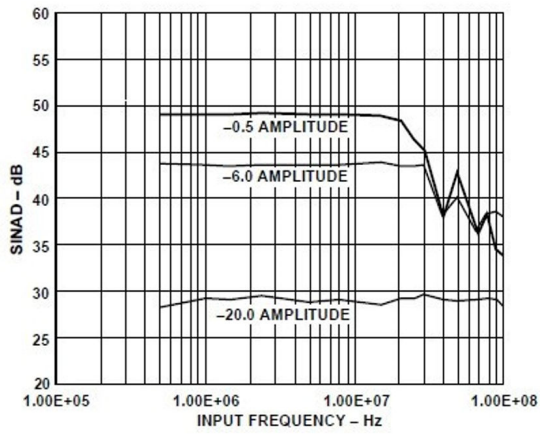


Figure 4. SINAD vs. Input Frequency

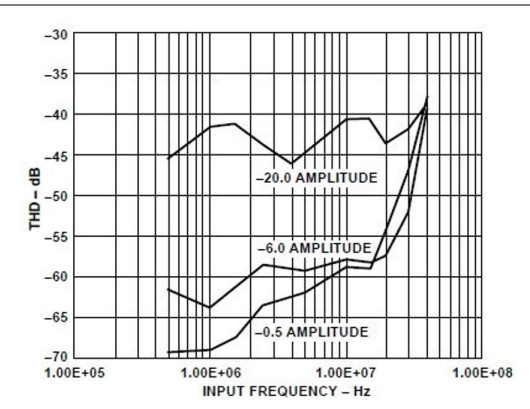


Figure 5. THD vs. Input Frequency

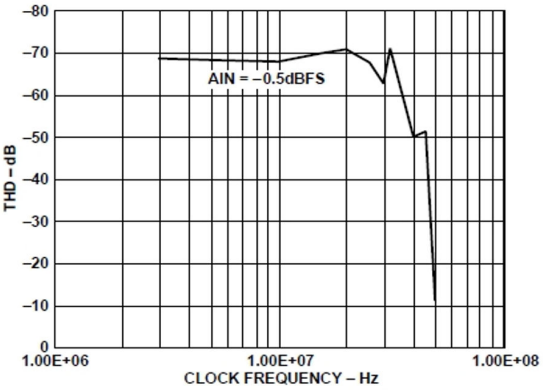


Figure 6. THD vs. Clock Frequency

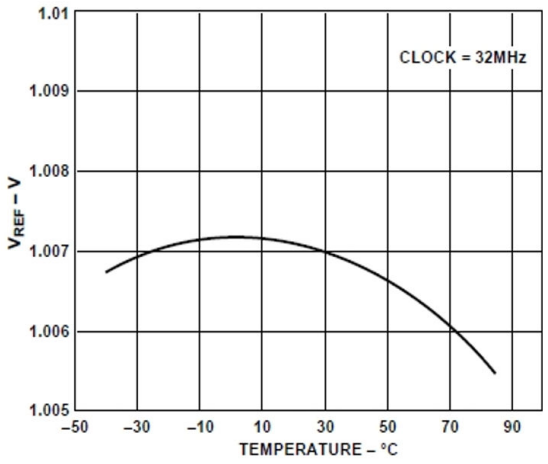


Figure 7. Voltage Reference Error vs. Temperature

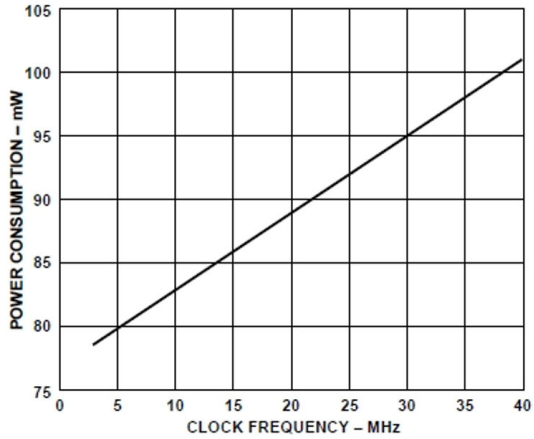


Figure 8. Power Consumption vs. Clock Frequency (MODE = AVSS)

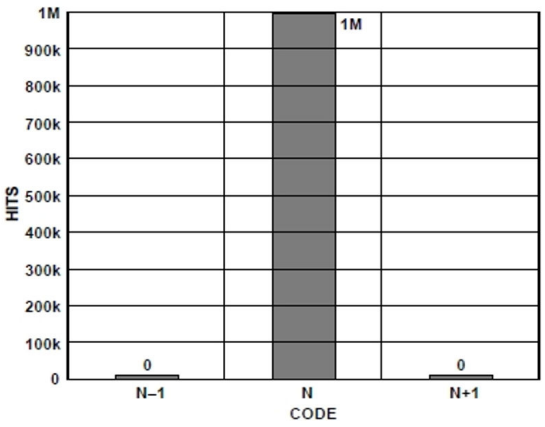


Figure 9. Grounded Input Histogram

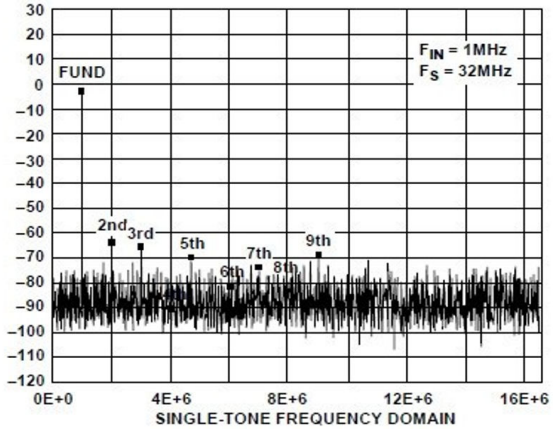


Figure 10. Single-Tone Frequency Domain

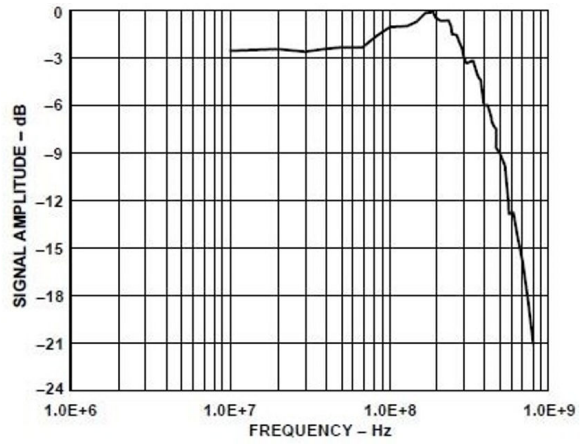


Figure 11. Full-Power Bandwidth

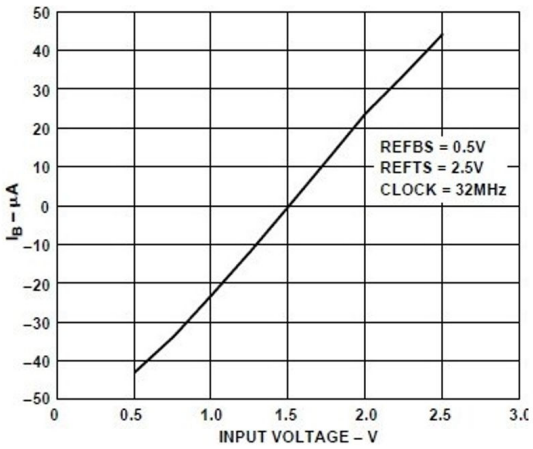


Figure 12. Input Bias Current vs. Input Voltage

Detailed Description

Overview

The 3PA9280 implements a pipelined multistage architecture to achieve a high sampling rate with low power. The 3PA9280 distributes the conversion over several smaller A/D sub-blocks, refining the conversion with progressively higher accuracy as it passes the results from stage to stage. As a consequence of the distributed conversion, the 3PA9280 requires a small fraction of the 256 comparators used in a traditional flash type A/D. A sample-and-hold function within each of the stages permits the first stage to operate on a new input sample, while the second, third, and fourth stages to operate on the three preceding samples.

Functional Block Diagram

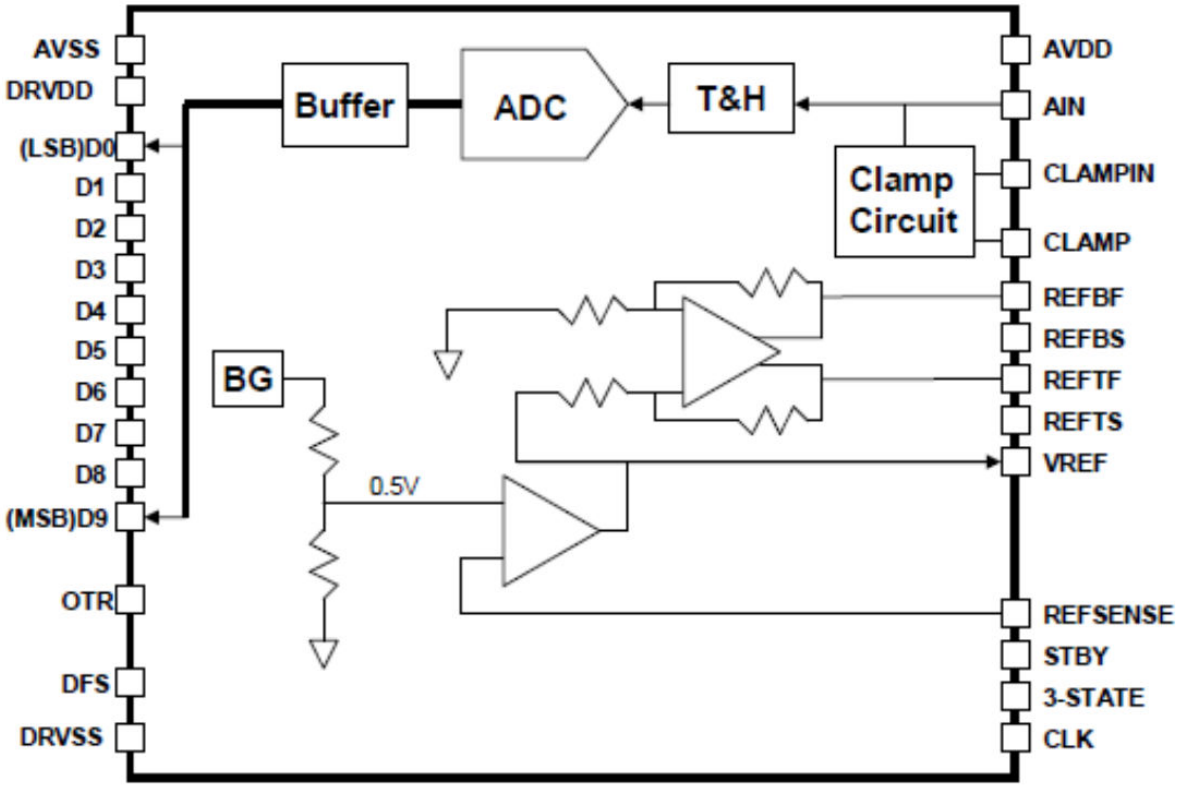


Figure 13. Functional Block Diagram

Feature Description

Operational Modes

The 3PA9280 is designed to allow optimal performance in a wide variety of imaging, communications, and instrumentation applications. To realize this flexibility, internal switches on the 3PA9280 are used to reconfigure the circuit into different modes. These modes are selected by appropriate pin strapping. There are three parts of the circuit affected by this modality: the voltage reference, the reference buffer, and the analog input. The nature of the application determines which mode is appropriate. The descriptions in the following sections and Table 2 assist in selecting the desired mode.

Table 2. Mode Selection

Modes	Input Connect	Input Span	REFSE NSE	REF	REFTS	REFBS	Figure
Top/ Bottom	AIN	1 V	Short REFSENSE, REFTS, and VREF together			AGND	Figure 17
	AIN	2 V	AGND	Short REFTS and VREF together		AGND	Figure 18
Center Span	AIN	1 V	Short VREF and REFSENSE together			AVDD / 2	Figure 19
	AIN	2 V	AGND			AVDD / 2	
Differential	AIN is input 1. REFTS and REFBS are shorted together for input 2.	1 V	Short VREF and REFSENSE Together			AVDD / 2	Figure 28
		2 V	AGND	No connect		AVDD / 2	
External Ref	AIN	2 V (Max)	AVDD	External reference	Span = REFTS − REFBS (2 V Max)		Figure 20 Figure 21
					Short to VREF	Short to VREF	Figure 22

Summary of Modes

Voltage Reference

- **1-V Mode** The internal reference may be set to 1 V by connecting REFSENSE and VREF together.
- **2-V Mode** The internal reference may be set to 2 V by connecting REFSENSE to the analog ground.
- **External Divider Mode** The internal reference may be set to a point between 1 V and 2 V by adding external resistors. See Figure 15 (f).
- **External Reference Mode** Enable users to apply an external reference to the VREF pin. This mode is attained by tying REFSENSE to V_{DD}.

Reference Buffer

- **Center Span Mode** Midscale is set by shorting REFTS and REFBS together and applying the midscale voltage to that point. The analog input swings about that midscale point.
- **Top/Bottom Mode** Set the input range between two points. The two points are between 1 V and 2 V apart.

Analog Input

- **Differential Mode** is attained by driving the AIN pin as an differential input, shorting REFTS and REFBS together, and driving them as the second differential input. The MODE pin is tied to AVDD / 2. Preferred mode for optimal distortion performance.
- **Single Ended** is attained by driving the AIN pin while the REFTS and REFBS pins are held at DC points. The MODE pin is tied to AVDD.
- **Single Ended/Clamped (AC Coupled)** The input may be clamped to some DC level by AC coupling the input. This is done by tying the CLAMPIN to some DC point and applying a pulse to the CLAMP pin. The MODE pin is tied to AVDD.

Input and Reference Overview

A simplified model of the 3PA9280 (see Figure 14), highlights the relationship between the analog input (AIN) and reference voltages (REFTS, REFBS, and VREF). Like the voltages applied to the resistor ladder in a flash A/D converter, REFTS and REFBS define the maximum and minimum input voltages to the A/D.

The input stage is normally configured for single-ended operation, but also allows for differential operation by shorting REFTS and REFBS together to be used as the second input.

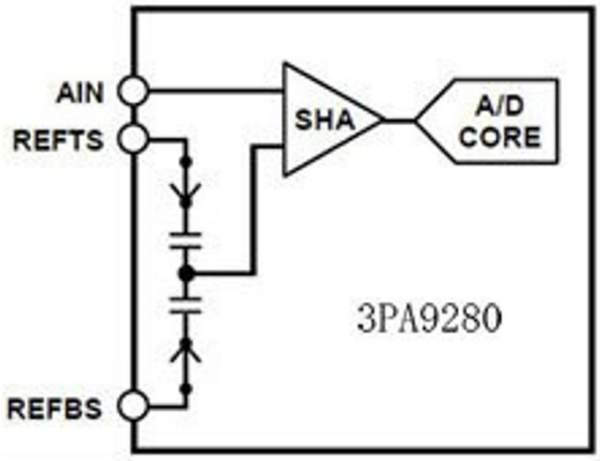


Figure 14. 3PA9280 Equivalent Functional Input Circuit

In single-ended operation, the input spans the range,

$$REFBS \le AIN \le REFTS \quad (1)$$

Where REFBS can be connected to GND, and REFTS connected to VREF. If a different reference range is required, REFBS and REFTS can be driven to any voltage within the power supply rails, so long as the difference between the two is between 1 V and 2 V. In differential operation, REFTS and REFBS are shorted together, and the input span is set by 2 × VREF.

$$(REFTS - VREF) \le AIN \le (REFTS + VREF) \quad (2)$$

Where VREF is determined by the internal reference or brought in externally by users. The best noise performance may be obtained by operating the 3PA9280 with a 2-V input range. The best distortion performance may be obtained by operating the 3PA9280 with a 1-V input range.

Reference Operation

The 3PA9280 can be configured in a variety of reference topologies. The simplest configuration is to use the onboard bandgap reference of the 3PA9280, which provides a pin-trappable option to generate either a 1-V or 2-V output. If a reference voltage other than those two is desired, an external resistor divider can be connected between VREF, REFSENSE, and the analog ground to generate a potential anywhere between 1 V and 2 V. Another alternative is to use an external reference for designs requiring enhanced accuracy and/or drift performance.

Figure 15 (d), Figure 15 (e), and Figure 15 (f) illustrate the reference and input architecture of the 3PA9280. In tailoring a desired arrangement, users can select an input configuration to match the drive circuit. Then, move to the reference modes at the bottom of the figure, and select a reference circuit to accommodate the offset and amplitude of a full-scale signal.

Table 2 outlines pin configurations to match user requirements.

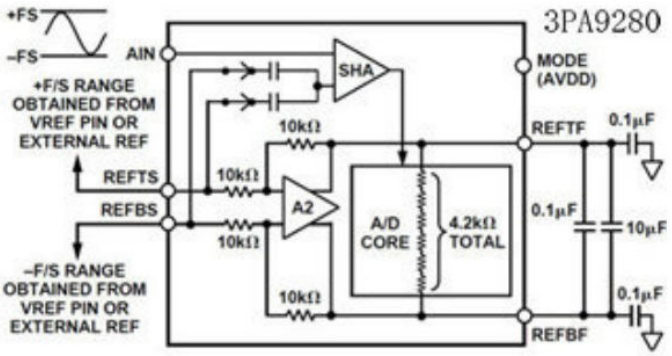


Figure 15 (a). Top/Bottom Mode

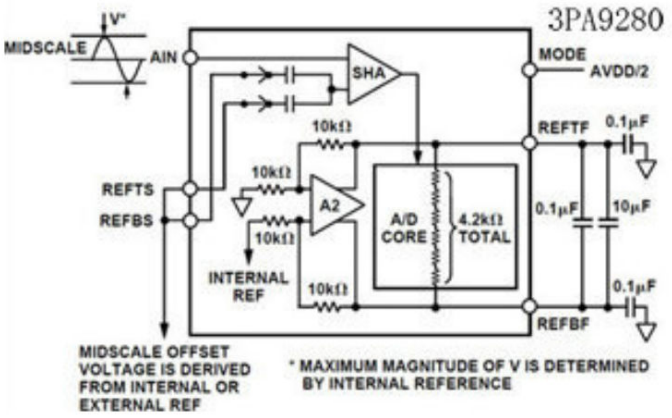


Figure 15 (b). Center Span Mode

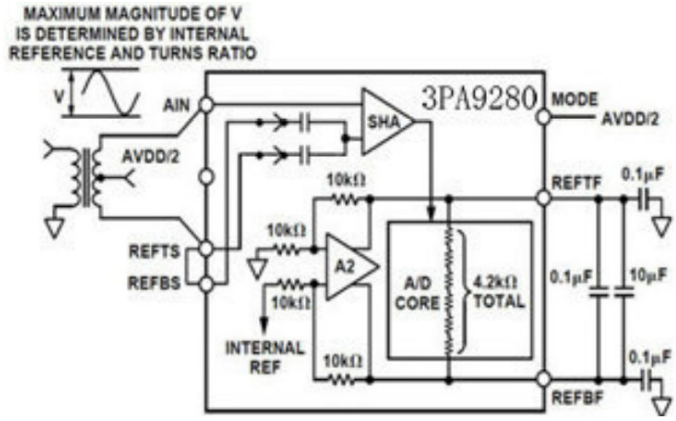


Figure 15 (c). Differential Mode

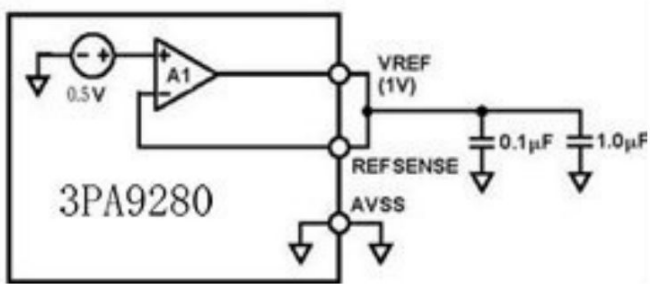


Figure 15 (d). 1-V Reference

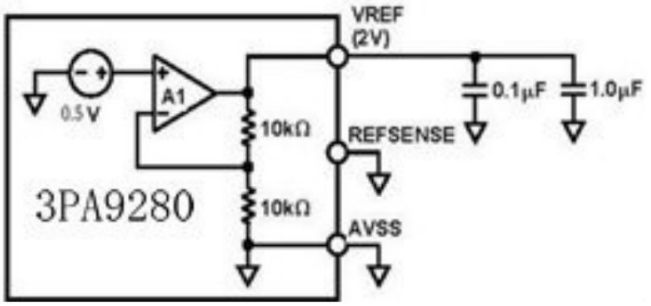


Figure 15 (e). 2-V Reference

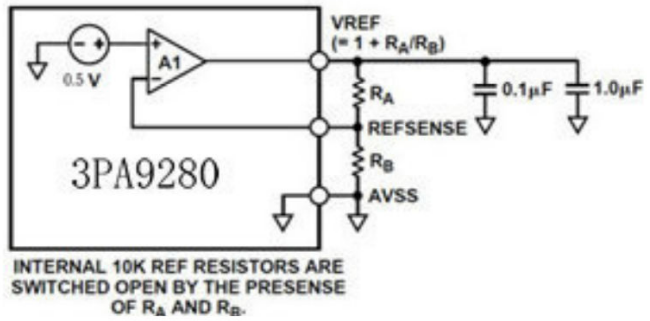


Figure 15 (f). Variable Reference (between 1 V and 2 V)

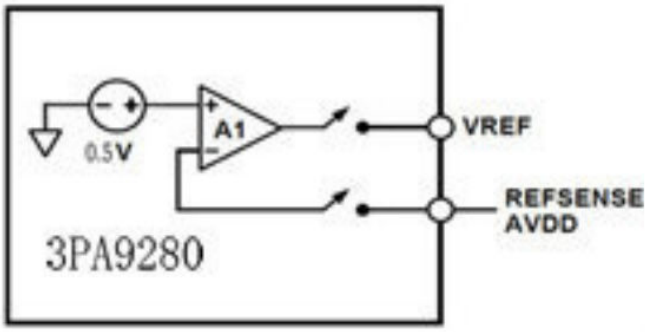


Figure 15 (g). Internal Reference Disable (Power Reduction)

Figure 15. a~g

The actual reference voltages used by the internal circuitry of the 3PA9280 appear on REFTF and REFBF. For proper operation, it is necessary to add a capacitor network to decouple these pins. REFTF and REFBF should be decoupled for all internal and external configuration as shown in Figure 16.

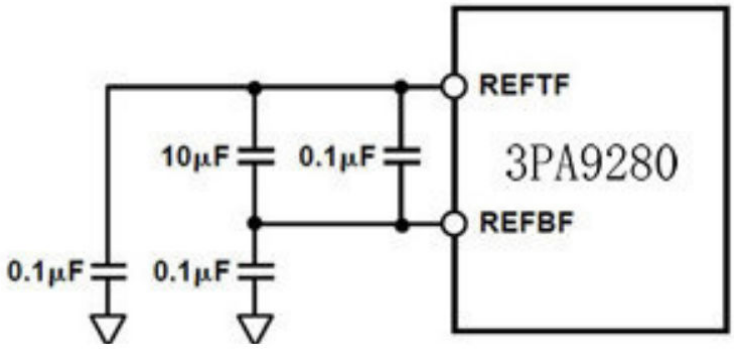


Figure 16. Reference Decoupling Network

Note:

REFTF = reference top, force REFBF = reference bottom, force

REFTS = reference top, sense REFBS = reference bottom, sense

Internal Reference Operation

Figure 17, Figure 18, and Figure 19 show sample connections of the 3PA9280 internal reference in its most common configurations. (Figure 17 and Figure 18 illustrate the top/bottom mode, while Figure 19 illustrates the center span mode). Figure 28 shows how to connect the 3PA9280 for 1-Vp-p differential operation. Shorting the VREF pin directly to the REFSENSE pin places the internal reference amplifier (A1) in unity-gain mode, and the resultant reference output is 1 V. In Figure 17, REFBS is grounded to give an input range from 0 V to 1 V. These modes can be chosen when the supply is either +3 V or +5 V. The VREF pin must be bypassed to AVSS (analog ground) with a 1.0-F tantalum capacitor in parallel with a low inductance, a low ESR, and a 0.1-µF ceramic capacitor.

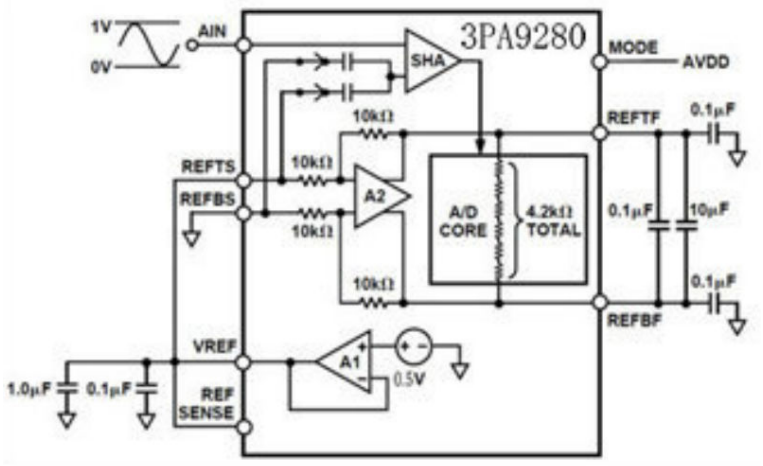


Figure 17. Internal Reference—1-Vp-p Input Span (Top/Bottom Mode)

Figure 18 shows the single-ended configuration for 2-Vp-p operation. REFSENSE is connected to GND, resulting in a 2-V reference output.

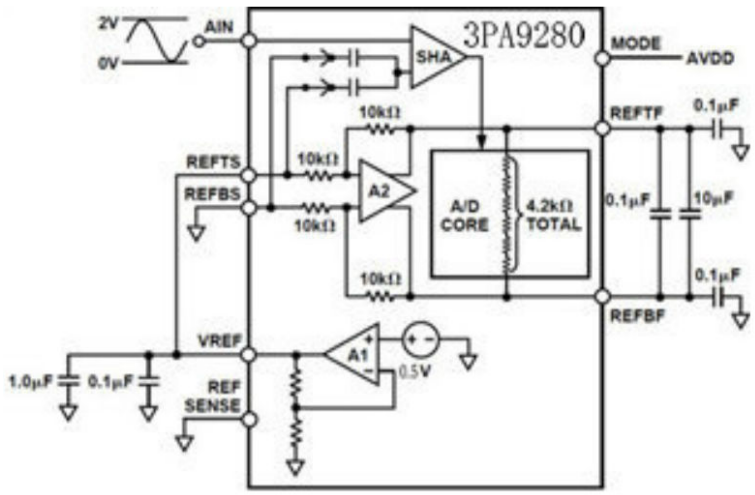


Figure 18.

Figure 19 shows the single-ended configuration that provides high-frequency dynamic performance (SINAD, SFDR). To optimize dynamic performance, center the common-mode voltage of the analog input at approximately 1.5 V. Connect the shorted REFTS and REFBS inputs to a low-impedance 1.5-V source. In this configuration, the MODE pin is driven to a voltage at midsupply (AVDD / 2). The maximum reference drive is 1 mA. An external buffer is required for heavier loads.

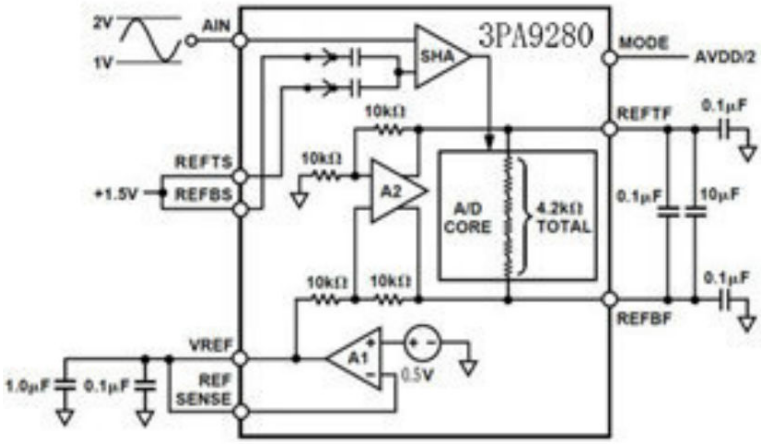


Figure 19. Internal Reference 1-Vp-p Input Span (Center Span Mode)

External Reference Operation

Using an external reference may provide more flexibility and improve drift and accuracy. Figure 20 show examples of how to use an external reference with the 3PA9280. To use an external reference, users must disable the internal reference amplifier by connecting the REFSENSE pin to V_{DD}, and drive the VREF pin with user-defined reference voltage.

The 3PA9280 contains an internal reference buffer (A2) that simplifies the drive requirements of an external reference. The external reference must simply be able to drive a 10-k load.

Figure 20 shows an example of an external reference generating 2.5 V at the shorted REFTS and REFBS inputs. In this instance, a REF43 2.5-V reference drives REFTS and REFBS. A resistive divider generates a 1-V VREF signal that is buffered by A3. A3 must be able to drive a 10-k capacitive load. Choose this op amp based on noise and accuracy requirements.

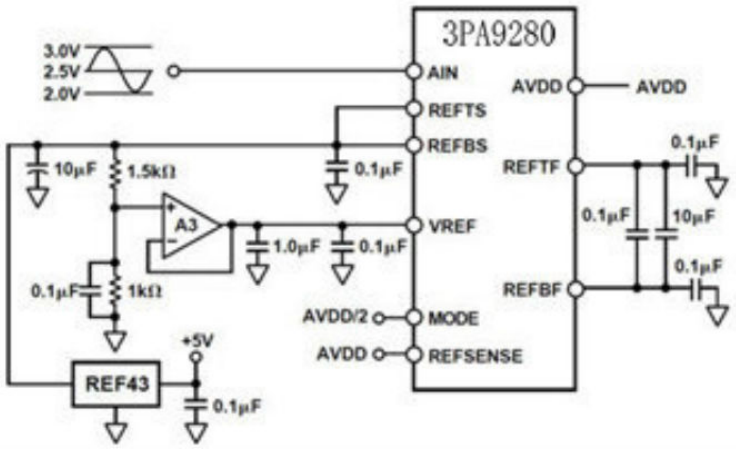


Figure 20. External Reference Mode—1-Vp-p Input Span 2.5 V_{CM}

Standby Operation

The ADC may be placed into the power-down (sleep) mode by driving the STBY (standby) pin to logic-high potential and holding the clock at logic low. In this mode, the typical power drain is approximately 4 mW. The ADC "wakes up" in 400 ns (typ) after the standby pulse goes low.

Clamp Operation

The 3PA9280 may be driven with a DC-coupled or AC-coupled input signal. When the input signal is AC-coupled, it features a flexible bottom-level clamp circuit for DC restoration of the signal. Figure 21 shows the external control signals needed for clamp operation. In AC-coupled cases, when a logic high or a pulse such as the H-sync in video systems is applied to the CLAMP pin, the bottom level of the signal AIN is clamped to the voltage provided at the CLAMPIN pin (see Figure 21 (a)). The allowable voltage range that can be applied to CLAMPIN depends on the operational limits of the internal clamp amplifier. The recommended clamp range is between 0 V and 1.0 V. The logic-high CLAMP control might be useful for some video applications, since the H-sync generating circuitry may be omitted. When a logic low is applied to the CLAMP pin (see Figure 21 (b)), the bottom level of the signal AIN is clamped to a ground level. When the input is DC-coupled, CLAMP is recommended to be shorted to logic low (see Figure 21 (c)). The DC input signal level needs to be higher than 0 V.

The input capacitor should be sized to allow sufficient acquisition time of the clamp voltage at AIN within the CLAMP interval, but also be sized to minimize droop between clamping intervals. For video applications, an input capacitor of 0.1 µF is recommended.

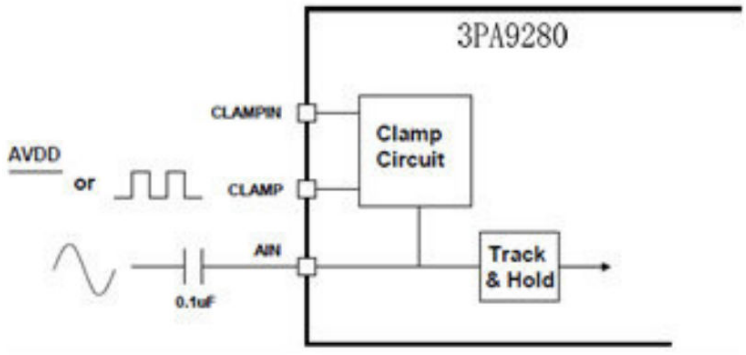


Figure 21 (a). Bottom Signal Level Clamped to CLAMPIN

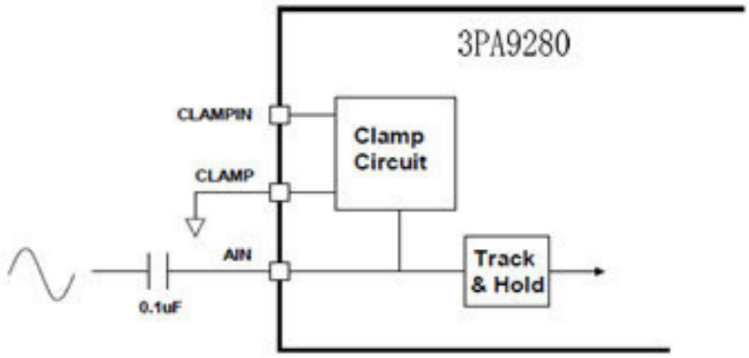


Figure 21 (b). Bottom Signal Level Clamped to Ground

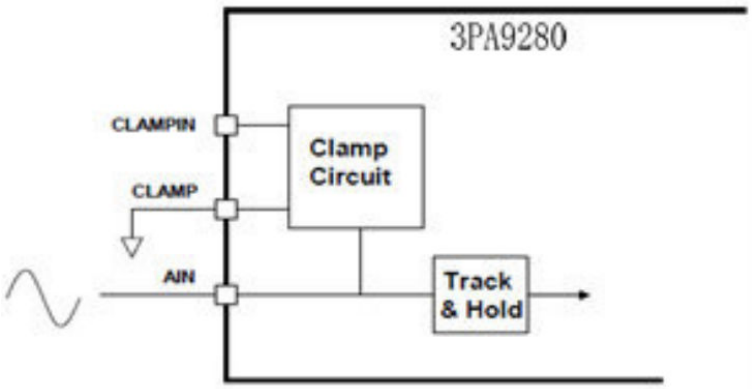


Figure 21 (c). DC-Coupled Input

Figure 21. a~c

Driving the Analog Input

Figure 24 shows the equivalent analog input of the 3PA9280, a sample-and-hold amplifier (switched capacitor input SHA). Bringing CLK to a logic-low level closes Switches 1 and 2, and opens Switch 3. The input source connected to AIN must charge the capacitor CH during this time. When CLK transitions from logic "low" to logic "high", Switches 1 and 2 open, placing the SHA in hold mode. Switch 3 then closes, forcing the output of the op amp to equal the voltage stored on CH. When CLK transitions from logic "high" to logic "low", Switch 3 opens first. Switches 1 and 2 close, placing the SHA in track mode.

The structure of the input SHA places certain requirements on the input drive source. The combination of the pin capacitance (CP) and the hold capacitance (CH) is typically less than 5 pF. The input source must be able to charge or discharge this capacitance to 8-bit accuracy in one half of a clock cycle. When the SHA goes into track mode, the input source must charge or discharge the capacitor CH from the voltage already stored on CH to the new voltage. In the worst case, a full-scale voltage step on the input, the input source must provide the charging current through the RON (50) of Switch 1 and quickly (within 1/2 CLK period) settle. This situation corresponds to driving a low-input impedance. On the other hand, when the source voltage equals the value previously stored on CH, the hold capacitor requires no input current, and the equivalent input impedance is extremely high.

Adding series resistance between the output of the source and the AIN pin reduces the drive requirements placed on the source. Figure 22 shows this configuration. The bandwidth of the particular application limits the size of this resistor. To maintain the performance outlined in the data sheet specifications, the resistor should be limited to 20 or less. For applications with signal bandwidths less than 16 MHz, users may proportionally increase the size of the series resistor.

Alternatively, adding a shunt capacitance between the AIN pin and analog ground lowers the AC load impedance. The value of this capacitance depends on the source resistance and the required signal bandwidth. The input span of the 3PA9280 is a function of the reference voltages. For more information about the input range, see the following sections.

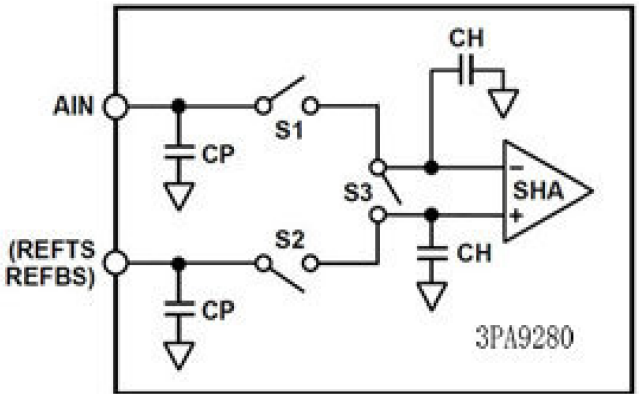


Figure 22. 3PA9280 Equivalent Input Structure

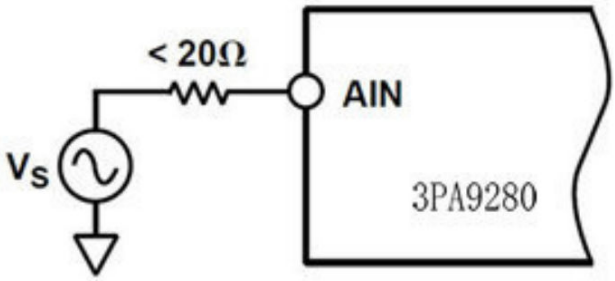


Figure 23. Simple 3PA9280 Drive Configuration

In many cases, particularly in single-supply operation, AC coupling offers a convenient way of biasing the analog input signal at the proper signal range. Figure 24 shows a typical configuration for AC-coupling the analog input signal to the 3PA9280. Maintaining the specifications outlined in the data sheet requires careful selection of the component values. The most important is the f–3 dB high-pass corner frequency. It is a function of R2 and the parallel combination of C1 and C2. The f–3 dB point can be approximated by Equation 3:

$$f_{-3\,dB} = 1/(2 \times pi \times [R2]C_{EQ}) \quad (3)$$

Where C_{EQ} is the parallel combination of C1 and C2. Note that C1 is typically a large electrolytic or tantalum capacitor that becomes inductive at the high frequencies. Adding a small ceramic or polystyrene capacitor (approximately 0.01 F) that does not become inductive until at negligibly higher frequencies, maintains a low impedance over a wide frequency range.

NOTE: AC-coupled input signals may also be shifted to a desired level with the internal clamp of the 3PA9280. See Clamp Operation.

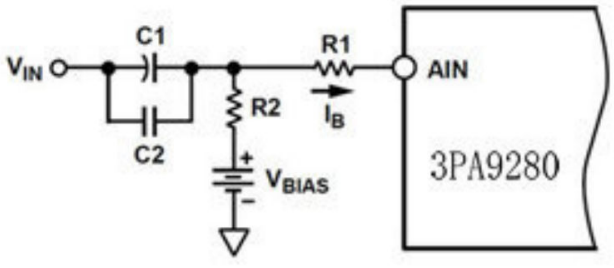


Figure 24. AC-Coupled Input

There are additional considerations when choosing the resistor values. The AC-coupling capacitors integrate the switching transients present at the input of the 3PA9280, and cause a net DC bias current (IB) to flow into the input. The magnitude of the bias current increases as the signal magnitude deviates from V midscale and the clock frequency increases; i.e., minimum bias current flow when AIN = V midscale. This bias current results in an offset error of (R1 + R2) × IB. If it is necessary to compensate this error, consider making R2 negligibly small or modifying VBIAS to account for the resultant offset.

In systems that must use DC coupling, use an op amp to level-shift a ground-referenced signal to comply with the input requirements of the 3PA9280. Figure 25 shows an AD8041 configured in non-inverting mode.

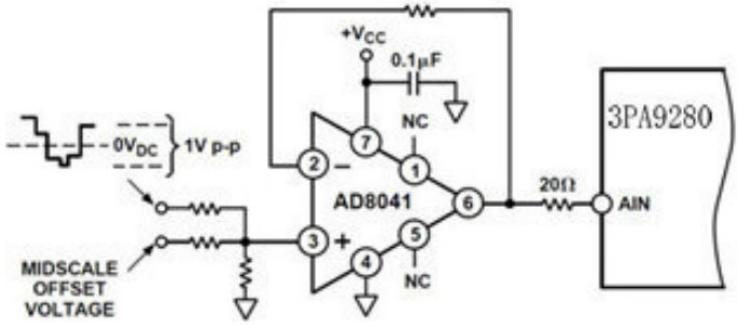


Figure 25. Bipolar Level Shift

Differential Input Operation

The 3PA9280 accepts differential input signals. This function may be used by shorting REFTS and REFBS and driving them as one leg of the differential signal (the top leg is driven into AIN). In the configuration below, the 3PA9280 is accepting a 1-Vp-p signal. See Figure 26.

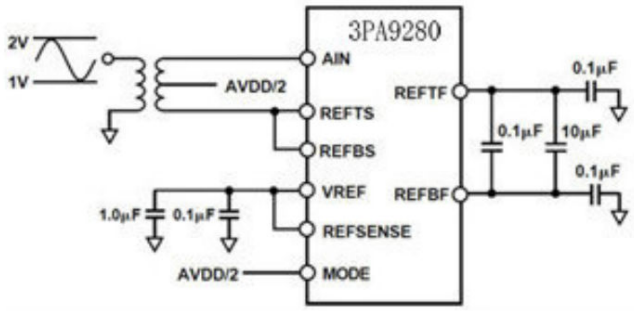


Figure 26. Differential Input

Clock Input

The 3PA9280 clock input is buffered internally with an inverter powered from the AVDD pin. This feature allows the 3PA9280 to accommodate 5-V or 3.3-V CMOS logic input signal swings with the input threshold for the CLK pin nominally at AVDD / 2 as Figure 27.

The pipelined architecture of the 3PA9280 operates on both rising and falling edges of the input clock. To minimize duty cycle variations, the recommended logic family to drive the clock input is high speed or advanced CMOS (HC/HCT, AC/ACT) logic. CMOS logic provides both symmetrical voltage threshold levels and sufficient rise and fall times to support 32-MSPS operation. The 3PA9280 is designed to support a conversion rate of 32 MSPS; running the part at slightly faster clock rates may be possible, although at reduced performance levels. Conversely, some slight performance improvements might be realized by clocking the 3PA9280 at slower clock rates.

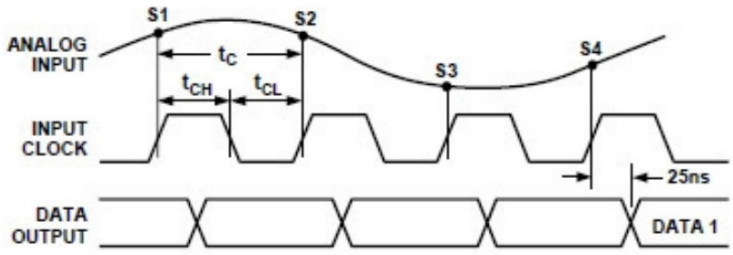


Figure 27. Timing Diagram

The power dissipated by the output buffers is largely proportional to the clock frequency; running at reduced clock rates reduces power consumption.

Digital Inputs and Outputs

The baseband region of the ADC. A trade-off exists between the complexity of this image rejection filter and the sample rate as well as dynamic range of the ADC. For each of the 3PA9280 digital control inputs, THREE-STATE and STBY are reference to the analog ground. The clock is also referenced to the analog ground. The format of the digital output is straight binary (see Figure 28). A low-power mode feature is provided so that STBY = HIGH, the clock is disabled, the static power of the 3PA9280 drops below 5 mW.

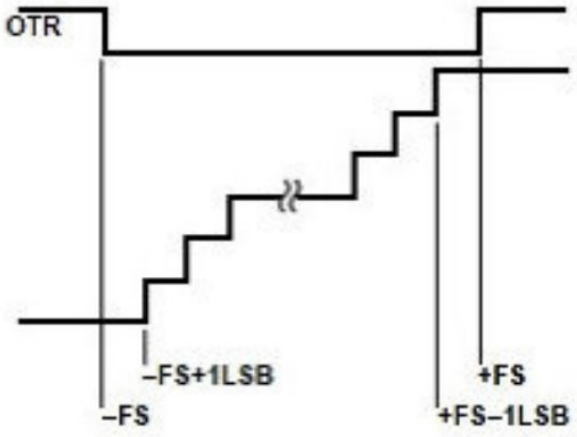


Figure 28. Output Data Format

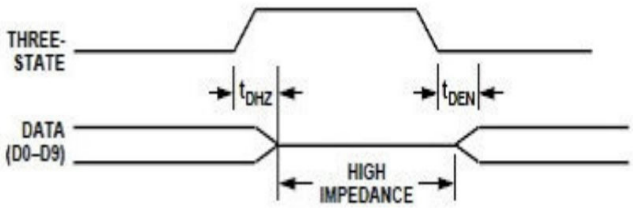


Figure 29. Three-State Timing Diagram

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

Direct If Down Conversion Using the 3PA9280

Sampling IF signals above the baseband region of an ADC (i.e., DC to FS / 2) is becoming increasingly popular in communication applications. This process is often referred as direct If down conversion or under sampling. There are several potential benefits when using the ADC to alias (i.e., or mix) down a narrowband or wideband IF signal. First and foremost is the elimination of a complete mixer stage with its associated amplifiers and filters, reducing cost and power dissipation. Second is the ability to apply various DSP techniques to perform such functions as filtering, channel selection, quadrature demodulation, data reduction, detection, etc.

In direct IF down conversion applications, one exploits the inherent sampling process of an ADC in which an IF signal lying outside the baseband region can be aliased back into the baseband region in a similar manner that a mixer down converts an IF signal. Similar to the mixer topology, an image rejection filter is required to limit other potential interfering signals from also aliasing back into. The 3PA9280 is well suited for various narrowband IF sampling applications. The low-distortion input SHA of the 3PA9280 has a full-power bandwidth extending to 300 MHz, encompassing many popular IF frequencies. The 3PA9280 typically yields an improvement in SNR when configured for the 2-V span, and the 1-V span provides optimum full-scale distortion performance. Furthermore, the 1-V span reduces the performance requirements of the input driver circuitry, and thus may be more practical for system implementation purposes.

Figure 30 shows a simplified schematic of the 3PA9280 configured in an IF sampling application. To reduce the complexity of the digital demodulator in many quadrature demodulation applications, the IF frequency and/or sample rate are selected so that the bandlimited IF signal aliases back into the center of the baseband region of the ADC (i.e., FS/4). For example, if an IF signal centered at 45 MHz is sampled at 20 MSPS, an image of this IF signal is aliased back to 5.0 MHz which corresponds to one quarter of the sample rate (i.e., FS / 4). This demodulation technique typically reduces the complexity of the post digital demodulator ASIC which follows the ADC.

To maximize its distortion performance, the 3PA9280 is configured in the differential mode with a 1-V span using a transformer. The center tap of the transformer is biased at midsupply via a resistor divider. Preceding the 3PA9280 is a bandpass filter as well as a 32dB gain stage. A large gain stage may be required to compensate for the high insertion losses of a SAW filter used for image rejection. The gain stage also provides adequate isolation for the SAW filter from the charge "kick back" currents associated with the input stage of the 3PA9280.

The gain stage can be realized by using one or two cascaded AD8009 operational amplifiers. The AD8009 is a low-cost, 1-GHz, current-feedback op amp having a 3rd-order intercept characterized by up to 250 MHz. A passive bandpass filter following the AD8009 attenuates its dominant 2nd-order distortion products which are otherwise aliased back into the baseband region of the 3PA9280. Also, it reduces any out-of-band noise which is also be aliased back due to the noise bandwidth of 220+ MHz of the 3PA9280. Note, the bandpass filters specifications are application-dependent, and affect both the total distortion and noise performance of this circuit.

The distortion and noise performance of an ADC at the given IF frequency is of particular concern when evaluating an ADC for a narrowband IF sampling application. Both single-tone and dual-tone SFDR vs. amplitude are very useful in assessing the noise performance of the ADC and noise contribution due to aperture jitter. In any application, one is advised to test several units of the same device under the same conditions to evaluate the given applications sensitivity to that particular device.

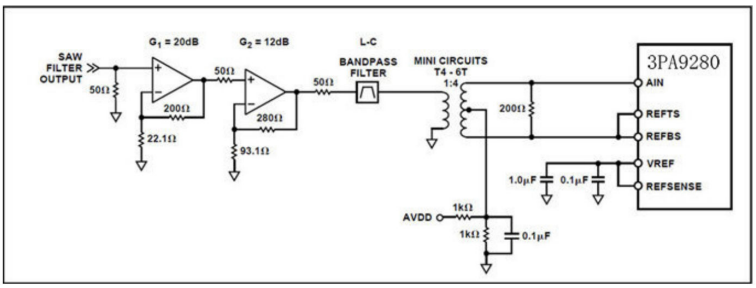


Figure 30. Simplified 3PA9280 IF Sampling Circuit

Figure 31 to Figure 34 combine the dual-tone SFDR and single-tone SFDR and SNR performance at IF frequencies of 45 MHz, 70 MHz, 85 MHz, and 135 MHz. Note, the SFDR vs. amplitude data is referenced to dBFS while the single tone SNR data is referenced to dBc.

The 3PA9280 is operated in differential mode (via the transformer) with a 1-V span. The analog supply (AVDD) and the digital supply (DRVDD) are set to +5 V and 3.3 V, respectively.

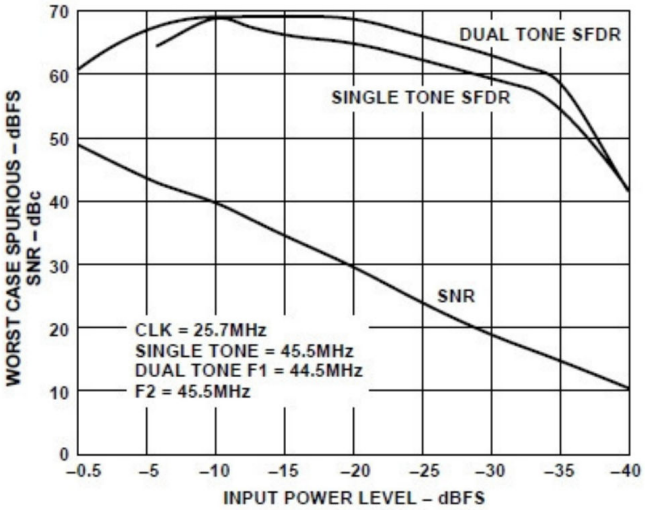


Figure 31. NR/SFDR for IF @ 45 MHz

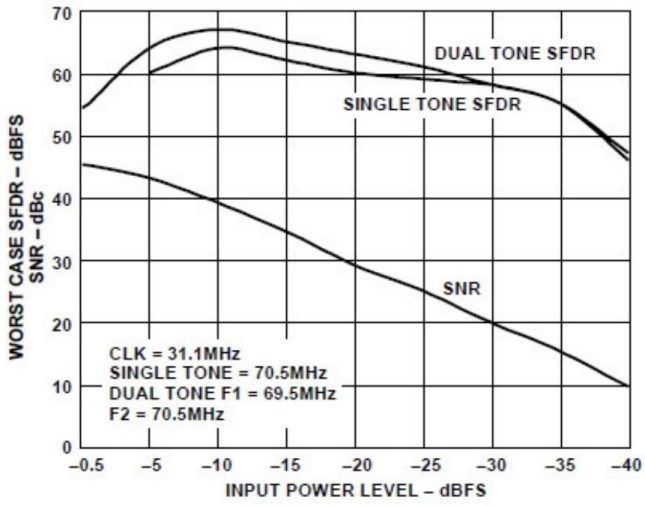


Figure 32. SNR/SFDR for IF @ 70 MHz

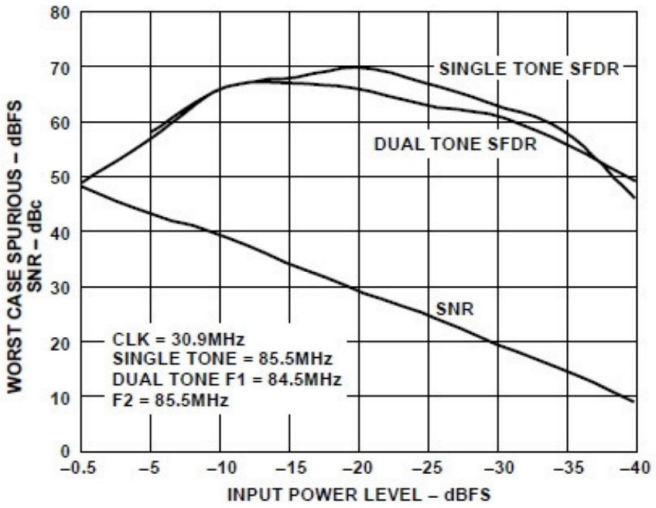


Figure 33. SNR/SFDR for IF @ 85 MHz

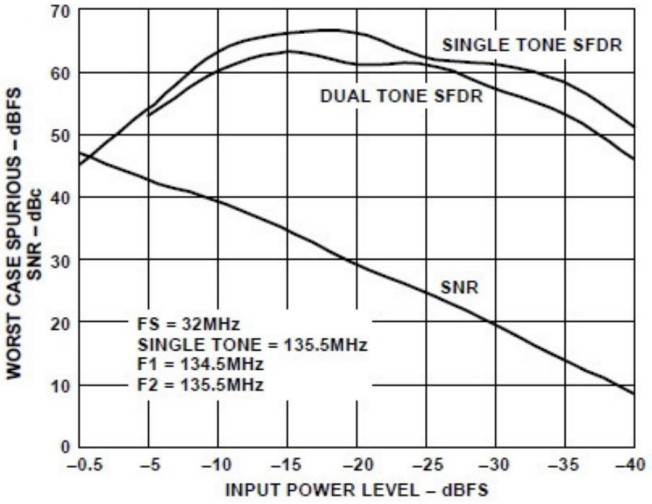


Figure 34. SNR/SFDR for IF @ 135 MHz

Grounding and Layout Rules

As is the case for any high-performance device, proper grounding and layout techniques are essential in achieving optimal performance. The analog and digital grounds on the 3PA9280 are separated to optimize the management of return currents in a system. Grounds should be connected near the ADC. It is recommended that a printed circuit board (PCB) of at least four layers, employing a ground plane and power planes, be used with the 3PA9280. The use of ground and power planes offers distinct advantages:

- The minimization of the loop area encompassed by a signal and its return path.
- The minimization of the impedance associated with ground and power paths.
- The inherent distributed capacitor formed by the power plane, PCB insulation, and ground plane.

These characteristics reduce the electromagnetic interference (EMI) and improve the overall performance.

It is important to design a layout that prevents noise from coupling onto the input signal. Digital signals should not be run in parallel with the input signal traces, and should be routed away from the input circuitry. Separate analog and digital grounds should be joined together directly under the 3PA9280 in a solid ground plane. The power and ground return currents must be

carefully managed. A general rule of thumb for mixed signal layouts dictates that the return currents from the digital circuitry should not pass through the critical analog circuitry.

Digital Outputs

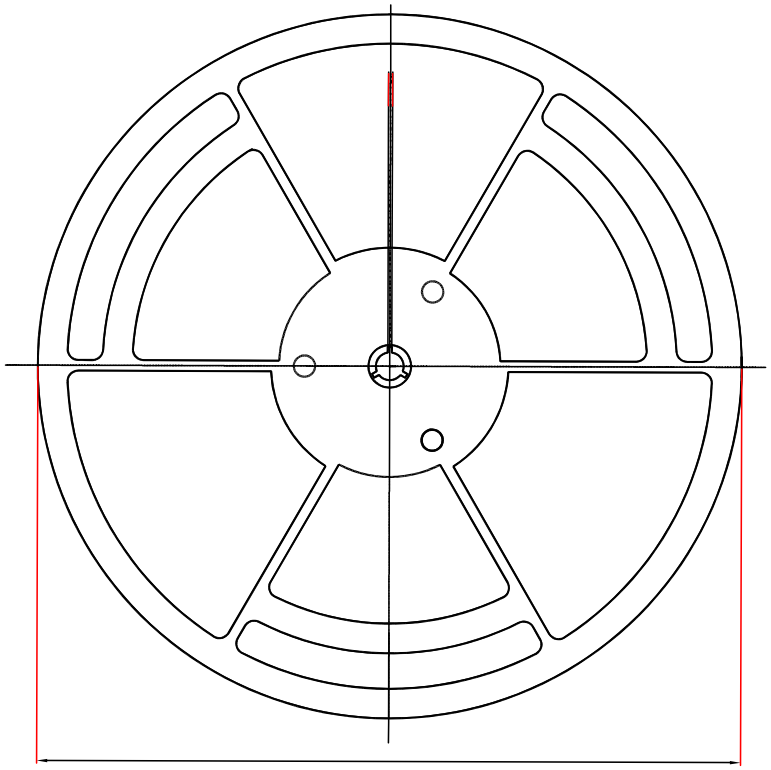
Each of the on-chip buffers for the 3PA9280 output bits (D0-D7) is powered from the DRVDD supply pins, separate from AVDD. The output drivers are sized to handle a variety of logic families while minimizing the amount of glitch energy generated. In all cases, a fan-out of one is recommended to keep the capacitive load on the output data bits below the specified 20-pF level.

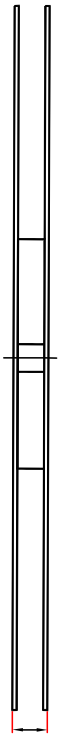
When DRVDD = 5 V, the 3PA9280 output signal swing is compatible with both high-speed CMOS and TTL logic families. For TTL, the 3PA9280 on-chip output drivers are designed to support several high-speed TTL families (F, AS, S). For applications where the clock rate is below 32 MSPS, other TTL families may be appropriate. When interfacing with lower-voltage CMOS logic, the 3PA9280 sustains 32-MSPS operation with DRVDD = 3 V. In all cases, check the logic family data sheets for compatibility with the 3PA9280 Digital Specification table.

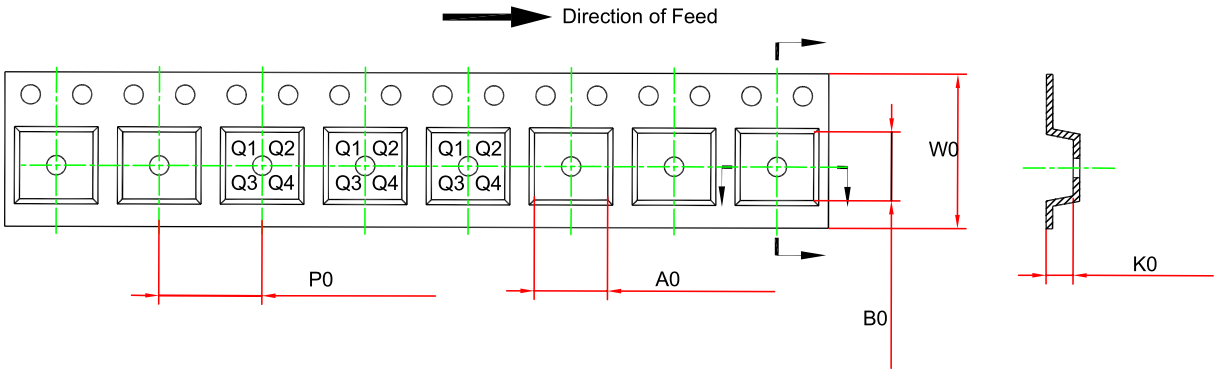
Three-State Outputs

The digital outputs of the 3PA9280 can be placed in a high-impedance state by setting the THREE-STATE pin to high. This feature is provided.

Tape and Reel Information







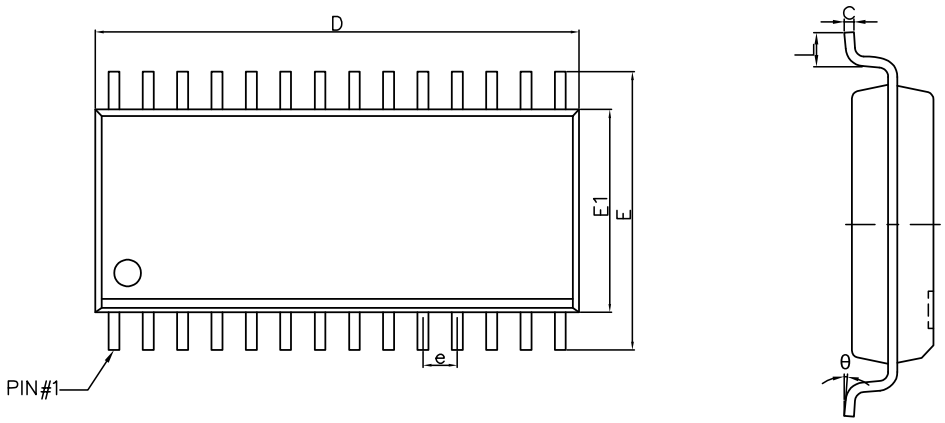
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm) (1)	B0 (mm) (1)	K0 (mm) (1)	P0 (mm)	W0 (mm)	Pin1 Quadrant
3PA9280	SSOP28	330	21.6	8.2	10.5	2.34	12	16	Q1

(1) The value is for reference only. Contact the 3PEAK factory for more information.

Package Outline Dimensions

SSOP28

Package Outline Dimensions SS6(SSOP-28-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	---	2.000	---	0.787
A1	0.050	---	0.002	---
A2	1.650	1.850	0.065	0.073
b	0.220	0.380	0.009	0.015
c	0.090	0.250	0.004	0.010
D	9.900	10.500	0.390	0.413
E	7.400	8.200	0.291	0.323
E1	5.000	5.600	0.197	0.220
e	0.650 BSC		0.026 BSC	
L	0.550	0.950	0.022	0.037
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
3PA9280	−40 to 85°C	SSOP28	3PA9280	3	2000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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