TPS325M5A Mixed-Signal Microcontrollers

156 MHz, up to 512 KB Flash, 336 KB SRAM, based on ARM Core, TPSensor, rich analog, optimized for HMI

1 Overview

1.1 Features

- MCU Core:
  - 32-bit STAR-MC1 core with FPU based on Arm® v8-M architecture, frequency up to 156 MHz
  - Compatible with Cortex®-M33 instruction set
- Operating conditions:
  - V_{DD}, V_{DDA} power supply voltage: 1.71 V to 3.6 V
- Memories
  - 512 KB of Flash memory
  - SRAM memory
    - 192 KB SRAM0
    - 128 KB SRAM1
    - 16 KB SRAM2 for retention
  - Quad-SPI memory interface
- Reset and supply management
  - Power-on/Power-down/Brown-out Reset (POR/PDR/BOR)
  - Supply Voltage Supervisor (SVS)
  - Low-power modes: Sleep, stop, standby and shutdown
  - V_{BAT} supply for RTC and backup registers
  - Active power: 107 uA/MHz
  - Standby power: 3 uA with RTC sourced from 32 kHz crystal, 16 KB retention SRAM
  - Shutdown power: 2.6 uA with RTC sourced from ILS
- Clock management
  - 4 ~ 32 MHz External High-Speed (EHS) crystal oscillator
  - 32 kHz External Low-Speed (ELS) oscillator
  - Internal High-Speed (IHS) 8 MHz RC oscillator (±0.5% tolerance at 30℃ on 3 V power supply)
  - Phase Lock Loop (PLL)
  - Internal Low-Speed (ILS) 32 kHz RC oscillator (±3% tolerance at 30℃ cross power supply voltage)
- Up to 56 I/Os
  - All mappable on external interrupt vectors
  - Several I/Os with 5 V tolerant capability, refer to Pinout Table for details
- Dual-DMA controller with 8-channel each
- 1 x 12-bit ADC with 14-external and 6-internal channels, up to 12-bit resolution at 2.5 Msps sampling rate. Temperature sensor integrated with ±2°C accuracy
- 1 x 12-bit DAC with 1 Msps, support 2 x buffered external channels
- 2 x fast rail-to-rail analog Comparators (CMPs) with built-in 6-bit DAC for internal voltage reference
- 2 x Operational Amplifiers (OAs) that can be used in PGA mode, buffer mode
- TPSensor® with high noise immunity
  - Support self and mutual capacitive sensing mode
  - Up to 13 channels (including one Guard channel)
  - One Shield channel for moisture tolerant
  - Wake on touch
  - Ultra-low power mode: 5 uA/Button @ 5Hz scan rate
- Internal Voltage Reference Buffer (VREFBUF) supporting three output voltages (1.5 V, 2.0 V, 2.5 V)
- 13 x Timers:
  - 5 x 16-bit General-Purpose Timers (GPTMRs) with 7-channel compare/capture each
  - 1 x 32-bit General-Purpose Timer (GPTMR) with 7-channel compare/capture each
  - 3 x 16-bit Advanced Timers (ADVTMRs), with up to 7 x PWM channels per each, dead time regeneration and emergency stop
  - 1 x Independent Watchdog timer (IWDG)
  - 1 x Window Watchdog timer (WWDG)
  - 1 x SysTick timer: 24-bit down-counter
  - 1 x RTC calendar with alarm, periodic wakeup from stop/standby
- Serial communication interfaces
  - 2 x I2C Fast-mode Plus (Fm+, 1 Mbit/s) with 20 mA current sink, SMBus/PMBus, wakeup from stop mode
  - 6 x UART (support LIN, modem control)
  - 3 x SPI/I2S
  - 1 x CAN2.0B
- Crypto engine
  - True Random Number Generator (TRNG)
  - AES: 128/192/256-bit key encryption hardware accelerator

  - HASH: SHA1/SHA2, MD5
- Cyclic Redundancy Check (CRC) calculation unit
- 96-bit unique Chip ID
- Development support: Serial Wire Debug (SWD)/JTAG, Embedded Trace Macrocell™
- Operation temperature: −40°C ~ +105°C
- Package options:
  LQFP-64

1.2 Package Options

Package Type	Pitch	Length	Width	Height	Unit
LQFP-64	0.5	10	10	1.5	mm

1.3 Description

The TSP325M5A device is based on the high-performance Arm® STAR 32-bit RISC core, operating at a frequency of up to 156 MHz. The ARM STAR core features a single-precision Floating-Point Unit (FPU) that supports all Arm single-precision data-processing instructions and data types. It also includes a full set of Digital Signal Processing (DSP) instructions and a Memory Protection Unit (MPU) to enhance application security.

The device embeds high-speed memories (512 KB of Flash memory and 336 KB of SRAM), a Quad SPI Flash memory interface, an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and 32-bit multi-AHB bus matrix.

The devices also incorporate several protection mechanisms for embedded Flash memory and SRAM, including readout protection, write protection, securable memory area, and proprietary code readout protection.

They offer a high-resolution of up to 12-bit Analog-to-Digital Converter (ADC), a Digital-to-Analog Converter (DAC) with 2-channels switchable output, two Comparators (CMPs) with built-in 6-bit Digital-to-Analog Converter (DAC), two Operational Amplifiers (OAs), an internal Voltage Reference Buffer (VREFBUF), a low-power Real-Time Clock (RTC), six 16/32-bit General-Purpose Timers (GPTMRs), three 16-bit Advanced Timers (ADVTMRs) PWM dedicated to motor control.

In addition, the devices offer a range of standard and advanced communication interfaces, including:

- Two I2Cs
- Three SPIs multiplexed with I2S
- Six UARTs
- One CAN2.0B interface

Furthermore, the devices incorporate a built-in Crypto Engine with True Random Number Generator (TRNG), Advanced Encryption Standard (AES), and HASH (SHA1/SHA2, MD5) modules for enhanced security and encryption capabilities.

The device operates within a temperature range of -40 to +105 °C (+125°C junction) and can be powered by a supply voltage ranging from 1.71 to 3.6 V. To support low-power applications, a comprehensive set of power-saving modes is available. The devices also support independent power supplies, including an analog independent supply input for ADC, DAC, OA and CMP. Additionally, a VBAT input allows for backup of the RTC and registers. The TSP325M5A family is available in a 64-pin configuration.

1.4 Functional Block Diagram

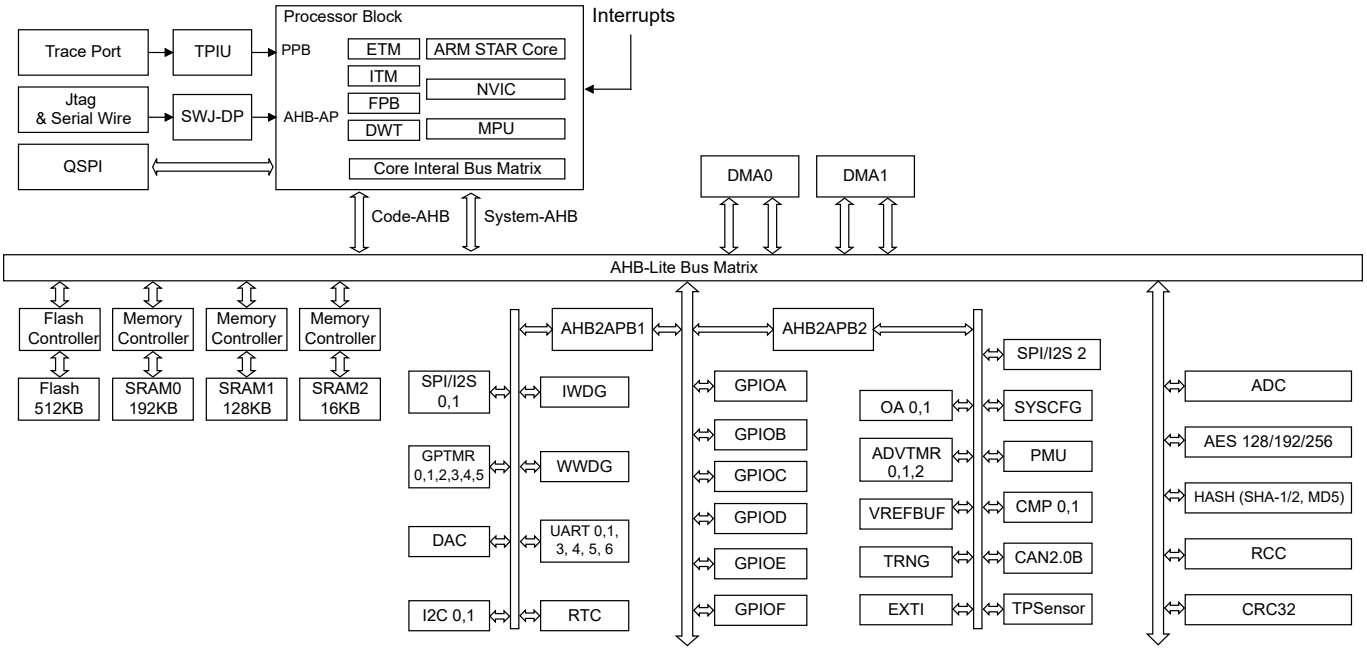


Figure 1. TSP325M5A Block Diagram

Table of Contents

2 Device Comparison

Part Number	Flash (KB)	RAM (KB)	ADC	TPSensor®	CAN	DAC	OA	CMP	QSPI	SPI/I2S	I2C	UART	GPTMR	ADVTMR	Total GPIO	Package Type
TPS325M5A57Q-QP5T	512	336	1 x 12bit @ 1Msps SAR ADC	1x12ch	1 x CAN 2.0B	1 x 12bit	2	1	1	3	2	6	6	3	56	LQFP64

3 Revision History

Date	Revision	Notes
2023-11-30	Rev.A.0	Initial released.

4 Functional Overview

4.1 Arm® STAR Core With FPU

The Arm® STAR with FPU processor is the Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of the MCU implementation, with a reduced pin count and with low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts. The Arm® STAR with FPU 32-bit RISC processor features an exceptional code-efficiency, delivering the expected high-performance from an Arm core in a memory size usually associated with 8-bit and 16-bit devices. The processor supports a set of DSP instructions which allows an efficient signal processing and a complex algorithm execution. Its single precision FPU speeds up the software development by using metalanguage development tools to avoid saturation.

With its embedded Arm core, the TSP325M5A family is compatible with all Arm tools and software.

4.2 Memory

4.2.1 Embedded Flash Memory

The TSP325M5A device features 512 KB of embedded Flash memory, which is available for storing both programs and data.

The option bytes enable the configuration of flexible protections:

- Readout Protection (RDP) protects the whole memory. Three levels of protection are available:
  - Level 0: No readout protection.
  - Level 1: Memory readout protection; the Flash memory is inaccessible for reading or writing if either the debug features are activated or the boot in RAM or bootloader is selected.
  - Level 2: Chip readout protection; the debug feature (JTAG or SWD), boot in RAM, and bootloader selection are disabled.

  This selection is irreversible.
- Write Protection (WRP): The protected area is protected against erasing and programming.

4.2.2 Embedded SRAM

The TSP325M5A devices embedded SRAM. This SRAM is divided into three blocks: SRAM0 with 192 KB, SRAM1 with 128 KB, and SRAM2 with 16 KB for retention. The SRAM memory can be accessed in read/write at maximum CPU clock speed with zero wait state.

4.2.3 Memory Organization

Block	Flash Memory Addresses	Size (Bytes)	Name
Main memory (512 KB, DBANK = 0, single-bank)	0x0800 0000 - 0x0800 1FFF	8K	Sector 0
	0x0800 2000 - 0x0800 3FFF	8K	Sector 1
	0x0800 4000 - 0x0800 5FFF	8K	Sector 2
	0x0800 6000 - 0x0800 7FFF	8K	Sector 3
	-	-	-
	0x0807 0000 - 0x0807 FFFF	8K	Sector 63
System memory	0x0FFE 0000 - 0x0FFE 7FFF	32K	System memory(1)
Option bytes	0x0FFE 8000 - 0x0FFE 805F	96	Option bytes
OTP	0x0FFE 9000 - 0x0FFE 93FF	1K	OTP area(2)
	0x0FFE 9400 - 0x0FFE 940F	16	OTP LOCK(3)

(1) 3PEAK bootloader.
(2) 1 KB One-Time Programmable (OTP) bytes for user data. The OTP data cannot be erased and can be written only once. If only one bit is at 0, the entire double word cannot be written anymore.
(3) 16 bytes OTP LOCK, each byte lock 64 bytes in the OTP area.

Table 1. Open Info

Item	Address	Description
Device info0	0x 4001 3100	Device ID (Chip ID)
Device info1	0x 4001 3104	HW_Revision & FW_Revision
Device info2	0x 4001 3108	DIE_X_Poisition & DIE_Y_Position (Chip ID)
Device info3	0x 4001 310C	LOT_Wafer_ID (Chip ID)

4.2.4 Memory Map

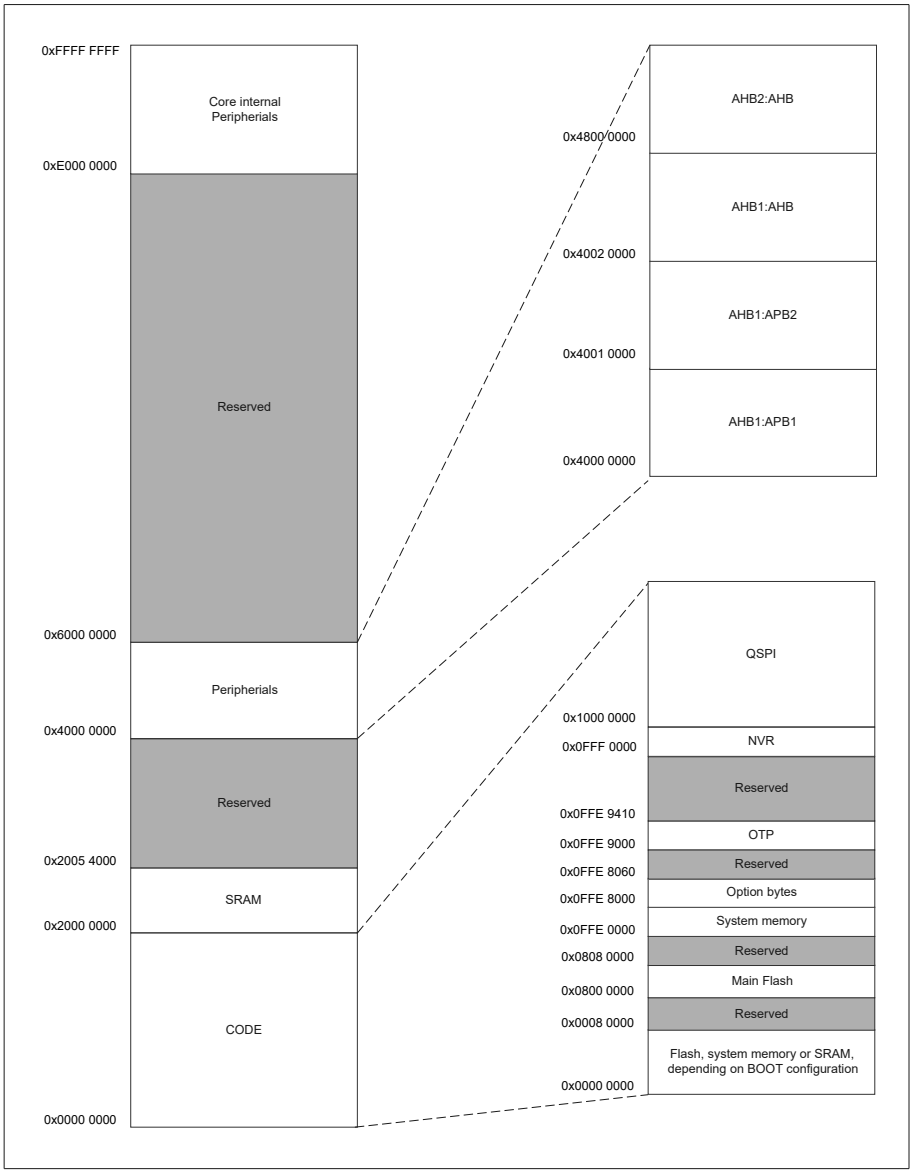


Figure 2. Memory Map

Bus	Boundary Address	Size (Bytes)	Destination Slave
Core PPB	0xE00F F000 – 0xE00F FFFF	4KB	Processor ROM table
	0xE004 4000 – 0xE004 4FFF	4KB	QSPI
	0xE004 3000 – 0xE004 3FFF	4KB	MTB
	0xE004 2000 – 0xE004 2FFF	4KB	CTI
	0xE004 1000 – 0xE004 1FFF	4KB	ETM
	0xE004 0000 – 0xE004 0FFF	4KB	TPIU
	0xE002 E000 – 0xE002 EFFF	4KB	SCS Non-sec alias
	0xE000 E000 – 0xE000 EFFF	4KB	SCS
	0xE000 2000 – 0xE000 2FFF	4KB	BPU
	0xE000 1000 – 0xE000 1FFF	4KB	DWT
	0xE000 0000 - 0xE000 0FFF	4KB	ITM
	0x6000 0000 - 0xDFFF FFFF		Reserved
AHB2:AHB	0x4800 2400 - 0x5FFF_FFFF		Reserved
	0x4800 2000 - 0x4800_23FF	1KB	FMC
	0x4800 1C00 - 0x4800 1FFF	1KB	CRC
	0x4800 1800 - 0x4800 1BFF	1KB	DMA1
	0x4800 1400 - 0x4800 17FF	1KB	DMA0
	0x4800 1000 - 0x4800 13FF	1KB	RCC
	0x4800 0C00 - 0x4800 0FFF	1KB	ADC
	0x4800 0800 - 0x4800 0BFF	1KB	HASH
	0x4800 0400 - 0x4800 07FF	1KB	AES
	0x4800 0000 - 0x4800 03FF	1KB	Reserved
AHB1:AHB	0x4002 1800 - 0x47FF_FFFF	112MB	Reserved
	0x4002 1400 - 0x4002 17FF	1KB	GPIOF
	0x4002 1000 - 0x4002 13FF	1KB	GPIOE
	0x4002 0C00 - 0x4002 0FFF	1KB	GPIOD
	0x4002 0800 - 0x4002 0BFF	1KB	GPIOC
	0x4002 0400 - 0x4002 07FF	1KB	GPIOB
	0x4002 0000 - 0x4002 03FF	1KB	GPIOA
AHB1:AHB2APB2	0x4001 D000 - 0x4001 FFFF	13KB	Reserved
	0x4001 CC00 - 0x4001 CFFF	1KB	EXTI
	0x4001 C800 - 0x4001 CBFF	1KB	Reserved
	0x4001 B800 - 0x4001 C7FF	4KB	Reserved
	0x4001 B400 - 0x4001 B7FF	1KB	TPSensor®
	0x4001 A400 - 0x4001 B3FF	4KB	Reserved
	0x4001 A000 - 0x4001 A3FF	1KB	OA1
	0x4001 9C00 - 0x4001 9FFF	1KB	OA0
	0x4001 9400 - 0x4001 9BFF	2KB	Reserved
	0x4001 9000 - 0x4001 93FF	1KB	CMP1

Bus	Boundary Address	Size (Bytes)	Destination Slave
	0x4001 8C00 - 0x4001 8FFF	1KB	CMP0
	0x4001 8400 - 0x4001 8BFF	2KB	Reserved
	0x4001 8000 - 0x4001 83FF	1KB	Reserved
	0x4001 7800 - 0x4001 7FFF	2KB	Reserved
	0x4001 7400 - 0x4001 77FF	1KB	SPI_I2S2
	0x4001 6400 - 0x4001 73FF		Reserved
	0x4001 6000 - 0x4001 63FF	1KB	TRNG
	0x4001 4000 - 0x4001 5FFF	8KB	CAN2.0B
	0x4001 3C00 - 0x4001 3FFF	1KB	ADVTMR2
	0x4001 3800 - 0x4001 3BFF	1KB	ADVTMR1
	0x4001 3400 - 0x4001 37FF	1KB	ADVTMR0
	0x4001 3000 - 0x4001 33FF	1KB	SYSCFG
	0x4001 1800 - 0x4001 2FFF	6KB	Reserved
	0x4001 1400 - 0x4001 17FF	1KB	VREFBUF
	0x4001 1000 - 0x4001 13FF	1KB	Reserved
	0x4001 0C00 - 0x4001 0FFF	1KB	UART3
	0x4001 0800 - 0x4001 0BFF	1KB	Reserved
	0x4001 0400 - 0x4001 07FF	1KB	UART1
	0x4001 0000 - 0x4001 03FF	1KB	UART0
AHB1:AHB2APB1	0x4000 9C00 - 0x4000_FFFF	25KB	Reserved
	0x4000 9800 - 0x4000_9BFF	1KB	SPI_I2S1
	0x4000 9400 - 0x4000_97FF	1KB	SPI_I2S0
	0x4000 8C00 - 0x4000_93FF	2KB	Reserved
	0x4000 8800 - 0x4000_8BFF	1KB	UART6
	0x4000 8400 - 0x4000_87FF	1KB	UART5
	0x4000 8300 - 0x4000_83FF	1KB	UART4
	0x4000 6800 - 0x4000_82FF	6KB	Reserved
	0x4000 6400 - 0x4000_67FF	1KB	DAC
	0x4000 6000 - 0x4000_63FF	1KB	WWDG
	0x4000 5C00 - 0x4000_5FFF	1KB	IWDG
	0x4000 5800 - 0x4000_5BFF	1KB	PMU
	0x4000 5400 - 0x4000_57FF	1KB	Reserved
	0x4000 5000 - 0x4000 53FF	1KB	I2C1
	0x4000 4C00 - 0x4000 4FFF	1KB	I2C0
	0x4000 4800 - 0x4000 4BFF	1KB	RTC
	0x4000 4400 - 0x4000 47FF	1KB	RTC_BKR
	0x4000 1800 - 0x4000 44FF	11KB	Reserved
	0x4000 1400 - 0x4000 17FF	1KB	GPTMR5
	0x4000 1000 - 0x4000 13FF	1KB	GPTMR4

Bus	Boundary Address	Size (Bytes)	Destination Slave
	0x4000 0C00 - 0x4000 0FFF	1KB	GPTMR3
	0x4000 0800 - 0x4000 0BFF	1KB	GPTMR2
	0x4000 0400 - 0x4000 07FF	1KB	GPTMR1
	0x4000 0000 - 0x4000 03FF	1KB	GPTMR0
	0x2005 4000 - 0x3FFF FFFF		Reserved
SRAM2	0x2005 0000 - 0x2005 3FFF	16KB	SRAM2
SRAM1	0x2003 0000 - 0x2004 FFFF	128KB	SRAM1
SRAM0	0x2000 0000 - 0x2002 FFFF	192KB	SRAM0
External Flash	0x1000 0000 - 0x1FFF FFFF	256MB	QSPI bank
	0x0FFF 0000 - 0x0FFF FFFF	64KB	NVR
	0x0FFE 9410 - 0x0FFE_FFFF		Reserved
	0x0FFE 9000 - 0x0FFE 940F	1KB+16B	OTP
	0x0FFE 8060 - 0x0FFE 8FFF		Reserved
	0x0FFE 8000 - 0x0FFE 805F	96B	Option bytes
	0x0FFE 0000 - 0x0FFE 7FFF	32KB	System memory
	0x0820 0000 - 0x0FEF FFFF		Reserved
	0x0800 0000 - 0x0807 FFFF	512KB	Main Flash memory
			Reserved
	0x0000 0000 - 0x0007 FFFF	512KB	Flash or system memory or SRAM

4.3 Interconnect Matrix

4.3.1 Interconnect Overview

Table 2. Interconnect Matrix(1)

Source/Destination	Destination/Source															
	GPTMR0	GPTMR1	GPTMR2	GPTMR3	GPTMR4	GPTMR5	ADVTMR0	ADVTRM1	ADVTMR2	RTC	OA0	OA1	ADC	DAC	CMP0	CMP1
GPTMR0	-	1	1	1	1	1	1	1	1	-	-	-	5	6	14	14
GPTMR1	1	-	1	1	1	1	1	1	1	-	-	-	5	6	14	14
GPTMR2	1	1	-	1	1	1	1	1	1	-	-	-	5	6	14	14
GPTMR3	1	1	1	-	1	1	1	1	1	-	-	-	5	6	14	14
GPTMR4	1	1	1	1	-	1	1	1	1	-	-	-	5	6	14	14
GPTMR5	1	1	1	1	1	-	1	1	1	-	-	-	5	6	-	-
ADVTMR0	1	1	1	1	1	1	-	1	1	-	-	-	5	6	14	14
ADVTMR0	1	1	1	1	1	1	1	-	1	-	-	-	5	6	14	14
ADVTMR0	1	1	1	1	1	1	1	1	-	-	-	-	5	6	14	14
RTC	2	2	2	2	2	2	2	2	2	-	-	-	15	-	-	-
OA0	-	-	-	-	-	-	-	-	-	-	-	-	3	-	-	-
OA1	-	-	-	-	-	-	-	-	-	-	-	-	3	-	-	-
ADC	4	-	-	-	-	-	4		-	-	-	-	-	-	-	-
DAC	-	-	-	-	-	-	-	-	-	-	7	7	-	-	11	11
CMP0	8	8	8	8	8	8	8	8	8	-	-	-	13	-	-	-
CMP1	8	8	8	8	8	8	8	8	8	-	-	-	13	-	-	-

EHS	-	-	-	-	-	-	-	-		-	-	-	-	-	-	-
ELS	9	9	9	9	9	9	9	9	9	-	-	-	-	-	-	-
IHS	9	9	9	9	9	9	9	9	9	-	-	-	-	-	-	-
ILS	9	9	9	9	9	9	9	9	-	-	-	-	-	-	-	-
MCO	9	9	9	9	9	9	9	9	9	-	-	-	-	-	-	-
Vref	-	-	-	-	-	-	-	-	-	-	-	-	10	-	12	12
Vavdd	-	-	-	-	-	-	-	-	-	-	-	-	10	-	-	-
VtemSen	-	-	-	-	-	-	-	-	-	-	-	-	10	-	-	-
EXTI	-	-	-	-	-	-	-	-	-	-	-	-	-	15	-	-
System error signal source	16	16	16	16	16	16	16	16	16	-	-	-	-	-	-	-

(1) The "-" symbol in cells means no available.

4.3.1.1 Timers → Timers

4.3.1.1.1 Timer External Trigger Inputs

Table 3. Interconnection to tmr_etrg_i[7:0] Input Multiplexer

Timer External Trigger Input Signals	Timer External Trigger Signals Assignment								
	GPTMR0	**GPTMR1**	**GPTMR2**	**GPTMR3**	**GPTMR4**	**GPTMR5**	**ADVTMR0**	**ADVTMR1**	**ADVTMR2**
TMRx_etrg[0]	GPTMR0_etrg	GPTMR1_etrg	GPTMR2_etrg	GPTMR3_etrg	GPTMR4_etrg	GPTMR5_etrg	ADVTMR0_etrg	ADVTMR1_etrg	ADVTMR2_etrg
TMRx_etrg[1]	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT
TMRx_etrg[2]	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT
TMRx_etrg[3]	ADC_AWD_OUT	GPTMR0_etrg	GPTMR0_etrg	GPTMR0_etrg	GPTMR1_etrg	GPTMR2_etrg	ADC_AWD_OUT		
TMRx_etrg[4]	ELS	GPTMR2_etrg	GPTMR1_etrg	GPTMR1_etrg	GPTMR2_etrg	GPTMR3_etrg	ELS		
TMRx_etrg[5]		GPTMR3_etrg	GPTMR3_etrg	GPTMR2_etrg	GPTMR3_etrg	GPTMR4_etrg			

TMRx_etrg[6]		GPTMR4_etrg	GPTMR4_etrg	GPTMR4_etrg	GPTMR5_etrg	ADVTMR0_etrg			
TMRx_etrg[7]	Reserved								

4.3.1.1.2 Timer Internal Trigger Inputs

Table 4. Interconnection to tmr_itrg_i[15:0] Input Multiplexer

Timer Internal Trigger Input Signals	Timer Internal Trigger Signals Assignment								
	GPTMR0	**GPTMR1**	**GPTMR2**	**GPTMR3**	**GPTMR4**	**GPTMR5**	**ADVTMR0**	**ADVTMR1**	**ADVTMR2**
TMRx_itrg[0]		GPTMR0_otrg	GPTMR0_otrg	GPTMR0_otrg	GPTMR0_otrg	GPTMR0_otrg	GPTMR0_otrg	GPTMR0_otrg	GPTMR0_otrg
TMRx_itrg[1]	GPTMR1_otrg		GPTMR1_otrg	GPTMR1_otrg	GPTMR1_otrg	GPTMR1_otrg	GPTMR1_otrg	GPTMR1_otrg	GPTMR1_otrg
TMRx_itrg[2]	GPTMR2_otrg	GPTMR2_otrg		GPTMR2_otrg	GPTMR2_otrg	GPTMR2_otrg	GPTMR2_otrg	GPTMR2_otrg	GPTMR2_otrg
TMRx_itrg[3]	GPTMR3_otrg	GPTMR3_otrg	GPTMR3_otrg		GPTMR3_otrg	GPTMR3_otrg	GPTMR3_otrg	GPTMR3_otrg	GPTMR3_otrg
TMRx_itrg[4]	GPTMR4_otrg	GPTMR4_otrg	GPTMR4_otrg	GPTMR4_otrg		GPTMR4_otrg	GPTMR4_otrg	GPTMR4_otrg	GPTMR4_otrg
TMRx_itrg[5]	GPTMR5_otrg	GPTMR5_otrg	GPTMR5_otrg	GPTMR5_otrg	GPTMR5_otrg		GPTMR5_otrg	GPTMR5_otrg	GPTMR5_otrg
TMRx_itrg[6]	ADVTMR0_otrg	ADVTMR0_otrg	ADVTMR0_otrg	ADVTMR0_otrg	ADVTMR0_otrg	ADVTMR0_otrg		ADVTMR0_otrg	ADVTMR0_otrg
TMRx_itrg[7]	ADVTMR1_otrg	ADVTMR1_otrg	ADVTMR1_otrg	ADVTMR1_otrg	ADVTMR1_otrg	ADVTMR1_otrg	ADVTMR1_otrg		ADVTMR1_otrg
TMRx_itrg[8]	ADVTMR2_otrg	ADVTMR2_otrg	ADVTMR2_otrg	ADVTMR2_otrg	ADVTMR2_otrg	ADVTMR2_otrg	ADVTMR2_otrg	ADVTMR2_otrg	
TMRx_itrg[9]	Reserved								
TMRx_itrg[10]									
TMRx_itrg[11]									
TMRx_itrg[12]									
TMRx_itrg[13]									
TMRx_itrg[14]									
TMRx_itrg[15]									

4.3.1.1.3 Timer OCREF Clear

Timer OCREF Clear Input Signal	Timer OCREF Clear Signal Assignment								
	GPTMR0	**GPTMR1**	**GPTMR2**	**GPTMR3**	**GPTMR4**	**GPTMR5**	**ADVTMR0**	**ADVTMR1**	**ADVTMR2**
TMRx_ocref_clear[0]	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT
TMRx_ocref_clear[1]	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT
TMRx_ocref_clear[2]									
TMRx_ocref_clear[3]									

4.3.1.1.4 Timer CH0 Inputs

Timer TI0 Input Signal	Timer TI0 Signal Assignment/Source								
	GPTMR0	**GPTMR1**	**GPTMR2**	**GPTMR3**	**GPTMR4**	**GPTMR5**	**ADVTMR0**	**ADVTMR1**	**ADVTMR2**
TMRx_CH0_in[0]	GPTMR0_CH0	GPTMR1_CH0	GPTMR2_CH0	GPTMR3_CH0	GPTMR4_CH0	GPTMR5_CH0	ADVTMR0_CH0	ADVTMR1_CH0	ADVTMR2_CH0
TMRx_CH0_in[1]	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT
TMRx_CH0_in[2]	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT
TMRx_CH0_in[3]	RTC_Wakeup						ELS		
TMRx_CH0_in[4]	ILS	RTC_Wakeup						ELS	
TMRx_CH0_in[5]	ELS	ILS	RTC_Wakeup						
TMRx_CH0_in[6]	IHS	ELS		RTC_Wakeup		MCO			
TMRx_CH0_in[7]		IHS			RTC_Wakeup				

4.3.1.1.5 Timer CH1 Inputs

Timer CH1 Input Signal	Timer TI1 Signal Assignment /Source

	GPTMR0	GPTMR1	GPTMR2	GPTMR3	GPTMR4	GPTMR5	ADVTMR0	ADVTMR1	ADVTMR2
TMRx_CH1_in[0]	GPTMR0_CH1	GPTMR1_CH1	GPTMR2_CH1	GPTMR3_CH1	GPTMR4_CH1	GPTMR5_CH1	ADVTMR0_CH1	ADVTMR1_CH1	ADVTMR2_CH1
TMRx_CH1_in[1]	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT			
TMRx_CH1_in[2]	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT			
TMRx_CH1_in[3]						13.56MHz			13.56MHz
TMRx_CH1_in[4]									
TMRx_CH1_in[5]									
TMRx_CH1_in[6]									
TMRx_CH1_in[7]									

4.3.1.1.6 Timer CH2 Inputs

Timer CH2 Input Signal	Timer TI2 Signal Assignment /Source								
	GPTMR0	GPTMR1	GPTMR2	GPTMR3	GPTMR4	GPTMR5	ADVTMR0	ADVTMR1	ADVTMR2
TMRx_CH2_in[0]	GPTMR0_CH2	GPTMR1_CH2	GPTMR2_CH2	GPTMR3_CH2	GPTMR4_CH2	GPTMR5_CH2	ADVTMR0_CH2	ADVTMR1_CH2	ADVTMR2_CH2
TMRx_CH2_in[1]	CMP0_OUT	CMP0_OUT	CMP0_OUT						
TMRx_CH2_in[2]	CMP1_OUT	CMP1_OUT	CMP1_OUT						
TMRx_CH2_in[3]						13.56MHz			13.56MHz
TMRx_CH2_in[4]									
TMRx_CH2_in[5]									
TMRx_CH2_in[6]									
TMRx_CH2_in[7]									

4.3.1.1.7 Timer CH3 Inputs

Timer CH3 Input Signal	Timer TI3 Signal Assignment /Source								
	GPTMR0	**GPTMR1**	**GPTMR2**	**GPTMR3**	**GPTMR4**	**GPTMR5**	**ADVTMR0**	**ADVTMR1**	**ADVTMR2**
TMRx_CH3_in[0]	GPTMR0_CH3	GPTMR1_CH3	GPTMR2_CH3	GPTMR3_CH3	GPTMR4_CH3	GPTMR5_CH3	ADVTMR0_CH3	ADVTMR1_CH3	ADVTMR2_CH3
TMRx_CH3_in[1]				CMP0_OUT	CMP0_OUT	CMP0_OUT			
TMRx_CH3_in[2]				CMP1_OUT	CMP1_OUT	CMP1_OUT			
TMRx_CH3_in[3]									
TMRx_CH3_in[4]									
TMRx_CH3_in[5]									
TMRx_CH3_in[6]									
TMRx_CH3_in[7]									

4.3.1.1.8 Timer Break 1 Inputs

Tmr_brk1 Input Signal	Timer Break1 Signal Assignment /Source								
	GPTMR0	**GPTMR1**	**GPTMR2**	**GPTMR3**	**GPTMR4**	**GPTMR5**	**ADVTMR0**	**ADVTMR1**	**ADVTMR2**
TMRx_brk_i[0]	GPTMR0_BRK_IN pin	GPTMR1_BRK_IN pin	GPTMR2_BRK_IN pin	GPTMR3_BRK_IN pin	GPTMR4_BRK_IN pin	GPTMR5_BRK_IN pin	ADVTMR0_BRK_IN pin	ADVTMR1_BRK_IN pin	ADVTMR2_BRK_IN pin
TMRx_brk_i[1]	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT	CMP0_OUT
TMRx_brk_i[2]	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT	CMP1_OUT
TMRx_brk_i[3]									

4.3.1.1.9 Timer Break 2 Inputs

Tmr_brk2 Input Signal	Timer Break2 Signal Assignment /Source								
	GPTMR0	GPTMR1	GPTMR2	GPTMR3	GPTMR4	GPTMR5	ADVTMR0	ADVTMR1	ADVTMR2
TMRx_brk2_i[0]							ADVTMR0_BRKIN2_IN pin	ADVTMR1_BRKIN2_IN pin	ADVTMR2_BRKIN2_IN pin
TMRx_brk2_i[1]							CMP0_OUT	CMP0_OUT	CMP0_OUT
TMRx_brk2_i[2]							CMP1_OUT	CMP1_OUT	CMP1_OUT
TMRx_brk2_i[3]									

4.3.1.1.10 Timer System Break Inputs

System Error Signal Source (tmr_sys_brk)	System Break Interconnect								
	GPTMR0	GPTMR1	GPTMR2	GPTMR3	GPTMR4	GPTMR5	ADVTMR0	ADVTMR1	ADVTMR2
Cortex-STAR core Lockup (Hard-fault) output (TMRx_sys_brk0)	GPTMR0_BRK	GPTMR1_BRK	GPTMR2_BRK	GPTMR3_BRK	GPTMR4_BRK	GPTMR5_BRK	ADVTMR0_BRK	ADVTMR1_BRK	ADVTMR2_BRK
SVS output (TMRx_sys_brk2)									
Clock security system (CSS) (TMRx_sys_brk3)									

4.3.2 ADC Trigger Inputs

ADC Trigger Input Channel Selection	ADC Trigger Input Assignment
adc_ext_trg [0]	RTC_Wakeup event detection
adc_ext_trg [1]	CMP0_out
adc_ext_trg [2]	CMP1_out

ADC Trigger Input Channel Selection	ADC Trigger Input Assignment
adc_ext_trg [3]	GPTMR0_otrg
adc_ext_trg [4]	GPTMR0_Capture/Compare Interrupt
adc_ext_trg [5]	GPTMR1_otrg
adc_ext_trg [6]	GPTMR1_Capture/Compare Interrupt
adc_ext_trg [7]	GPTMR2_otrg
adc_ext_trg [8]	GPTMR2_Capture/Compare Interrupt
adc_ext_trg [9]	GPTMR3_otrg
adc_ext_trg [10]	GPTMR3_Capture/Compare Interrupt
adc_ext_trg [11]	GPTMR4_otrg
adc_ext_trg [12]	GPTMR4_Capture/Compare Interrupt
adc_ext_trg [13]	GPTMR5_otrg
adc_ext_trg [14]	GPTMR5_Capture/Compare Interrupt
adc_ext_trg [15]	EXTI15 (EXTI Line15 interrupt pin)
adc_ext_trg [16]	EXTI2 (EXTI Line 2 interrupt pin)
adc_ext_trg [17]	ADVTMR0_otrg
adc_ext_trg [18]	ADVTMR0_otrg2
adc_ext_trg [19]	ADVTMR0_Capture/Compare Interrupt
adc_ext_trg [20]	ADVTMR1_otrg
adc_ext_trg [21]	ADVTMR1_otrg2
adc_ext_trg [22]	ADVTMR1_Capture/Compare Interrupt
adc_ext_trg [23]	ADVTMR2_otrg
adc_ext_trg [24]	ADVTMR2_otrg2
adc_ext_trg [25]	ADVTMR2_Capture/Compare Interrupt
adc_ext_trg [26]	Reserved

ADC Trigger Input Channel Selection	ADC Trigger Input Assignment
adc_ext_trg [27]	
adc_ext_trg [28]	
adc_ext_trg [29]	
adc_ext_trg [30]	
adc_ext_trg [31]	

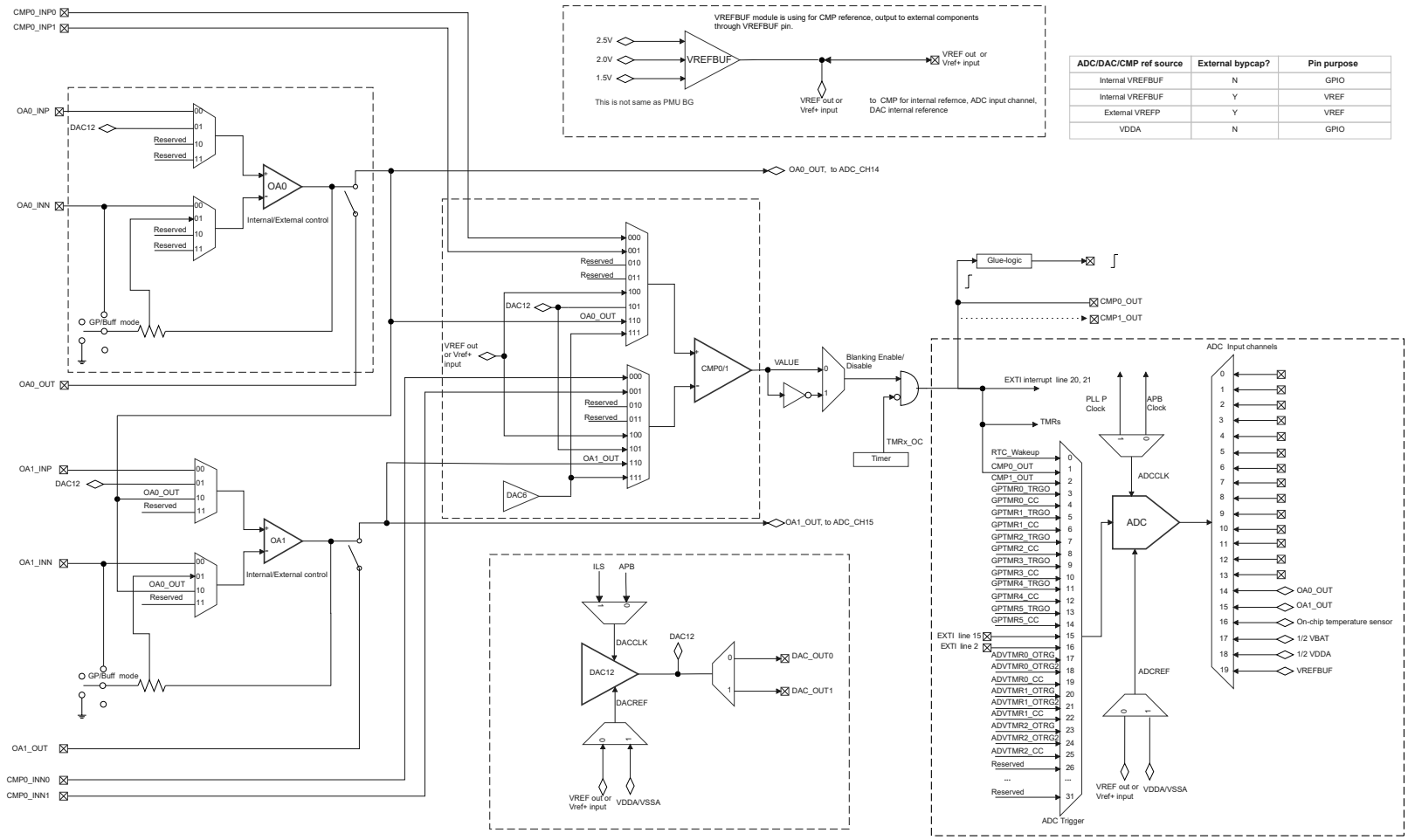
4.3.3 DAC Trigger Inputs

DAC Trigger Input Channel Selection	DAC Trigger Input Assignment
dac_trg_input 0	GPTMR0_otrg
dac_trg_input 1	GPTMR1_otrg
dac_trg_input 2	GPTMR2_otrg
dac_trg_input 3	GPTMR3_otrg
dac_trg_input 4	GPTMR4_otrg
dac_trg_input 5	GPTMR5_otrg
dac_trg_input 6	ADVTMR0_otrg
dac_trg_input 7	ADVTMR1_otrg
dac_trg_input 8	ADVTMR2_otrg
dac_trg_input 9	EXTI4 (EXTI Line 4 interrupt pin)
dac_trg_input 10-18	Reserved

4.3.4 CMP Blanking Inputs

CMP Blanking Signal Selection BLANKSEL[2:0]	CMP Input Assignment	
	CMP0 Input Channel	CMP1 Input Channel
000	ADVTMR0_CH3_OC	ADVTMR0_CH3_OC
001	ADVTMR1_CH3_OC	ADVTMR1_CH3_OC
010	ADVTMR2_CH3_OC	ADVTMR2_CH3_OC
011	GPTMR0_CH0_OC	GPTMR0_CH0_OC
100	GPTMR1_CH0_OC	GPTMR1_CH0_OC
101	GPTMR2_CH0_OC	GPTMR2_CH0_OC
110	GPTMR3_CH2_OC	GPTMR3_CH2_OC
111	GPTMR4_CH2_OC	GPTMR4_CH2_OC

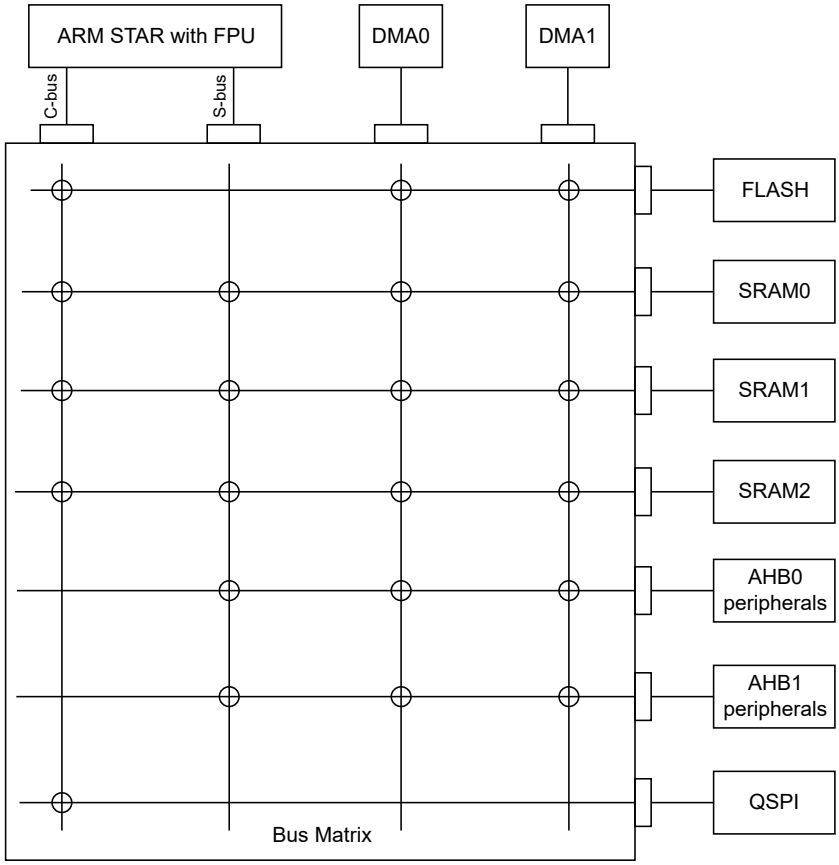
4.3.5 Analog Interconnection



ADC/DAC/CMP ref source	External bypcap?	Pin purpose
Internal VREFBUF	N	GPIO
Internal VREFBUF	Y	VREF
External VREFP	Y	VREF
VDDA	N	GPIO

4.4 Multi-AHB Bus Matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs) and the slaves (Flash memory, RAM, QUADSPI, AHB and APB peripherals). It also ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.



4.5 Power Management Unit (PMU)

The Power Management Unit (PMU) includes the following features:

- Regulators for core
- Supplier Voltage Supervisors (SVS)
- Brown-out Reset circuit (BOR), power-on and power-off
- Different power modes for saving power on the applications

4.5.1 Power Supply Schemes

The TSP325M5A device requires a V_{DD} operating voltage supply ranging from 1.71 V to 3.6 V. Several independent supplies can be provided for specific peripherals.

- V_{DD} = 1.71 V to 3.6 V
  V_{DD} serves as the external power supply for the I/Os, the internal regulators, and the system analog such as reset, power management and internal clocks. This is supplied externally via the VDD pins.
- V_{DDA} = 1.71 V to 3.6 V
  V_{DDA} acts as the external analog power supply for ADC, DAC, VREFBUF, OA, and CMP. If V_{DDA} is not in use, it should be connected to $V_{DD.}$
- V_{REF-}, V_{REF+}
  V_{REF+} is the input reference voltage for ADCs and DACs. It is also the output of VREFBUF when enabled.

When V_{DDA} < 2 V, V_{REF+} must be equal to V_{DDA}.
When V_{DDA} ≥ 2 V, V_{REF+} must be between 2 V and V_{DDA}.
The internal voltage reference buffer supports three output voltages, configured with VRS bits in the VREFBUF_CSR register:

- V_{REF+} = 1.5 V
- V_{REF+} = 2.0 V
- V_{REF+} = 2.5 V

V_{REF-} is double bonded with V_{SSA}.

4.5.2 Voltage Regulators

Two linear voltage regulators are integrated: one primary regulator for the CORE and another for the RTC domain. The primary regulator supports both boost and normal modes. In boost mode, the CPU runs up to 156 MHz, while in normal mode, it runs up to 48 MHz.

4.5.3 Supply Voltage Supervisor (SVS)

The Supply Voltage Supervisor (SVS) monitors the power supply V_{DD} by comparing it to a selected threshold. The SVS is enabled by setting the SVSEN bit.

An SVSO flag signals whether V_{DD} is above or below the SVS threshold. This event is internally connected to the EXTI line 16 and can generate an interrupt if enabled through the EXTI registers. The SVS output interrupt can be generated when V_{DD} drops below the SVS threshold and/or when V_{DD} rises above the SVS threshold, depending on EXTI line 16 rising/falling edge configuration.

4.5.4 Power Modes

The TSP325M5A device is in run mode by default after system or power reset. The user has the option to choose from several low-power modes, detailed as follows:

- Sleep mode
  In this mode, only the CPU is halted while all other peripherals s continue to operate. These peripherals can wake up the CPU when an interrupt or event occurs.
- Stop mode
  This mode allows the device to achieve minimal power consumption while retaining the SRAM and register contents. All clocks within the VCORE domain are halted.
- Standby mode
  This mode is used to achieve the minimum power consumption with Brown-out Reset (BOR). The internal regulator is switched off to power down the VCORE domain. Several modules remain active, including Retention SRAM, IWDG, ILS or ELS clock, and RTC.
- Shutdown mode
  This mode aims for the lowest power consumption. The internal regulator is switched off, powering down the VCORE domain, with only a few modules such as the ILS or ELS clock and RTC remaining active.
- Battery replacement mode
  This mode allows the system to quickly replace the battery on the main power supply while the VBAT pin is connected to an external capacitor or battery cell. It is only supported for tens of seconds, relying on the external capacitor. Only ILS or ELS clock and RTC are active in this mode.

Mode		Run		Sleep		Stop	Standby		Shutdown	Battery Replacement
		High Power	Ultra-Low-Power	High Power	Ultra-Low-Power		Standby1	Standby2		
Maximum System Frequency		156 MHz	48 MHz	156 MHz	48 MHz	32 kHz	32 kHz	32 kHz	32 kHz	32 kHz
Wakeup Source		N/A		Any interrupts/ events	Any interrupts/ events	EXTI	RTC, IWDG, BOR, SVS TPSensor® (Optional) wakeup cell, NRST	RTC, IWDG, BOR, SVS, wakeup cell, NRST	RTC, wakeup cell, NRST	NA
PMU	VBUF_FLASH	On	On	On	On	Off	Off	Off	Off	Off
	POR	On	On	On	On	On	On	On	On	Off
	SVS	On	On	On	On	On	On	Optional	Off	Off
	LDO_CORE	HP + dynamic enable	LP	HP + dynamic enable	LP	On	Off	Off	Off	Off
	SWITCH_D0	On	On	On	On	On	On	On	On	On

Mode		Run		Sleep		Stop	Standby		Shutdown	Battery Replacement
		High Power	Ultra-Low-Power	High Power	Ultra-Low-Power		Standby1	Standby2		
	VREF_RTC/ POR_RTC	On	On	On	On	On	On	On	On	On
	LDO_RTC	On	On	On	On	On	On	On	On	On
	Power Function	On	On	On	On	On	On	On	On	On
	SWITCH_TSR	On	On	On	On	On	On	On	On	Off
Core	CPU	On	On	Gated	Gated	Gated	Off	Off	Off	Off
	ETM	On	On	Gated	Gated	Gated	Off	Off	Off	Off
	SWD/JTAG	On	On	Gated	Gated	Gated	Off	Off	Off	Off
	EXTI	On	On	On	On	On	Off	Off	Off	Off
	RCC	On	On	On	On	Gated	Off	Off	Off	On
	DMA	Optional	Optional	Optional	Optional	Gated	Off	Off	Off	Off
	Flash	On	On	Gated	Gated	Off	Off	Off	Off	Off
	SRAM0 (192 KB)	On	On	On	On	Optional	Off	Off	Off	Off
	SRAM1 (128 KB)	On	On	On	On	Optional	Off	Off	Off	Off
	SRAM2 (retention,16 KB)	On	On	On	On	On	On	Off	Off	Off
Clock	ILS	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional
	ELS	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional
	IHS	Optional	Optional	Optional	Optional	Off	Off	Off	Off	Off
	EHS	Optional	Optional	Optional	Optional	Off	Off	Off	Off	Off
	PLL	Optional	Optional	Optional	Optional	Off	Off	Off	Off	Off
Peripherals	ADC	Optional	Optional	Optional	Optional	Off	Off	Off	Off	Off
	OA0,1	Optional	Optional	Optional	Optional	Off	Off	Off	Off	Off
	CMP0,1	Optional	Optional	Optional	Optional	Optional	Off	Off	Off	Off
	DAC	Optional	Optional	Optional	Optional	Off	Off	Off	Off	Off
	CAN2.0B	Optional	Optional	Gated	Gated	Off	Off	Off	off	Off
	TPSENSOR	Optional	Optional	Optional	Optional	Optional	Optional	Off	Off	Off

Mode		Run		Sleep		Stop	Standby		Shutdown	Battery Replacement
		High Power	Ultra-Low-Power	High Power	Ultra-Low-Power		Standby1	Standby2		
	UART0,1,3,4,5,6	Optional	Optional	Optional	Optional	Off	Off	Off	Off	Off
	I2C0,1	Optional	Optional	Optional	Optional	Off	Off	Off	Off	Off
	SPI_I2S0,1,2	Optional	Optional	Optional	Optional	Off	Off	Off	Off	Off
	GPTMR0,1,2,3,4,5	Optional	Optional	Optional	Optional	Off	Off	off	Off	Off
	ADVTMR0,1,2	Optional	Optional	Optional	Optional	Off	Off	Off	Off	Off
	IWDG	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Off	Off
	WWDG	Optional	Optional	Gated	Gated	Off	Off	off	off	off
IO	32K crystal IO	Active	Active	Active	Active	Active	Active	Active	Active	Active
	IO with wake-up cell (5 pins)	Off	Off	Off	Off	Off	Optional	Optional	Optional	Off
	Other IO	Active	Active	State held	State held	State held	High impedance or analog path	High impedance or analog path	High impedance or analog path	Off

4.6 Reset and Clock System

The devices incorporate a reset and clock system.

4.6.1 Reset

There are three types of reset function:

- Power Reset
- System Reset
- RTC Domain Reset

4.6.1.1 Power Reset

The activation of a power reset occurs under the following conditions:

- During a Power-on Reset (POR) or Brown-out Reset (BOR).
  A Power-on Reset BOR, including Power-on or Power-down Reset (POR/PDR), sets all registers to their reset values, with the exception of the RTC domain.
- When exiting standby mode.
  In this scenario, all registers in the VCORE domain are set to their reset value. Registers outside the VCORE domain (RTC, WKUP, IWDG, and standby/shutdown modes control) are not impacted.
- When exiting shutdown mode.
  In this situation, a BOR is generated, resetting all registers with the exception of those in the RTC domain.

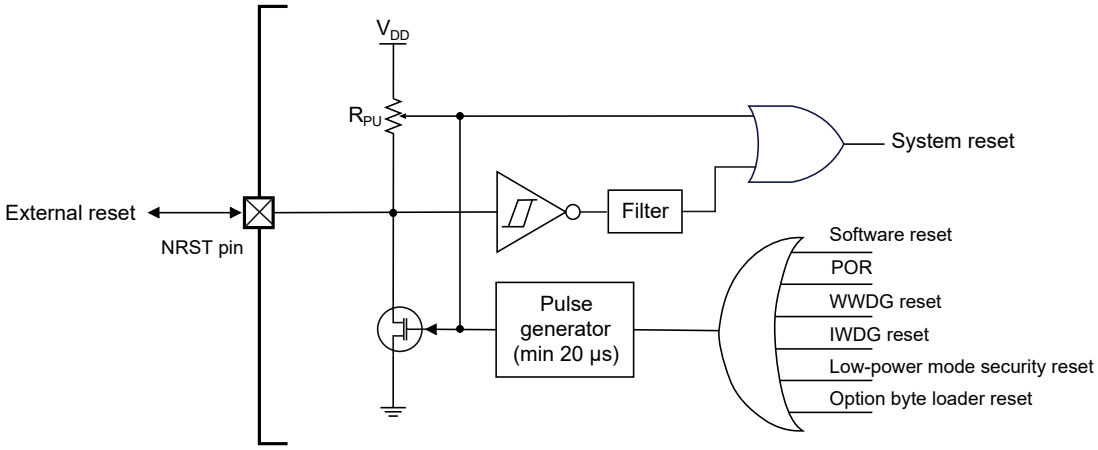
4.6.1.2 System Reset

A system reset sets all registers to their reset values except the reset flags in the clock control/status register (RCC_CSR) and the registers in the RTC domain.

A system reset is generated when one of the following events occurs:

- A low level on the NRST pin (external reset)
- Window Watchdog event (WWDG reset)
- Independent Watchdog event (IWDG reset)
- A software reset (SW reset)
- Low-power mode security reset
- Option byte loader reset
- A Brown-out Reset (BOR)

The reset source can be identified by checking the reset flags in the control/status register.



NRST pin (external reset)

In this mode, any valid reset signal on the NRST pin is propagated to the device's internal logic. However, resets generated internally by the device are not visible on the pin.

4.6.1.3 RTC Domain Reset

The RTC domain has two specific resets. An RTC domain reset is generated when one of the following events occurs:

- Software reset, triggered by setting the BDRST bit
- V_{DD} or V_{BAT} power on if both supplies have previously been powered off.

> Note
>
> An RTC domain reset only affects the following components: the ELS oscillator, the RTC, the Backup registers and the RCC RTC domain control register.

4.6.2 Clock System

4.6.2.1 Clock Distributor

The clock features include the following clock sources.

- **Clock sources**
  - 4 - 32 MHz External High-Speed (EHS) oscillator with external crystal or ceramic resonator. It can supply clock to system PLL. The EHS can also be configured in bypass mode for an external clock.
  - 32.768 kHz External Low-Speed (ELS) crystal which optionally drivesthe real time clock.
  - 8 MHz Internal High-Speed (IHS) RC oscillator, trimmable by software with ±0.5% accuracy. It can supply clock to system PLL.
  - 32 kHz Internal Low-Speed (ILS) RC oscillator with 2% accuracy.
  - System PLL with a maximum output frequency of 156 MHz. It can be fed with EHS or IHS clock.
  - 10 MHz internal oscillator dedicated using for TPSensor® module with frequency hopping support.
- **Clock divider**: Rich clock dividers to get the best trade-off between speed and current consumption.
- **Safe clock switching**: Clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management**: To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Clock out**:

- MCO: MCU clock output included IHS, EHS, PLLCLK, and SYSCLK.
- LCO: Low frequency clock output included ILS and ELS.

4.6.2.2 Clock Safety System

The system clock is automatically switched to IHS in the event of EHS clock failure. And a software interrupt is generated if enabled.

The ELS clock failure can be detected and generate an interrupt. It is aslo automatically switched to IHS or ILS depended on the software selection. If IHS is selected, the proper divider is enabled as well.

4.7 Interrupts and Events

4.7.1 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) hardware block provides flexible interrupt management features with minimal interrupt latency, including 115 Maskable interrupt channels and 4-bit for 16 programmable priority levels.

4.7.2 Extended Interrupts and Events Controller (EXTI)

EXTI Line	Line Source	Line Type
0	GPIO0	Configurable
1	GPIO1	Configurable
2	GPIO2	Configurable
3	GPIO3	Configurable
4	GPIO4	Configurable
5	GPIO5	Configurable
6	GPIO6	Configurable
7	GPIO7	Configurable
8	GPIO8	Configurable
9	GPIO9	Configurable
10	GPIO10	Configurable
11	GPIO11	Configurable
12	GPIO12	Configurable
13	GPIO13	Configurable
14	GPIO14	Configurable
15	GPIO15	Configurable
16	SVS	Configurable
17	RTC alarm event	Configurable
18	Timestamp or CSS_ELS	Configurable
19	RTC wakeup timer	Configurable
20	CMP0 output	Configurable
21	CMP1 output	Configurable
31	TPSensor	Configurable

4.7.3 Interrupt Vector Table

NMI/MI	Position	Priority	Type of priority	Acronym	Description	Address
NMI	-	-	-	-	Reserved	0x0000 0000
NMI	-	-3	Fixed	Reset	Reset	0x0000 0004
NMI	-	-2	Fixed	NMI	Non maskable interrupt. SRAM parity err + EHS CSS	0x0000 0008
NMI	-	-1	Fixed	HardFault	All classes of fault	0x0000 000C
NMI	-	0	Settable	MemManage	Memory management	0x0000 0010
NMI	-	Configurable	Settable	BusFault	Pre-fetch fault, memory access fault	0x0000 0014
NMI	-	Configurable	Settable	UsageFault	Undefined instruction or illegal state	0x0000 0018
...	...	...	...	...	...	
...	...	...	...	...	...	
NMI	-	Configurable	-	-	Reserved	0x0000 001C
NMI		Configurable			Reserved	0x0000 0028
NMI	-	Configurable	-	-	System service call via SWI instruction	0x0000 002C
NMI	-	Configurable	-	-	Monitor	0x0000 0030
NMI	-	Configurable	-	-	Reserved	0x0000 0034
NMI	-	Configurable	Settable	PendSV	Pendable request for system service	0x0000 0038
NMI	-	Configurable	Settable	SysTick	System tick timer	0x0000 003C
MI	0	Configurable	Settable	WWDG	Window Watchdog interrupt	0x0000 0040
MI	1	Configurable	Settable	SVS	SVS through EXTI line 16	0x0000 0044
MI	2	Configurable	Settable	RTC/ CSS_ELS	RTC/CSS on ELS through EXTI line 18	0x0000 0048
MI	3	Configurable	Settable	RTC_WKUP	RTC Wakeup timer through EXTI line 19	0x0000 004C
MI	4	Configurable	Settable	FMC	FMC global interrupt	0x0000 0050
MI	5	Configurable	Settable	RCC	RCC global interrupt	0x0000 0054
MI	6	Configurable	Settable	EXTI0	EXTI Line 0 interrupt	0x0000 0058
MI	7	Configurable	Settable	EXTI1	EXTI Line 1 interrupt	0x0000 005C
MI	8	Configurable	Settable	EXTI2	EXTI Line 2 interrupt	0x0000 0060
MI	9	Configurable	Settable	EXTI3	EXTI Line 3 interrupt	0x0000 0064
MI	10	Configurable	Settable	EXTI4	EXTI Line 4 interrupt	0x0000 0068
MI	11	Configurable	Settable	Reserved	Reserved	0x0000 006C
MI	12	Configurable	Settable	DMA0_CH0	DMA0 channel 0 interrupt	0x0000 0070
MI	13	Configurable	Settable	DMA0_CH1	DMA0 channel 1 interrupt	0x0000 0074
MI	14	Configurable	Settable	DMA0_CH2	DMA0 channel 2 interrupt	0x0000 0078
MI	15	Configurable	Settable	DMA0_CH3	DMA0 channel 3 interrupt	0x0000 007C

NMI/MI	Position	Priority	Type of priority	Acronym	Description	Address
MI	16	Configurable	Settable	DMA0_CH4	DMA0 channel 4 interrupt	0x0000 0080
MI	17	Configurable	Settable	DMA0_CH5	DMA0 channel 5 interrupt	0x0000 0084
MI	18	Configurable	Settable	DMA0_CH6	DMA0 channel 6 interrupt	0x0000 0088
MI	19	Configurable	Settable	DMA0_CH7	DMA0 channel 7 interrupt	0x0000 008C
MI	20	Configurable	Settable	ADC	ADC global interrupt	0x0000 0090
MI	21	Configurable	Settable	Reserved	Reserved	0x0000 0094
MI	22	Configurable	Settable	Reserved	Reserved	0x0000 0098
MI	23	Configurable	Settable	CAN2.0B_INTR1	CAN2.0B interrupt	0x0000 009C
MI	24	Configurable	Settable	Reserved	Reserved	0x0000 00A0
MI	25	Configurable	Settable	Reserved	Reserved	0x0000 00A4
MI	26	Configurable	Settable	Reserved	Reserved	0x0000 00A8
MI	27	Configurable	Settable	EXTI9-5	EXTI Line[9:5] interrupts	0x0000 00AC
MI	28	Configurable	Settable	ADVTMR0_BRK	ADVTMR0 Break	0x0000 00B0
MI	29	Configurable	Settable	ADVTMR0_UP	ADVTMR0 Update	0x0000 00B4
MI	30	Configurable	Settable	ADVTMR0_TRG_COM/ ADVTMR0_DIR/ ADVTMR0_IDX	ADVTMR0 trigger and commutation/ADVTMR0 Direction Change interrupt/ ADVTMR0 Index	0x0000 00B8
MI	31	Configurable	Settable	ADVTMR0_CC	ADVTMR0 capture compare interrupt	0x0000 00BC
MI	32	Configurable	Settable	GPTMR0_BRK	GPTMR0 Break	0x0000 00C0
MI	33	Configurable	Settable	GPTMR0_UP	GPTMR0 Update	0x0000 00C4
MI	34	Configurable	Settable	GPTMR0_TRG_COM/ GPTMR0_DIR/ GPTMR0_IDX	GPTMR0 trigger and commutation/GPTMR0 Direction Change interrupt/ GPTMR0 Index	0x0000 00C8
MI	35	Configurable	Settable	GPTMR0_CC	GPTMR0 capture compare interrupt	0x0000 00CC
MI	36	Configurable	Settable	GPTMR1_BRK	GPTMR1 Break	0x0000 00D0
MI	37	Configurable	Settable	GPTMR1_UP	GPTMR1 Update	0x0000 00D4
MI	38	Configurable	Settable	GPTMR1_TRG_COM/ GPTMR1_DIR/ GPTMR1_IDX	GPTMR1 trigger and commutation/GPTMR1 Direction Change interrupt/ GPTMR1 Index	0x0000 00D8
MI	39	Configurable	Settable	GPTMR1_CC	GPTMR1 capture compare interrupt	0x0000 00DC
MI	40	Configurable	Settable	GPTMR2_BRK	GPTMR2 Break	0x0000 00E0
MI	41	Configurable	Settable	GPTMR2_UP	GPTMR2 Update	0x0000 00E4

NMI/MI	Position	Priority	Type of priority	Acronym	Description	Address
MI	42	Configurable	Settable	GPTMR2_TRG_COM/ GPTMR2_DIR/ GPTMR2_IDX	GPTMR2 trigger and commutation/GPTMR2 Direction Change interrupt/ GPTMR2 Index	0x0000 00E8
MI	43	Configurable	Settable	GPTMR2_CC	GPTMR2 capture compare interrupt	0x0000 00EC
MI	44	Configurable	Settable	GPTMR3_BRK	GPTMR3 Break	0x0000 00F0
MI	45	Configurable	Settable	GPTMR3_UP	GPTMR3 Update	0x0000 00F4
MI	46	Configurable	Settable	GPTMR3_TRG_COM/ GPTMR3_DIR/ GPTMR3_IDX	GPTMR3 trigger and commutation/GPTMR3 Direction Change interrupt/ GPTMR3 Index	0x0000 00F8
MI	47	Configurable	Settable	GPTMR3_CC	GPTMR3 capture compare interrupt	0x0000 00FC
MI	48	Configurable	Settable	GPTMR4_BRK	GPTMR4_ Break	0x0000 0100
MI	49	Configurable	Settable	GPTMR4_UP	GPTMR4 Update global interrupts	0x0000 0104
MI	50	Configurable	Settable	GPTMR4_TRG_COM/ GPTMR4__DIR /GPTMR4_IDX	GPTMR4 trigger and communication/ GPTMR4_Direction Change interrupt/GPTMR4_ Index	0x0000 0108
MI	51	Configurable	Settable	GPTMR4_CC	GPTMR4_DACUNDER capture compare interrupt	0x0000 010C
MI	52	Configurable	Settable	GPTMR5_BRK	GPTMR5_Break	0x0000 0110
MI	53	Configurable	Settable	GPTMR5_UP	GPTMR5_ Update global interrupts	0x0000 0114
MI	54	Configurable	Settable	GPTMR5_TRG_COM/ GPTMR5_DIR/ GPTMR5_IDX	GPTMR5 trigger and commutation/ GPTMR5_Direction Change interrupt/GPTMR5_Index	0x0000 0118
MI	55	Configurable	Settable	GPTMR5_CC	GPTMR5 capture compare interrupt	0x0000 011C
MI	56	Configurable	Settable	Reserved	Reserved	0x0000 0120
MI	57	Configurable	Settable	Reserved	Reserved	0x0000 0124
MI	58	Configurable	Settable	Reserved	Reserved	0x0000 0128
MI	60	Configurable	Settable	I2C0_ER	I2C0 error interrupt	0x0000 0130
MI	62	Configurable	Settable	I2C1_ER	I2C1 error interrupt	0x0000 0138
MI	63	Configurable	Settable	Reserved	Reserved	0x0000 013C
MI	64	Configurable	Settable	Reserved	Reserved	0x0000 0140
MI	65	Configurable	Settable	SPI/I2S0	SPI/I2S0 global interrupt	0x0000 0144
MI	66	Configurable	Settable	SPI/I2S1	SPI/I2S1 global interrupt	0x0000 0148
MI	67	Configurable	Settable	SPI/I2S2	SPI/I2S2 global interrupt	0x0000 014C

NMI/MI	Position	Priority	Type of priority	Acronym	Description	Address
MI	68	Configurable	Settable	Reserved	Reserved	0x0000 0150
MI	69	Configurable	Settable	Reserved	Reserved	0x0000 0154
MI	77	Configurable	Settable	EXTI15_10	EXTI Line[15:10] interrupts	0x0000 0174
MI	78	Configurable	Settable	RTC_ALARM	RTC alarms interrupts	0x0000 0178
MI	79	Configurable	Settable	ADVTMR1_BRK	ADVTMR1 Break	0x0000 017C
MI	80	Configurable	Settable	ADVTMR1_UP	ADVTMR1 Update	0x0000 0180
MI	81	Configurable	Settable	ADVTMR1_TRG_COM/ ADVTMR1_DIR/ GPTMR1_IDX	ADVTMR1 trigger and commutation/Direction Change interrupt/Index	0x0000 0184
MI	82	Configurable	Settable	ADVTMR1_CC	ADVTMR1 capture compare interrupt	0x0000_0188
MI	83	Configurable	Settable	Reserved	Reserved	0x0000_018C
MI	84	Configurable	Settable	Reserved	Reserved	0x0000_0190
MI	85	Configurable	Settable	Reserved	Reserved	0x0000_0194
MI	86	Configurable	Settable	DMA1_CH0	DMA1 channel 0 interrupt	0x0000_0198
MI	87	Configurable	Settable	DMA1_CH1	DMA1 channel 1 interrupt	0x0000_019C
MI	88	Configurable	Settable	DMA1_CH2	DMA1 channel 2 interrupt	0x0000_01A0
MI	89	Configurable	Settable	DMA1_CH3	DMA1 channel 3 interrupt	0x0000_01A4
MI	90	Configurable	Settable	DMA1_CH4	DMA1 channel 4 interrupt	0x0000_01A8
MI	91	Configurable	Settable	DMA1_CH5	DMA1 channel 5 interrupt	0x0000_01AC
MI	92	Configurable	Settable	DMA1_CH6	DMA1 channel 6 interrupt	0x0000_01B0
MI	93	Configurable	Settable	DMA1_CH7	DMA1 channel 7 interrupt	0x0000_01B4
MI	94	Configurable	Settable	Reserved	Reserved	0x0000_01B8
MI	95	Configurable	Settable	CMP0	CMP0 through EXTI lines 20	0x0000_01BC
MI	96	Configurable	Settable	CMP1	CMP1 through EXTI lines 21	0x0000_01C0
MI	97	Configurable	Settable	Reserved	Reserved	0x0000_01C4
MI	98	Configurable	Settable	Reserved	Reserved	0x0000_01C8
MI	99	Configurable	Settable	ADVTMR2_BRK	ADVTMR2 Break	0x0000_01CC
MI	100	Configurable	Settable	ADVTMR2_UP	ADVTMR2 Update	0x0000_01D0
MI	101	Configurable	Settable	ADVTMR2_TRG_COM/ ADVTMR2_DIR/ ADVTMR2_IDX	ADVTMR2 trigger and commutation/Direction Change interrupt/Index	0x0000_01D4
MI	102	Configurable	Settable	ADVTMR2_CC	ADVTMR2 capture compare interrupt	0x0000_01D8
MI	103	Configurable	Settable	Reserved	Reserved	0x0000_01DC

NMI/MI	Position	Priority	Type of priority	Acronym	Description	Address
MI	104	Configurable	Settable	FPU	Floating point interrupt	0x0000_01E0
MI	105	Configurable	Settable	Reserved	Reserved	0x0000_01E4
MI	106	Configurable	Settable	Reserved	Reserved	0x0000_01E8
MI	107	Configurable	Settable	AES	AES global interrupt	0x0000_01EC
MI	108	Configurable	Settable	TRNG	TRNG global interrupt	0x0000_01F0
MI	109	Configurable	Settable	Reserved	Reserved	0x0000_01F4
MI	110	Configurable	Settable	HASH	HASH global interrupt	0x0000_01F8
MI	111	Configurable	Settable	Reserved	Reserved	0x0000_01FC
MI	112	Configurable	Settable	Reserved	Reserved	0x0000_0200
MI	113	Configurable	Settable	Reserved	Reserved	0x0000_0204
MI	114	Configurable	Settable	TPSensor®	TPSensor® global interrupt	0x0000_0208
MI	115	Configurable	Settable	DAC	DAC global interrupt	0x0000_020C

4.8 Boot Modes

At startup, a BOOT0 pin (or nBOOT0 option bit) and a nBOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The bootloader is located in the system memory. It is used to reprogram the Flash memory by using UART and I2C through the Device Firmware Upgrade (DFU).

Boot_lock	nBoot1 Bit	nBoot0 Bit	Boot Pin	nSWBOOT0	Boot Memory Space Alias
1	x	x	x	x	Main Flash memory
0	x	x	0	1	Main Flash memory is selected as boot area
0	0	0	x	0	SRAM0 is selected as boot area
0	1	0	x	0	System memory is selected as boot area

4.9 Debug

The Arm SWJ-DP interface is embedded and acts as a combined JTAG and serial wire debug port. It facilitates connecting a Serial Wire Debug (SWD) or a JTAG probe to the target.

4.10 Device ID

The device ID is used to identify device configurations, including memory, peripherals, and so on.

Part Numbers	Device ID
TPS325M5A57Q-QP5T	800000F2

4.11 Chip ID

The device supports a 96-bit unique ID; refer to Table 1 for details.

4.12 Peripherals

4.12.1 Cyclic Redundancy Check (CRC)

The Cyclic Redundancy Check (CRC) calculation unit is used to obtain a CRC code using a configurable generator with a specified polynomial value and size. CRC-based techniques are commonly used to verify the integrity of data transmission or storage. In the scope of the EN/IEC 60335-1 standard, CRC-based techniques are utilized to ensure the integrity of Flash memory.

- Support 8/16/32-bit data input.
- For 8/16/32-bit input data length, the calculation cycles are 1/2/4 AHB clock cycles.
- The free 8-bit register is unrelated to calculation and can be used for any other goals by any other peripheral devices.
- User-configurable polynomial value and size.

4.12.2 IOs and Pins

Up to 56 I/O ports are implemented, all mappable on 16 external interrupt lines.

- Programmable pull-up or pull-down on all ports.
- Analog function (input and output buffer disabled)
- Alternate function selection registers
- Locking mechanism (GPIOx_LCKR) provided to freeze the I/O port configurations.

Each GPIO pin can be configured by software as output (push-pull or open-drain), input, peripheral alternate function, or analog function. All GPIO pins are shared with digital or analog alternate functions.

4.12.2.1 Wake-Up Pins

The devices are equipped with up to 5 wake-up pins, namely WKUP1, WKUP2, WKUP3, WKUP4, and WKUP5. For more information, please refer to the pin assignment table. These wake-up pins have the capability to wake the system from standby or shutdown mode.

4.12.2.2 TPSensor® Pins

There are up to 16 TPSensor® channels integrated into the devices. Meanwhile, there are additional 2 pins functional in specified packages (Shield and Guard pins for better performance). Please refer to the pin assignment table for details.

TPSensor Channel	Description
TPSensor_CH0, 1, 2, 3, 4 ... 15	TPSensor® input channel
GUARD	TPSensor® guard channel (can be acting as input channel if NOT using guard function)
SHIELD	TPSensor® shield channel

4.12.2.3 General-Purpose Input/Output (GPIO)

Each GPIO pin can be configured by software as an output, input or peripheral alternative function, such as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function (push-pull or open-drain). Most of the GPIO pins are shared with analog or digital alternate functions. Fast I/O toggling can be achieved that is mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked following a specific sequence to avoid spurious writing to the I/Os registers.

IO Type	Description
TTA	3.6 V tolerance I/O with analog switch, max clock up to 96 MHz, no protection on current flow inside MCU.
TTC	3.6 V tolerance I/O with analog switch, max clock up to 48 MHz.

IO Type	Description
TTF	3.6 V tolerance I/O with analog switch, max clock up to 120 MHz.
FTA	5 V tolerance I/O with analog switch, max clock up to 120 MHz, MCU power first for protecting current flow inside MCU.
FTC	5 V tolerance I/O with no analog switch and 5 mA drive strength, max clock up to 48 MHz, 3.4 Mbps I2C support.

4.12.3 Direct Memory Access Controller (DMA)

The device embeds 2 DMAs (DMA0, DMA1) and the features support:

- 8 independently configurable channels per each
- 4-level priorities option of DMA request channels by software and hardware
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/ destination addresses must be aligned with the data size
- Support for circular buffer management
- Support memory to memory, peripherals-to-memory, memory to peripheral, and peripheral-to-peripheral transfers
- Programmable number of data to be transferred: up to 65536

Table 5. DMA0 Request Mapping

DMA0 Request	Channel0	Channel1	Channel2	Channel3	Channel4	Channel5	Channel6	Channel7
Request0	ADC							
Request1		SPI0_RX	SPI0_TX	SPI1_RX	SPI1_TX	SPI2_RX	SPI2_TX	
Request2				UART3_TX	UART3_RX	UART5_TX	UART5_RX	
Request3		UART6_TX	UART6_RX	I2C0_TX	I2C0_RX	I2C1_TX	I2C1_RX	
Request4		ADVTMR0_CH0		ADVTMR0_CH3 ADVTMR0_TRIG ADVTMR0_COM	ADVTMR0_UP	ADVTMR0_CH1	ADVTMR0_CH2	
Request5	GPTMR0_CH2	GPTMR0_UP	GPTMR0_TRIG	GPTMR0_COM	GPTMR0_CH0			GPTMR0_CH1 GPTMR0_CH3
Request6		ADVTMR1_CH0		ADVTMR1_CH3 ADVTMR1_TRIG ADVTMR1_COM	ADVTMR1_UP	ADVTMR1_CH1	ADVTMR1_CH2	
Request7				HASH		AES_IN	AES_OUT	

Table 6. DMA1 Request Mapping

DMA1 Request	Channel0	Channel1	Channel2	Channel3	Channel4	Channel5	Channel6	Channel7
Request0	DAC	GPTMR5_CH0	GPTMR5_CH1	GPTMR5_CH2	GPTMR5_CH3	GPTMR5_UP	GPTMR5_TRIG	GPTMR5_COM
Request1		UART0_TX	UART0_RX	UART1_TX	UART1_RX	UART4_TX	UART4_RX	
Request2	GPTMR4_CH0	GPTMR4_CH1	GPTMR4_CH2	GPTMR4_CH3	GPTMR4_UP	GPTMR4_TRIG	GPTMR4_COM	
Request3	GPTMR1_CH2	GPTMR1_UP	GPTMR1_TRIG	GPTMR1_COM	GPTMR1_CH0			GPTMR1_CH1 GPTMR1_CH3
Request4	GPTMR2_CH2	GPTMR2_UP	GPTMR2_TRIG	GPTMR2_COM	GPTMR2_CH0			GPTMR2_CH1 GPTMR2_CH3
Request5		ADVTMR2_CH0		ADVTMR2_CH3 ADVTMR2_TRIG ADVTMR2_COM	ADVTMR2_UP	ADVTMR2_CH1	ADVTMR2_CH2	

DMA1 Request	Channel0	Channel1	Channel2	Channel3	Channel4	Channel5	Channel6	Channel7
Request6	GPTMR3_CH2	GPTMR3_UP	GPTMR3_TRIG	GPTMR3_COM	GPTMR3_CH0			GPTMR3_CH1 GPTMR3_CH3
Request7				HASH		AES_IN	AES_OUT	

4.12.4 Analog-to-Digital Converter (ADC)

The 12-bit SAR ADC module supports fast 12-bit analog-to-digital conversions with single-ended or differential inputs.

- Up to 2.2 Msps maximum conversion rate with full resolution
- Single-ended or differential mode inputs
- 12-bit/10-bit/8-bit programmable resolution
- Up to 20 input channels support, refer to Table 7 for details
- Scan conversion operation
  - Single and continuous conversion modes
  - Scan mode for automatic conversion of channel 0 to channel N
  - Start factors are software and timers trigger
  - Upper and lower limits can be specified
  - Either detection of within the range or without the range can be set
  - 20 FIFO stages for scan conversion and four FIFO stages for priority conversion are incorporated
  - An interrupt is generated when data is written in the specified count of FIFO stages
- Window comparison function
- DMA request generation during regular channel conversion
- Interrupt generation at ADC ready, the end of sampling, the end of conversion, end of sequence conversion, analog watchdog or overrun events
- External high accuracy reference support via VREF+/VREF- pins
- Temperature sensor with ±2°C accuracy

Table 7. ADC Input Channels

Sequence No.	ADC Channels	External Pin Output
0	A1	External pin
1	A2	External pin
2	A3	External pin
3	A4	External pin
4	A5	External pin
5	A6	External pin
6	A7	External pin
7	A8	External pin
8	A9	External pin
9	A10	External pin
10	A11	External pin
11	A12	External pin
12	A13	External pin

Sequence No.	ADC Channels	External Pin Output
13	A14	External pin
14	A15	OA0 (internal connection)
15	A16	OA1 (internal connection)
16	A17	On-chip temperature sensor (internal connection)
17	A18	1/2 V_{BAT} (internal connection)
18	A19	1/2 V_{DDA} (internal connection)
19	A20	VREFBUF (internal connection)

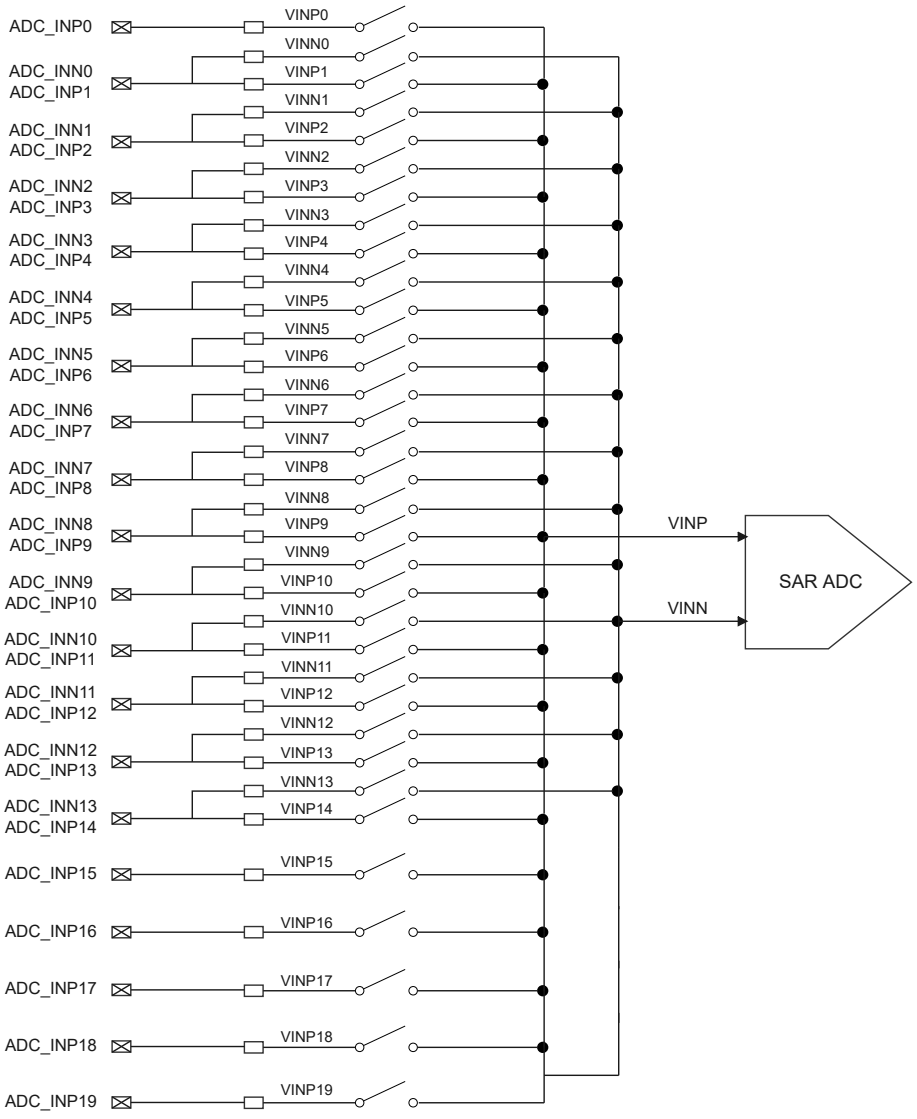


Figure 3. ADC Differential Mode Block Diagram (DIFSEL = 0 Single Mode)

Table 8. ADC Trigger Connections

EXTSEL[4:0]	Trigger Source		EXTSEL[4:0]	Trigger Source
00000	RTC_Wakeup event detection		01110	GPTMR5_Capture/Compare Interrupt

00001	CMP0_OUT		01111	EXTI line 15
00010	CMP1_OUT		10000	EXTI line 2
00011	GPTMR0_TRIG		10001	ADVTMR0_TRIG
00100	GPTMR0_Capture/Compare Interrupt		10010	ADVTMR0_TRIG2
00101	GPTMR1_TRIG		10011	ADVTMR0_Capture/Compare Interrupt
00110	GPTMR1_Capture/Compare Interrupt		10100	ADVTMR1_TRIG
00111	GPTMR2_TRIG		10101	ADVTMR1_TRIG2
01000	GPTMR2_Capture/Compare Interrupt		10110	ADVTMR1_Capture/Compare Interrupt
01001	GPTMR3_TRIG		10111	ADVTMR2_TRIG
01010	GPTMR3_Capture/Compare Interrupt		11000	ADVTMR2_TRIG2
01011	GPTMR4_TRIG		11001	ADVTMR2_Capture/Compare Interrupt
01100	GPTMR4_Capture/Compare Interrupt		11010	Reserved
01101	GPTMR5_TRIG		11011	Reserved

4.12.5 Digital-to-Analog Converter (DAC)

The Digital-to-Analog Converter (DAC) module is a 12-bit voltage output converter, capable of transforming digital signals into analog. The DACcan be configured in 8-bit or 12-bit mode with up to 1 Msps and can be configured 32K, 48K, and 96K sampling rates for audio applications.

- One DACcore with two output buffers
  - Left or right data alignment in 12-bit mode
  - Synchronized update capability
  - Noise-wave generation
  - Triangular-wave generation
  - External triggers for conversion
  - Input voltage reference for external V_{REF+}, or V_{DDA}

Table 9. DACTrigger Connections

EXTSEL[3:0]	DACTrigger source
0000	GPTMR0_otrg
0001	GPTMR1_otrg
0010	GPTMR2_otrg
0011	GPTMR3_otrg
0100	GPTMR4_otrg
0101	GPTMR5_otrg
0110	ADVTMR0_otrg
0111	ADVTMR1_otrg
1000	ADVTMR2_otrg
1001	EXTI4 (EXTI Line 4 interrupt pin)
1010	Reserved

4.12.6 Voltage Reference Buffer (VREFBUF)

The internal Voltage Reference Buffer (VREFBUF) supports three voltages: 1.5 V, 2.0 V, and 2.5 V.

An external voltage reference can be provided through the VREF+ pin when the internal VREFBUF is off.

The VREF+ pin is double-bonded with V_{DDA} on some packages. In these packages, the internal VREFBUF is not available.

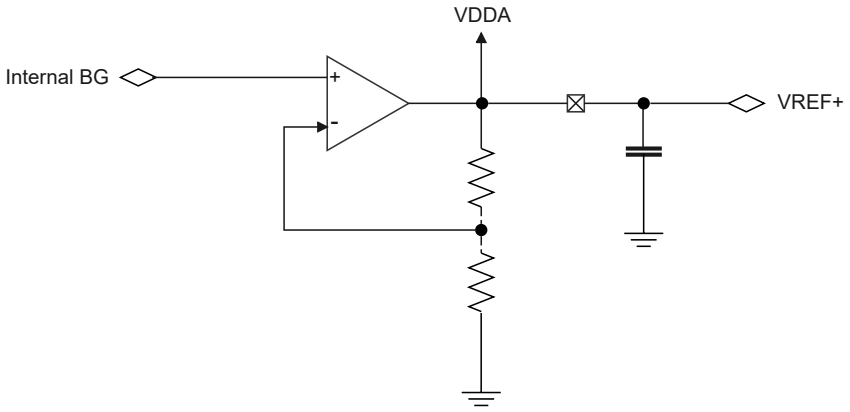


Figure 4. VREFUBUF Block Diagram

4.12.7 Comparator (CMP)

This device features two comparators, CMP0 and CMP1, with the following supporting details:

- Up to 8 input channels both for positive and negative ports
- Multiplexed with I/O pins
- Internal 6-bit DAC integrated for voltage reference
- Programmable hysteresis
- Output redirection to I/Os or to timer inputs for triggering break events for fast PWM shutdowns
- Output blanking for immunity to switching noise
- Per-channel interrupt generation with wake-up from sleep and standby modes

Table 10. CMP0 Input Channel Connections

INPSEL	CMP0 Channels	INNSEL	CMP0 Channels
000	External pin	000	External pin
001	External pin	001	External pin
010	Reserved	010	Reserved
011	Reserved	011	Reserved
100	VREFBUF	100	VREFBUF
101	DAC	101	DAC
110	OA0_OUT	110	OA1_OUT
111	Internal DAC6	111	Internal DAC6

Table 11. CMP1 Input Channel Connections

INPSEL	CMP1 Channels	INNSEL	CMP1 Channels
000	External pin	000	External pin

INPSEL	CMP1 Channels	INNSEL	CMP1 Channels
001	External pin	001	External pin
010	Reserved	010	Reserved
011	Reserved	011	Reserved
100	VREFBUF	100	VREFBUF
101	DAC	101	DAC
110	OA0_OUT	110	OA1_OUT
111	Internal DAC6	111	Internal DAC6

Table 12. CMP0/CMP1 Output Channel Connections

CMP0 OUT	External Pinout, Module	CMP1 OUT	External Pinout, Module
CMP0_OUT	External pin (CMP0_OUT)	CMP1_OUT	External pin (CMP1_OUT)
	Internal to Timers (refer to Timer interconnection tables in Timers → Timers for details)		Internal to Timers (refer to Timer interconnection tables in Timers → Timers for details)
	Internal to ADC		Internal to ADC
	Reserved		Reserved

Table 13. CMP0/CMP1 Blanking Sources

Value	CMP0	CMP1
000	ADVTMR0_CH4_OC	ADVTMR0_CH4_OC
001	ADVTMR1_CH4_OC	ADVTMR1_CH4_OC
010	ADVTMR2_CH4_OC	ADVTMR2_CH4_OC
011	GPTMR0_CH1_OC	GPTMR0_CH1_OC
100	GPTMR1_CH1_OC	GPTMR1_CH1_OC
101	GPTMR2_CH1_OC	GPTMR2_CH1_OC
110	GPTMR3_CH3_OC	GPTMR3_CH3_OC
111	GPTMR4_CH3_OC	GPTMR4_CH3_OC

4.12.8 Operational Amplifier (OA)

This device embedded two Operational Amplifiers (OAs): OA0 and OA1.

- Rail-to-rail input and output voltage range
- Multiplexed with I/O pins
- Up to 4 input channels both for positive and negative ports
- Programmable gain up to 65x

Table 14. OA0 Input Channel Connections

PSEL	OA0 Channels	NSEL	OA0 Channels
00	External pin (OA0_INP)	00	External pin (OA0_INN)
01	DAC	01	Reserved

PSEL	OA0 Channels	NSEL	OA0 Channels
10	Reserved	10	Reserved
11	Reserved	11	Reserved

Table 15. OA1 Input Channel Connections

PSEL	OA1 Channels	NSEL	OA1 Channels
00	External pin (OA1_INP)	00	External pin (OA1_INN)
01	DAC	01	Reserved
10	OA0_Out	10	OA0_Out
11	Reserved	11	Reserved

4.12.9 TPSensor®

The TPSensor® offers:

- Support for up to 12 individual capacitance touch channels
- Both self-capacitance and mutual-capacitance sensing techniques
- Spread-spectrum clocks for low radiated emissions
- Support for synchronized conversion on a zero-crossing event trigger
- Best-in-class liquid tolerance
- Superior immunity against external noise
- Wake-on-touch functionality support

4.12.10 Timers and Watchdogs

The devices include:

- Three Advanced Timers (ADVTMR)
- Six General-Purpose Timers (GPTMR)
- One Independent Watchdog (IWDG)
- One Window Watchdog (WWDG)
- One SysTick Timer

4.12.10.1 General-Purpose Timer (GPTMR)

There are up to six synchronizable General-Purpose Timers (GPTMR0, GPTMR1, GPTMR2, GPTMR3, GPTMR4, GPTMR5) embedded in the TSP325M5A devices. Each GPTMR can be used to generate PWM outputs, or act as a simple time base.

GPTMR0, GPTMR1, GPTMR2, GPTMR3 and GPTMR4 have a 16-bit auto-reload up/downcounter and 16-bit prescaler.

GPTMR5 has a 32-bit auto-reload up/downcounter and 32-bit prescaler.

These timers feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

4.12.10.2 Advanced Timer (ADVTMR)

The Advanced Timer (ADVTMR0, ADVTMR1, ADVTMR2) for motor control can each be seen as a four-phase PWM multiplexed on 8 channels. They have complemenary PWM outputs with programmable inserted dead-times. They can also be seen a complete GPTMR.

The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation
- One-pulse mode output

4.12.10.3 Watchdog Timer

The TSP325M5A devices integrate 2 watchdog timers: Indpendent Watchdog (IWDG) and Window Watchdog (WWDG).

Indpendent Watchdog (IWDG)

The Independent Watchdog (IWDG) is based on a 12-bit downcounter and an 8-bit prescaler. It is clocked from an independent 32 kHz Internal Low-Speed (ILS) RC, and as it operates independently from the main clock, it can operate in stop and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes.

Additionally, the IWDG can be sourced from ELS when it functions as a software watchdog.

Window Watchdog (WWDG)

The Window Watchdog (WWDG) is based on a 7-bit down-counter that can be set as free running. It serves as a watchdog, capable of resetting the device when an issue is detected. Its clocking is derived from the main clock, and it features an early warning interrupt function.

4.12.10.4 SysTick Timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

4.12.11 Real-Time Clock (RTC)

The RTC supports the following features:

- Calendar with subsecond, seconds, minutes, hours (in 12 or 24-hour format), weekday, date, month, and year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- Real-time correction from 1 to 32767 RTC clock, allowing synchronization with a master clock.
- Reference clock detection: Using a more precise second source clock (50 or 60 Hz) to boost calendar precision.
- A timestamp feature for saving the current calendar data. This can be triggered by an event on the timestamp pin or by a switch to VBAT mode.
- A 17-bit auto-reload Wakeup Timer (WUT) for periodic events with programmable resolution and period.
- 32 x 32-bit backup registers, retained in all low-power modes. Ideal for storing sensitive data, these registers are not reset by a system power reset or when the device wakes up from standby or shutdown mode.

4.12.12 Inter-Integrated Circuit (I2C)

The I2C interface is an internal circuit that allows communication with an external I2C interface. This external interface is an industry-standard two-line serial interface (SCL, SDA) used for connection to external hardware.

The device has two embedded I2C modules (I2C0, I2C1). Refer to Table 16 for the features implementation.

The I2C features are as follows:

- Support slave and master modes, multi-master capability
- Support up to 1 Mbit/s Fast-mode Plus (Fm+) and 20 mA output drive I/Os
- 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
- Optional clock stretching
- SMBus 2.0 compatibility
- PMBus 1.1 compatibility
- Wake up from Sleep mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 16. I2C Implementation

I2C Features (1)	I2C0	I2C1
7-bit addressing mode	√	√
10-bit addressing mode	√	√
Standard-mode (up to 100 Kbit/s)	√	√
Fast-mode (up to 400 Kbit/s)	√	√
Fast-mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	√	√
Independent clock	√	√
SMBus/PMBus	√	√

(1) √ = Supported.

4.12.13 Universal Asynchronous Receiver/Transmitter (UART)

The UART is used to translate data between parallel serial interfaced, provides a flexible full duplex data exchange using synchronous/asynchronous transfer.

The device embedded 6 UARTs (UART0, UART1, UART3, UART4, UART5, UART6).

The UART features as below:

- Single-wire half-duplex communication
- Supports both asynchronous and clocked synchronous serial communication modes
- Programmable baud rate generator and auto baud rate detection
- LIN break generation and detection
- Dual clock domain
- TX-FIFO/RX-FIFO status interrupts when FIFO mode is enabled
- Single-wire half-duplex communication
- Data length support 7, 8, 9 bits
- Support DMA for continuous communication

4.12.14 Serial Peripheral Interface (SPI)/Integrated Interchip Sound (I2S)

The device embedded two SPI/I2S interfaces (SPI/I2S 0, SPI/I2S 1).

The SPI features are as below:

- SPI interfaces with a frequency of up to 30 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking
- Separate transmit and receive 32-bit FIFO with DMA capability
- Data frame size can be 4 to 16 bits
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- NSS management by hardware or software for both master and slave dynamic change of master/slaver operation
- Enhanced TI and NSS pulse modes, SPI Motorola support

The I2S features are as below:

- Data format may be 16-bit, 20-bit, 24-bit or 32-bit
- Sampling frequency from 8 kHz to 192 kHz
- Support either master or slave mode
- Full-duplex/half-duplex communication
- Packet frame is fixed to 16-bit (16-bit data frame) or 32-bit (16-bit, 20-bit, 24-bit, 32-bit data frame) by audio channel
- Supported I2S protocols
  - I2S Philips standard
  - MSB-justified standard (left-justified)
  - LSB-justified standard (right-justified)
  - PCM standard (with short and long frame synchronization on 16-bit channel frame or 16-bit data frame extended to 32-bit channel frame)
- DMA capability for transmission and reception

4.12.15 Controller Area Network (CAN2.0B)

The CAN module is a communication controller that implements the CAN protocol, conforming to the ISO 11898-1 Standard and the CAN Specification 2.0 Part B.

- Standard/extended data frames
- Up to 1 Mbit/s
- Up to 8 bytes payload
- Configurable Receive Buffer (RB) size
  - Up to 8 slots
  - FIFO-like behavior
  - Received frames that are "not accepted" or "incorrect" will not overwrite the frames already stored
- Two Transmit Buffers
  - Primary Transmit Buffer (PTB) (one frame slot)
  - Configurable Secondary Transmit Buffer (STB). Support up to 8 slots, operation in FIFO or priority decision mode
- Independent and programmable internal acceptable filters (up to 4 acceptable filters)
- Extended features

- Limitation of re-arbitration and retransmission (1 to 7 or "unlimited" attempts)
- Listen only mode
- Loopback mode (internal and external)
- Transceiver standby mode

- Time-stamping (CiA 603 time-stamping, external 16-bit counter)

4.12.16 Accelerator Encryption Engine

4.12.16.1 True Random Number Generator (TRNG)

The True Random Number Generator (TRNG) module can generate a 32-bit random value by using continuous analog noise. It can be disabled to reduce power consumption.

4.12.16.2 Advanced Encryption Standard (AES)

- Compliance with NIST Advanced Encryption Standard (AES), FIPS publication 197 from November 2001
- 128-bit data block processing
- Support for cipher key lengths of 128-bit,192-bit and 256-bit
- Encryption and decryption with multiple chaining modes:
  - Electronic Codebook (ECB) mode
  - Cipher Block Chaining (CBC) mode
  - Counter (CTR) mode
  - Cipher Feedback 1, 128 (CFB)
  - Output Feedback 1, 128 (OFB)
- 4x32-bit buffer for data input and output
- Data-swapping logic to support 1-bit, 8-bit, 16-bit or 32-bit data
- 256-bit register for storing the cryptographic key (eight 32-bit registers)
- 128-bit register for storing initialization vector (four 32-bit registers)

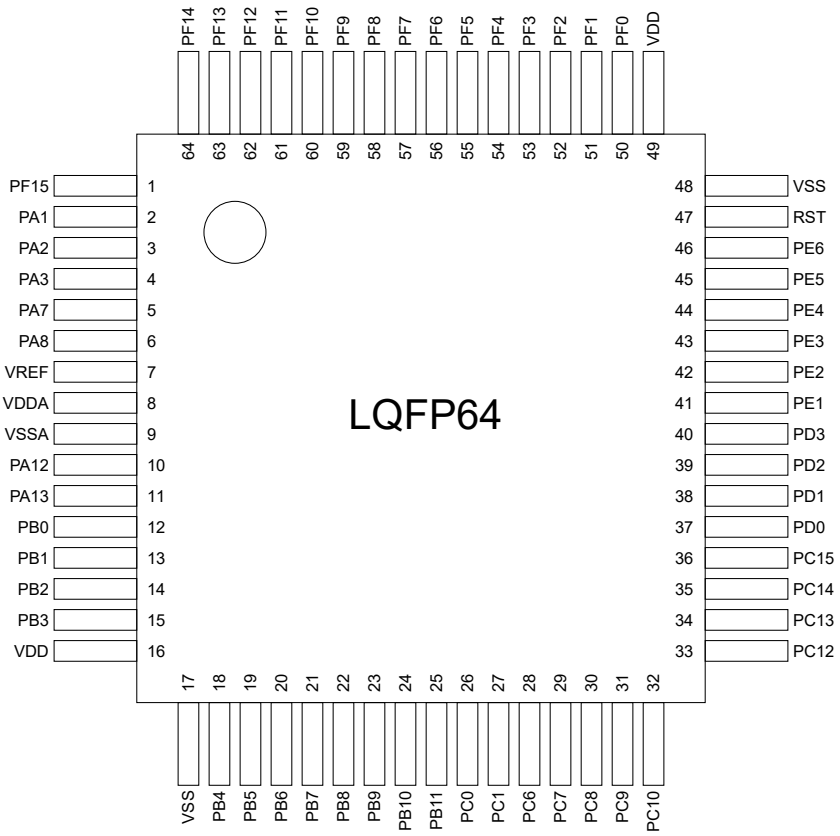
4.12.16.3 HASH

The HASH module supports popular hash algorithms, including SHA-1, SHA-256, SHA-224, and MD5. The HASH module features as below:

- Federal Information Processing Standards Publication FIPS PUB 180-4, (SHA-1 and SHA-2 family)
- Corresponding 32-bit words of the digest from consecutive message blocks are added to each other to form the digest of the whole message
- Automatic padding to complete the input bit string to fit digest minimum block size of 512 bits (16 × 32 bits)
- Single 32-bit input register associated to an internal input FIFO of sixteen 32-bit words, corresponding to one block size
- 8 × 32-bit words (H0 to H7) for output message digest
- Automatic data flow control with support of Direct Memory Access (DMA) using one channel. Fixed burst of 4 supported

5 Pinouts and Pin Description

5.1 LQFP-64 Pinout Description



5.2 Pin Definition

Name	Abbreviation	Definition
Pin Type	Power	Power supply pins (V_{DD}, V_{SS}, V_{DDA}, V_{SSA}, V_{BAT}, V_{REF+}, V_{REF-})
	I/O	Input/Output pins
	I	Input pins
	O	Output pins
	NRST	Bidirectional reset pin with embedded weak pull-up resistor
I/O structure	TTA	3.6 V tolerance I/O with analog switch, max clock up to 96 MHz, no protection on current flow inside MCU.
	TTC	3.6 V tolerance I/O with analog switch, max clock up to 48 MHz.
	TTF	3.6 V tolerance I/O with analog switch, max clock up to 120 MHz.
	FTA	5 V tolerance I/O with analog switch, max clock up to 120 MHz, MCU power first for protecting current flow inside MCU.
	FTC	5 V tolerance I/O with no analog switch and 5mA drive strength, max clock up to 48 MHz, 3.4 Mbps I2C support.
Pin function	Alternate function	The functions can be selected and controlled through the registers GPIOx_AFRH and GPIOx_AFRL.
	Additional function	The functions can be enabled/disabled through the peripheral registers.

Note: All I/Os are set as analog mode during and after a reset, except the port PE2, PE3, PE4, PE5, PE6.

LQFP-64	Pad Name	Pin Type	IO Structure	Analog Function	Additional Function
1	PF15	I/O	TTF	OA0_OUT	
2	PA1	I/O	TTC	ADC_IN1	
3	PA2	I/O	TTC	ADC_IN2	
4	PA3	I/O	TTC	ADC_IN3	
5	PA7	I/O	TTC	ADC_IN7/DAC_OUT0	
6	PA8	I/O	TTC	ADC_IN8/DAC_OUT1	

LQFP-64	Pad Name	Pin Type	IO Structure	Analog Function	Additional Function
7	VREF	Power	VREF	VREF	
8	VDDA	Power	VDDA		
9	VSSA	Power	VSSA		
10	PA12	I/O	TTC	ADC_IN12/GUARD	
11	PA13	I/O	TTC	ADC_IN13/SHIELD	
12	PB0	I/O	TTA	TPSensor_CH2	
13	PB1	I/O	TTA	TPSensor_CH3	
14	PB2	I/O	TTA	TPSensor_CH4	
15	PB3	I/O	TTA	TPSensor_CH5	
16	VDD	Power	VDD		
17	VSS	Power	VSS		
18	PB4	I/O	TTA	TPSensor_CH6	
19	PB5	I/O	TTA	TPSensor_CH7	
20	PB6	I/O	TTA	TPSensor_CH8	
21	PB7	I/O	TTA	TPSensor_CH9	
22	PB8	I/O	TTA	TPSensor_CH10	
23	PB9	I/O	TTA	TPSensor_CH11	
24	PB10	I/O	TTA	TPSensor_CH12	
25	PB11	I/O	TTA	TPSensor_CH13	
26	PC0	I/O	TTA	OSCH_IN	
27	PC1	I/O	TTA	OSCH_OUT	
28	PC6	I/O	TTF		
29	PC7	I/O	FTA		
30	PC8	I/O	FTC		

LQFP-64	Pad Name	Pin Type	IO Structure	Analog Function	Additional Function
31	PC9	I/O	FTC		
32	PC10	I/O	FTC		
33	PC12	I/O	TTF		
34	PC13	I/O	TTF		
35	PC14	I/O	TTF		
36	PC15	I/O	TTF		
37	PD0	I/O	TTC		
38	PD1	I/O	TTC		
39	PD2	I/O	TTC		
40	PD3	I/O	FTC		
41	PE1	I/O	FTA		
42	PE2	I/O	FTA		
43	PE3	I/O	FTA		
44	PE4	I/O	FTA		
45	PE5	I/O	FTA		
46	PE6	I/O	FTA		
47	RST	RST	NRST		
48	VSS	Power	VSS		
49	VDD	Power	VDD		
49	VBAT	Power	VBAT		
50	PF0	I/O	TTF		
51	PF1	I/O	TTF		
52	PF2	I/O	FTC		
53	PF3	I/O	FTC		

LQFP-64	Pad Name	Pin Type	IO Structure	Analog Function	Additional Function
54	PF4	I/O	TTC		
55	PF5	I/O	TTC		
56	PF6	I/O	TTC	CMP1_INP1	
57	PF7	I/O	TTC	CMP1_INP0	WKUP2
58	PF8	I/O	TTF	CMP0_INP1	
59	PF9	I/O	TTF	CMP0_INP0	WKUP3
60	PF10	I/O	TTF	OA1_INP/CMP1_INN1	
61	PF11	I/O	TTF	OA1_INN/CMP1_INN0	
62	PF12	I/O	TTF	OA1_OUT	
63	PF13	I/O	TTF	OA0_INP/CMP0_INN1	
64	PF14	I/O	TTF	OA0_INN/CMP0_INN0	

Note: For Alternate Functions (AF), please refer to Alternate Function for the configuration details.

5.3 Alternate Function

Table 17. Alternate Function

Port A … Port F (PA … PF)	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SWD/TRACE	I2C 0/1, UART 0/1/3/4/5/6, SPI&I2S 0/1, QSPI, CAN	I2C 0/1, UART 3/4/5, SPI&I2S 0/1/2, CAN	I2C 1, ADVTMR 0, SPI&I2S 0, QSPI, CAN, GPTMR 0/1/2/3/5	I2C 0, UART 0, SPI&I2S 1/2, CAN, GPTMR 1/2/4, ADVTMR 0/1/2	UART 4/5, SPI&I2S 1, GPTMR 2/4, ADVTMR 1/2	N/A	EVENT
PA0		I2C0_SDA	SPI2_MOSI_I2S2_SDO	GPTMR0_CH0				EVENTOUT
PA1		I2C0_SCL	SPI2_MISO_I2S2_SDI	GPTMR0_CH0N	UART0_TX			EVENTOUT
PA2		I2C0_SMBA	SPI2_SCK_I2S2_CK	GPTMR0_CH1	UART0_RX			EVENTOUT
PA3			SPI2_NSS0_I2S2_WS	GPTMR0_CH1N				EVENTOUT
PA4		UART0_CTS	I2S2_MCK	GPTMR0_CH2				EVENTOUT
PA5		UART0_RTS_DE		GPTMR0_CH2N				EVENTOUT
PA6		UART0_TX		GPTMR0_CH3				EVENTOUT
PA7		UART0_RX		GPTMR0_ETRG	GPTMR1_CH0			EVENTOUT
PA8		UART0_TX		GPTMR0_BKIN	GPTMR1_CH0N			EVENTOUT
PA9		UART0_RX		GPTMR1_CH0				EVENTOUT
PA10		UART1_TX		GPTMR1_CH0N				EVENTOUT
PA11		UART1_RX		GPTMR1_CH1				EVENTOUT
PA12	MCO	I2C1_SDA		GPTMR1_CH1N	GPTMR1_CH1			EVENTOUT
PA13		I2C1_SCL	UART1_CTS	GPTMR1_CH2	GPTMR1_CH1N			EVENTOUT
PA14		I2C1_SMBA		GPTMR1_CH2N	GPTMR1_CH2			EVENTOUT
PA15		UART1_CTS	I2S1_MCK	GPTMR1_CH3	GPTMR1_CH2N			EVENTOUT

Table 18. Alternate Function

Port A…Port F (PA … PF)	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SWD/TRACE	I2C 0/1, UART 0/1/3/4/5/6, SPI&I2S 0/1, QSPI, CAN	I2C 0/1, UART 3/4/5, SPI&I2S 0/1/2, CAN	I2C 1, ADVTMR 0, SPI&I2S 0, QSPI, CAN, GPTMR 0/1/2/3/5	I2C 0, UART 0, SPI&I2S 1/2, CAN, GPTMR 1/2/4, ADVTMR 0/1/2	UART 4/5, SPI&I2S 1, GPTMR 2/4, ADVTMR 1/2	N/A	EVENT
PB0		UART1_RTS_DE	SPI1_NSS0_I2S1_WS		GPTMR1_CH3			EVENTOUT
PB1		UART1_TX	SPI1_SCK_I2S1_CK	GPTMR1_BKIN				EVENTOUT
PB2		UART1_RX	SPI1_MISO_I2S1_SDI	GPTMR2_BKIN	GPTMR1_ETRG			EVENTOUT
PB3			SPI1_MOSI_I2S1_SDO	GPTMR2_ETRG				EVENTOUT
PB4		SPI1_NSS0_I2S1_WS		GPTMR2_CH3				EVENTOUT
PB5		SPI1_SCK_I2S1_CK		GPTMR2_CH2N				EVENTOUT
PB6		SPI1_MISO_I2S1_SDI		GPTMR2_CH2				EVENTOUT
PB7		SPI1_MOSI_I2S1_SDO		GPTMR2_CH1N				EVENTOUT
PB8		I2S1_MCK	I2C1_SMBA	GPTMR2_CH1				EVENTOUT
PB9		I2C1_SCL	CAN_STBY	GPTMR2_CH0N				EVENTOUT
PB10		I2C1_SDA	CAN_RX	GPTMR2_CH0				EVENTOUT
PB11	RTC_REFIN		CAN_TX	GPTMR3_CH0	GPTMR2_ETRG			EVENTOUT
PB12		UART2_RX	I2C1_SDA	GPTMR3_CH0N	GPTMR2_BKIN	SPI1_NSS3_I2S1_WS		EVENTOUT
PB13		UART2_TX	I2C1_SCL	GPTMR3_CH1		SPI1_NSS2_I2S1_WS		EVENTOUT
PB14		UART2_RTS_DE	I2C1_SMBA	GPTMR3_CH1N		SPI1_NSS3_I2S1_WS		EVENTOUT
PB15		UART2_CTS		GPTMR3_CH2				EVENTOUT

Table 19. Alternate Function

Port A…Port F (PA … PF)	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SWD/TRACE	I2C 0/1, UART 0/1/3/4/5/6, SPI&I2S 0/1, QSPI, CAN	I2C 0/1, UART 3/4/5, SPI&I2S 0/1/2, CAN	I2C 1, ADVTMR 0, SPI&I2S 0, QSPI, CAN, GPTMR 0/1/2/3/5	I2C 0, UART 0, SPI&I2S 1/2, CAN, GPTMR 1/2/4, ADVTMR 0/1/2	UART 4/5, SPI&I2S 1, GPTMR 2/4, ADVTMR 1/2	N/A	EVENT
PC0				GPTMR3_CH2N				EVENTOUT
PC1				GPTMR3_CH3				EVENTOUT
PC2	RFIDCLK	UART2_RX		GPTMR3_ETRG	SPI1_NSS1_I2S1_WS	GPTMR4_BKIN		EVENTOUT
PC3		UART2_TX	SPI1_MISO_I2S1_SDI	I2C1_SMBA	GPTMR3_BKIN	GPTMR4_ETRG		EVENTOUT
PC4		I2C1_SCL	SPI1_MOSI_I2S1_SDO		GPTMR4_CH3			EVENTOUT
PC5		I2C1_SDA	SPI1_SCK_I2S1_CK		GPTMR4_CH2N			EVENTOUT
PC6	MCO	UART3_CTS	SPI1_NSS0_I2S1_WS	I2S0_MCK	GPTMR4_CH2	GPTMR2_BKIN		EVENTOUT
PC7	MCO	UART3_RTS_DE	SPI0_NSS0_I2S0_WS		GPTMR4_CH1N			EVENTOUT
PC8		UART3_TX	SPI0_SCK_I2S0_CK	I2C1_SDA	GPTMR4_CH1			EVENTOUT
PC9		UART3_RX	SPI0_MISO_I2S0_SDI	I2C1_SCL	GPTMR4_CH0N	ADVTMR2_BKIN		EVENTOUT
PC10			SPI0_MOSI_I2S0_SDO	I2C1_SMBA	GPTMR4_CH0	ADVTMR2_BKIN2		EVENTOUT
PC12		SPI1_NSS0_I2S1_WS	UART3_RX		ADVTMR2_CH0			EVENTOUT
PC13		SPI1_SCK_I2S1_CK	UART3_TX	SPI0_NSS3_I2S0_WS	ADVTMR2_CH0N			EVENTOUT
PC14		SPI1_MISO_I2S1_SDI		SPI0_NSS2_I2S0_WS	ADVTMR2_CH1			EVENTOUT
PC15		SPI1_MOSI_I2S1_SDO	I2S0_MCK	SPI0_NSS1_I2S0_WS	ADVTMR2_CH1N			EVENTOUT

Table 20. Alternate Function

Port A…Port F (PA … PF)	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SWD/TRACE	I2C 0/1, UART 0/1/3/4/5/6, SPI&I2S 0/1, QSPI, CAN	I2C 0/1, UART 3/4/5 ,SPI&I2S 0/1/2, CAN	I2C 1, ADVTMR 0, SPI&I2S 0, QSPI, CAN, GPTMR 0/1/2/3/5	I2C 0, UART 0,SPI&I2S 1/2, CAN,GPTMR 1/2/4, ADVTMR 0/1/2	UART 4/5, SPI&I2S 1, GPTMR 2/4, ADVTMR 1/2	N/A	EVENT
PD0		SPI0_NSS0_I2S0_WS	I2S1_MCK		ADVTMR2_CH2			EVENTOUT
PD1		SPI0_SCK_I2S0_CK	UART4_RX	CAN_TX	ADVTMR2_CH2N	ADVTMR1_ETRG		EVENTOUT
PD2	I2C0_SCL	SPI0_MISO_I2S0_SDI	UART4_TX	CAN_RX	ADVTMR2_CH3	ADVTMR1_BKIN		EVENTOUT
PD3		SPI0_MOSI_I2S0_SDO	I2C0_SDA	CAN_STBY	ADVTMR2_ETRG	UART4_RTS_DE		EVENTOUT
PD4		UART4_RX	I2C0_SCL	SPI0_NSS1_I2S0_WS	ADVTMR2_BKIN	ADVTMR1_BKIN2		EVENTOUT
PD7		UART4_TX	I2C0_SMBA	SPI0_NSS2_I2S0_WS	ADVTMR2_BKIN2			EVENTOUT
PD8	TRACED3	UART4_RTS_DE		SPI0_NSS3_I2S0_WS	ADVTMR1_BKIN2			EVENTOUT
PD9		UART4_CTS						EVENTOUT
PD10		I2C0_SDA						EVENTOUT
PD11	TRACED2	I2C0_SCL			ADVTMR1_BKIN			EVENTOUT
PD12	TRACED1	I2C0_SMBA		CAN_TX	ADVTMR1_ETRG			EVENTOUT

Table 21. Alternate Function

Port A…Port F (PA … PF)	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SWD/TRACE	I2C 0/1, UART 0/1/3/4/5/6, SPI&I2S 0/1, QSPI, CAN	I2C 0/1, UART 3/4/5, SPI&I2S 0/1/2, CAN	I2C 1, ADVTMR 0, SPI&I2S 0, QSPI, CAN, GPTMR 0/1/2/3/5	I2C 0, UART 0, SPI&I2S 1/2, CAN, GPTMR 1/2/4, ADVTMR 0/1/2	UART 4/5, SPI&I2S 1, GPTMR 2/4, ADVTMR 1/2	N/A	EVENT
PE0	TRACED0		SPI2_NSS0_I2S2_WS	CAN_RX	ADVTMR1_CH3			EVENTOUT
PE1	TRACECK	CAN_STBY	SPI2_SCK_I2S2_CK	QSPI_CLK	ADVTMR1_CH2N	UART4_CTS		EVENTOUT
PE2	JTRST	I2S0_MCK	SPI2_MISO_I2S2_SDI	QSPI_IO0	ADVTMR1_CH2	ADVTMR2_BKIN		EVENTOUT
PE3	JTDO_TRACESWO	SPI0_SCK_I2S0_CK	SPI2_MOSI_I2S2_SDO	QSPI_IO1	ADVTMR1_CH1N	ADVTMR2_BKIN2		EVENTOUT
PE4	JTDI	SPI0_NSS0_I2S0_WS		QSPI_IO2	ADVTMR1_CH1			EVENTOUT
PE5	JTMS_SWDIO	SPI0_MOSI_I2S0_SDO	UART4_RX	QSPI_IO3	ADVTMR1_CH0N			EVENTOUT
PE6	JTCK_SWCLK	SPI0_MISO_I2S0_SDI	UART4_TX	QSPI_CS	ADVTMR1_CH0			EVENTOUT
PE7								EVENTOUT
PE8								EVENTOUT
PE9		QSPI_CS	SPI2_MOSI_I2S2_SDO	ADVTMR0_CH0	CAN_STBY			EVENTOUT
PE10	LSCO	QSPI_IO3	SPI2_MISO_I2S2_SDI	ADVTMR0_CH0N	CAN_RX			EVENTOUT
PE11	BOOT	QSPI_IO2	SPI2_SCK_I2S2_CK	ADVTMR0_CH1	CAN_TX			EVENTOUT
PE12	NMI	QSPI_IO1	SPI2_NSS0_I2S2_WS	ADVTMR0_CH1N		UART5_CTS		EVENTOUT

Table 22. Alternate Function

Port A…Port F (PA … PF)	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SWD/TRACE	I2C 0/1, UART 0/1/3/4/5/6, SPI&I2S 0/1, QSPI, CAN	I2C 0/1, UART 3/4/5, SPI&I2S 0/1/2, CAN	I2C 1, ADVTMR 0, SPI&I2S 0, QSPI, CAN, GPTMR 0/1/2/3/5	I2C 0, UART 0, SPI&I2S 1/2, CAN, GPTMR 1/2/4, ADVTMR 0/1/2	UART 4/5, SPI&I2S 1, GPTMR 2/4, ADVTMR 1/2	N/A	EVENT
PF0		QSPI_IO0	I2C0_SDA	ADVTMR0_CH2	SPI2_NSS3_I2S2_WS			EVENTOUT
PF1		QSPI_CLK	I2C0_SCL	ADVTMR0_CH2N	I2S2_MCK			EVENTOUT
PF2		UART5_RX	I2C0_SMBA	ADVTMR0_CH3				EVENTOUT
PF3		UART5_TX		ADVTMR0_ETRG				EVENTOUT
PF4		UART5_RTS_DE	UART4_RX	ADVTMR0_BKIN				EVENTOUT
PF5		UART5_CTS	UART4_TX	ADVTMR0_BKIN2				EVENTOUT
PF6			UART5_RX	CMP1_OUT	ADVTMR0_CH3			EVENTOUT
PF7		UART5_CTS	UART5_TX	GPTMR5_BKIN	ADVTMR0_ETRG			EVENTOUT
PF8		UART5_RTS_DE	CMP1_OUT	GPTMR5_ETRG	ADVTMR0_BKIN	QSPI_IO0		EVENTOUT
PF9		UART5_TX	CMP0_OUT	GPTMR5_CH3	ADVTMR0_BKIN2	QSPI_CLK		EVENTOUT
PF10		UART5_RX	CMP0_OUT	GPTMR5_CH2N	SPI2_NSS2_I2S2_WS			EVENTOUT
PF11			I2S2_MCK	GPTMR5_CH2	SPI2_NSS1_I2S2_WS			EVENTOUT
PF12		UART6_CTS	SPI2_NSS0_I2S2_WS	GPTMR5_CH1N				EVENTOUT
PF13		UART6_RTS_DE	SPI2_SCK_I2S2_CK	GPTMR5_CH1	I2C0_SDA			EVENTOUT
PF14		UART6_TX	SPI2_MISO_I2S2_SDI	GPTMR5_CH0N	I2C0_SCL			EVENTOUT
PF15		UART6_RX	SPI2_MOSI_I2S2_SDO	GPTMR5_CH0	I2C0_SMBA			EVENTOUT

6 Electronical Characteristics

6.1 Absolute Maximum Ratings (1) (2)

Symbol	Parameter	MIN	MAX	UNIT
Temperature	Junction temperature, T_J	–40	125	°C
	Operating Temperature Range, T_A	-40	105	°C
	Storage temperature, TSTG	-50	150	°C
$\lvert\Delta V_{DDx}\rvert$	Variations between different VDDX power pins of the same domain		50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins		50	mV
$V_{REF+}-V_{DDA}$	Allowed voltage difference for $V_{REF+} > V_{DDA}$		0.4	V

(1) Stresses beyond those listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.

(2) All main power (V_{DD}, V_{DDA}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

6.2 ESD Rating (1) (2)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A= 25 °C, conforming to ANSI/ ESDA/JEDEC JS-001			6000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A= 25 °C, conforming to ANSI/ ESDA/JEDEC JS-002			500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±6000 V may actually have higher performance.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

6.3 Static Latch-up (1) (2)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
L_U	Static latch-up class	T_A = +25 °C, conforming to JESD78E			150	mA

(1) A supply overvoltage is applied to each power supply pin.

(2) A current injection is applied to each input, output and configurable I/O pin.

6.4 Thermal Characteristics (1) (2)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
Θ_{JA}	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm			48.2		°C/W

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
	Thermal resistance junction-ambient QFN88 - 10 × 10 mm			20.7		°C/W
	Thermal resistance junction-ambient LQFP80 - 12 × 12 mm			39.36		°C/W
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm			45.4		°C/W

(1) T_J max = T_A max + (P_D max x Θ_{JA}), T_A max is the maximum abient temperature, Θ_{JA} is the package junction to ambient resistance, P_D max is the sum of P_{INT} max and PI/O max (P_D max = P_{INT} max + $P_{I/O}$max),P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

(2) $P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ ((V_{DDIOx} – V_{OH}) × I_{OH}), taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

6.5 Current Characteristics (1) (2)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
Σ_{IVDD}	Total current into sum of all V_{DD} power lines (source)				150	mA
Σ_{IVSS}	Total current out of sum of all V_{SS} ground lines (sink)				150	mA
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source)				100	mA
$I_{VSS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)				100	mA
$I_{IO(PIN)}$	Output current sunk by any I/O except FTC				20	mA
	Output current sunk by any I/O of FTC				5.0	mA
$\Sigma_{IIO(PIN)}$	Total output current sunk/sourced by sum of all I/Os and control pins				100	mA

(1) All main power (V_{DD}, V_{DDA}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

(2) This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.

6.6 Recommended Operating Conditions

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
V_{DD}	Standard operating voltage		1.71		3.6	V
V_{DDA} (1) (2)	Analog supply voltage		1.71		3.6	V
V_{BAT}(3)	Backup operating voltage		1.71		3.6	V
$C_{VDD/VDDA}$(4)	Recommended capacitor for power supply		4.7	10		μF

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
C_{VREF+}(5)	Recommended capacitor for V_{REF+}			1.0		μF
V_{IO}	I/O input voltage	TTA&TTC	-0.3		V_{DD}+0.3	V
		FTC	-0.3		5.0	V
		FTA	-0.3		min (V_{DD}/ V_{DDA}, + 3.6V)	V
Temperature	Junction temperature, T_J		–40		125	°C
	Ambient Temperature, T_A	Refer to Part numbers for details	-40		105	°C
		Refer to Part numbers for details	-40		85	°C
f_{HCLK}	Internal AHB clock frequency				156	MHz
f_{PCLK}	Internal APB clock frequency				156	MHz
$t_{VDD/VDDA}$	Power supply rise time rate		2		∞	μs/V
	Power supply falling time rate	Active mode	33		∞	μs/V
		Low power mode	200		∞	μs/V

(1) Modules can have a different supply voltage range specification. See the specification of the respective module in this data sheet.

(2) Modules can have a different supply voltage range specification. See the specification of the respective module in this data sheet.

(3) In some applications, this pin can connect external capacitors for main power battery replacement while RTC data is maintained.

(4) A capacitor tolerance of ±20% or better is required. A low-ESR ceramic capacitor of 100 nF (minimum) should be placed as close as possible (within a few millimeters) to the respective pin pair.

(5) A 1μF capacitor is required on this pin if it is using internal voltage reference output such as 1.5V, 2.0V or 2.5V.

6.7 RUN Mode Supply Current Into VCC Excluding External Current (1)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$I_{RUNH, Flash}$(2)	Supply current in Run mode, f_{HCLK}=48M	25°C		5.87		mA
		45°C		5.97		mA
		85°C		6.50		mA
		105°C		7.72		mA
	Supply current in Run mode, f_{HCLK}=96M	25°C		10.31		mA
		45°C		10.44		mA
		85°C		10.97		mA
		105°C		12.2		mA
	Supply current in Run mode, f_{HCLK}=120M	25°C		12.55		mA
		45°C		12.68		mA
		85°C		13.22		mA

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
		105°C		14.47		mA
	Supply current in Run mode, f_{HCLK}=156M	25°C	14	15.89	17	mA
		45°C		16.04		mA
		85°C		16.58		mA
		105°C		17.84		mA
$I_{RUNL, Flash}$(3)	Supply current in LP Run mode, f_{HCLK}=48M	25°C		5.45		mA
		45°C		5.53		mA
		85°C		5.98		mA
		105°C		7.04		mA
$I_{RUN, SRAM}$(4)	Supply current in Run mode, f_{HCLK}=156M	25°C		16.15		mA
		45°C		16.31		mA
		85°C		16.84		mA
		105°C		18.1		mA

(1) Guaranteed by characterization results.

(2) All inputs are tied to 0 V or to VDD. Outputs do not source or sink any current. Characterized with program executing typical data processing. VCORE running at high power mode, PLL is souring by fEHS =24MHz crystal, all peripherals disable.

(3) All inputs are tied to 0 V or to VDD. Outputs do not source or sink any current. Characterized with program executing typical data processing. VCORE running at low power mode, PLL is souring by fEHS =24MHz crystal, all peripherals disable.

(4) Same condtion as note (2), but program and data reside entirely in RAM. All execution is from RAM. No access to Flash.

6.8 RUN Mode Supply Current Per MHz (1) (2)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$I_{RUN, FLASH}$	Supply current in Run mode, f_{HCLK} = 156M	Coremark		17.31		mA
		Coremark		110.93		μA/MHz
		Pseudo-dhrystone		17.30		mA
		Pseudo-dhrystone		110.87		μA/MHz
$I_{RUN, SRAM}$ (3)	Supply current in Run mode, f_{HCLK} = 156M	Coremark		17.11		mA
		Coremark		110.93		μA/MHz
		Pseudo-dhrystone		16.8		mA
		Pseudo-dhrystone		107.66		μA/MHz

(1) Guaranteed by characterization results.

(2) All inputs are tied to 0 V or to VDD. Outputs do not source or sink any current. Characterized with program executing typical data processing. VCORE running at high power mode, PLL is souring by fEHS =24MHz crystal, all peripherals disable.

(3) Same condtion as note (1), but program and data reside entirely in RAM. All execution is from RAM. No access to Flash.

6.9 Sleep Mode Supply Current Into VCC Excluding External Current (1) (2) (3)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$I_{SLEEPH, Flash}$(2)	Supply current in Sleep mode, f_{HCLK} = 48M	25°C		3.80		mA
		45°C		3.88		mA
		85°C		4.30		mA
		105°C		5.33		mA
	Supply current in Sleep mode, f_{HCLK} = 96M	25°C		6.88		mA
		45°C		6.99		mA
		85°C		7.51		mA
		105°C		8.74		mA
	Supply current in Sleep mode, f_{HCLK} = 120M	25°C		8.26		mA
		45°C		8.38		mA
		85°C		8.89		mA
		105°C		10.12		mA
	Supply current in Sleep mode, f_{HCLK} = 156M	25°C	9	10.25	11	mA
		45°C		10.37		mA
		85°C		10.88		mA
		105°C		12.12		mA
$I_{SLEEPL, Flash}$(3)	Supply current in LP Sleep mode, f_{HCLK} = 48M	25°C		3.80		mA
		45°C		3.88		mA
		85°C		4.3		mA
		105°C		5.33		mA

(1) Guaranteed by characterization results.

(2) All inputs are tied to 0 V or to VDD. Outputs do not source or sink any current. Characterized with program executing typical data processing. VCORE running at high power mode, PLL is souring by fEHS =24MHz crystal, all peripherals disable.

(3) All inputs are tied to 0 V or to VDD. Outputs do not source or sink any current. Characterized with program executing typical data processing. VCORE running at low power mode, PLL is souring by fEHS =24MHz crystal, all peripherals disable.

6.10 STOP Mode Supply Current Into VCC Excluding External Current (1)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$I_{STOP, ELS}$(2) (3)	Supply current in STOP mode (backup registers retained, f_{RTC}= f_{ELS}, TPSensor enabled, Retention SRAM enabled, IWDG enabled) (3)	25°C		34.8		μA
	Supply current in STOP mode (backup registers retained, f_{RTC}= f_{ELS}, TPSensor disabled, Retention SRAM enabled, IWDG enabled) (3)	25°C		27.8		μA
$I_{STOP, ILS}$	Supply current in STOP mode (backup registers retained, f_{RTC}= f_{ILS}, TPSensor	25°C		34.6		μA

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
	enabled, Retention SRAM enabled, IWDG enabled) (3)					
	Supply current in STOP mode (backup registers retained, f_{RTC}= f_{ILS}, TPSensor disabled, Retention SRAM enabled, IWDG enabled) (3)	25°C		26.8		uA

(1) Guaranteed by characterization results.

(2) Characterized with a ECS-.327-12.5-34S-TR9 crystal with a load capacitance chosen to closely match the required load.

(3) 5Hz scan with single button wake up.

6.11 Standby1 Mode Supply Current Into VCC Excluding External Current (1)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$I_{STANDBY, ELS}$(2) (3)	Supply current in Standby mode (backup registers retained, f_{RTC}= f_{ELS}, TPSensor enabled, Retention SRAM enabled, IWDG enabled, f_{IWDG}=f_{ELS})	25°C		10.3		μA
	Supply current in Standby mode (backup registers retained, f_{RTC}= f_{ELS}, TPSensor disabled, Retention SRAM enabled, IWDG enabled, f_{IWDG}=f_{ELS})	25°C		3.0		μA
	Supply current in Standby mode (backup registers retained, f_{RTC}= f_{ELS}, TPSensor enabled, Retention SRAM disabled, IWDG enabled, f_{IWDG}=f_{ELS})	25°C		10.2		μA
$I_{STANDBY, ILS}$(3)	Supply current in Standby mode (backup registers retained, f_{RTC}= f_{ILS}, TPSensor enabled, Retention SRAM enabled, IWDG disabled)	25°C		11.0		μA
	Supply current in Standby mode (backup registers retained, f_{RTC}= f_{ILS}, TPSensor enabled, Retention SRAM enabled, IWDG enabled, f_{IWDG}=f_{ILS})	25°C		11.4		μA
	Supply current in Standby mode (backup registers retained, f_{RTC}= f_{ILS}, TPSensor disabled, Retention SRAM enabled, IWDG enabled, f_{IWDG}=f_{ILS})	25°C		2.5		μA
	Supply current in Standby mode (backup registers retained, f_{RTC}= f_{ILS}, TPSensor enabled, Retention SRAM disabled, IWDG enabled, f_{IWDG}=f_{ILS})	25°C		10.6		μA

(1) Guaranteed by characterization results.

(2) Characterized with a ECS-.327-12.5-34S-TR9 crystal with a load capacitance chosen to closely match the required load.

(3) 5Hz scan with single button wake up.

6.12 Standby2 Mode Supply Current Into VCC Excluding External Current (1)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$I_{STANDBY, ELS}$(2)	Supply current in Standby mode (backup registers retained, f_{RTC}= f_{ELS}, IWDG disabled, SVS enabled)	VDD= 2.4V to 3.6V, 25°C		2.606		uA
		VDD= 2.4V to 3.6V, 45°C		3.06		uA
		VDD= 2.4V to 3.6V, 85°C		7.76		uA
		VDD= 2.4V to 3.6V, 105°C		26.02		uA
	Supply current in Standby mode (backup registers retained, f_{RTC}= f_{ELS}, IWDG enabled f_{IWDG}=f_{ELS}, SVS enabled)	VDD= 2.4V to 3.6V, 25°C		2.62		uA
		VDD= 2.4V to 3.6V, 45°C		3.22		uA
		VDD= 2.4V to 3.6V, 85°C		7.72		uA
		VDD= 2.4V to 3.6V, 105°C		25.99		uA
	Supply current in Standby mode (backup registers retained, f_{RTC}= f_{ELS}, IWDG enabled f_{IWDG}=f_{ELS}, SVS disabled)	VDD= 2.4V to 3.6V, 25°C		2.57		uA
		VDD= 2.4V to 3.6V, 45°C		3.17		uA
		VDD= 2.4V to 3.6V, 85°C		7.67		uA
		VDD= 2.4V to 3.6V, 105°C		25.91		uA
$I_{STANDBY, ILS}$	Supply current in Standby mode (backup registers retained, f_{RTC}= f_{ILS}, IWDG disabled, SVS disabled)	VDD= 2.4V to 3.6V, 25°C		2.58		uA
		VDD= 2.4V to 3.6V, 45°C		2.97		uA
		VDD= 2.4V to 3.6V, 85°C		7.67		uA
		VDD= 2.4V to 3.6V, 105°C		25.89		uA
	Supply current in Standby mode (backup registers retained, f_{RTC}= f_{ILS}, IWDG enabled f_{IWDG}=f_{ILS}, SVS enabled)	VDD= 2.4V to 3.6V, 25°C		2.66		uA
		VDD= 2.4V to 3.6V, 45°C		3.15		uA
		VDD= 2.4V to 3.6V, 85°C		7.74		uA
		VDD= 2.4V to 3.6V, 105°C		26.01		uA
	Supply current in Standby mode (backup registers retained, f_{RTC}= f_{ILS}, IWDG enabled f_{IWDG}=f_{ILS}, SVS disabled)	VDD= 2.4V to 3.6V, 25°C		2.59		uA
		VDD= 2.4V to 3.6V, 45°C		3.08		uA
		VDD= 2.4V to 3.6V, 85°C		7.69		uA
		VDD= 2.4V to 3.6V, 105°C		25.96		uA

(1) Guaranteed by characterization results.

(2) Characterized with a ECS-.327-12.5-34S-TR9 crystal with a load capacitance chosen to closely match the required load.

6.13 Shutdown Mode Supply Current Into VCC Excluding External Current (1)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$I_{SHUTDOWN, ELS}$(2)	Supply current in Shutdown mode (backup registers retained, f_{RTC}= f_{ELS}, IWDG disabled, SVS disabled)	25°C		2.6		uA
		45°C		3.02		uA
		85°C		7.69		uA
		105°C		25.9		uA

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
	Supply current in Shutdown mode (backup registers retained,RTC disabled, IWDG disabled, SVS disabled)	25°C		2.37		uA
		45°C		2.84		uA
		85°C		7.53		uA
		105°C		25.8		uA
$I_{SHUTDOWN, ILS}$	Supply current in Shutdown mode (backup registers retained, f_{RTC}= f_{ILS}, IWDG disabled, SVS disabled)	25°C		2.55		uA
		45°C		3.03		uA
		85°C		7.72		uA
		105°C		25.99		uA
	Supply current in Shutdown mode (backup registers retained,RTC disabled, IWDG disabled, SVS disabled)	25°C		2.37		uA
		45°C		2.83		uA
		85°C		7.53		uA
		105°C		25.8		uA

(1) Guaranteed by characterization results.

(2) Characterized with a ECS-.327-12.5-34S-TR9 crystal with a load capacitance chosen to closely match the required load.

6.14 Battery replacement Mode Supply Current Into VCC Excluding External Current (1)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$I_{BATREPLACE, ELS}$(2)	Supply current in Battery replacement mode (RTC enabled f_{RTC}= f_{ELS}, IWDG disabled, SVS disabled)	25°C		810		nA
		45°C		1170		nA
$I_{BATREPLACE, ILS}$	Supply current in Battery replacement mode (RTC enabled f_{RTC}= f_{ILS}, IWDG disabled, SVS disabled)	25°C		810		nA
		45°C		1170		nA

(1) Guaranteed by characterization results.

(2) Characterized with a ECS-.327-12.5-34S-TR9 crystal with a load capacitance chosen to closely match the required load.

6.15 External Low-speed Clock (1) (2) (3)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
f_{ELS}	External low-speed crystal	ELSBYP=0		32768		Hz
D_{CELS}	ELS duty cycle, measured at LSCO	ELSBYP=0	30		70	%
V_{ELSL}(4)	OSC_IN input pin low level voltage	ELSBYP=1	V_{SS}	-	0.3 x V_{DD}	V
V_{ELSH}(4)	OSC_IN input pin high level voltage	ELSBYP=1	0.7 x V_{DD}		V_{DD}	V

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
DC_{ELS}	OSC IN input signal duty cycle		30		70	%
OA_{ELS}	Oscillator allowance for ELS crystal C_L=12.5pF			200		kΩ
C_P(5)	Integrated effective load capacitance			2		pF
t_{ELS}	Start-up time	time between enable to ready signal			2.150	s
I_{DD}	ELS current consumption	ELSCTRL[11:4]=0xF		558		nA
		ELSCTRL[11:4]=0x0		243		nA

(1) To improve EMI on the ELS oscillator, observe the following guidelines.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) Refer to CRY-ECX-34Q-3P3X1P6 for details on crystal part numbers.

(3) Data based on characterization results, not tested in production.

(4) When ELSBYP is set, ELS circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger inputs section of this data sheet. Duty cycle requirements are defined by DCELS.

(5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).

6.16 External High-speed Clock (EHS) (1) (2) (3)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
f_{EHS}	External high-speed crystal	EHSBYP=0	4		32	MHz
D_{CEHS}	EHS duty cycle, measured at MCO	EHSBYP=0	45		55	%
V_{EHSL}	OSC_IN input pin low level voltage	EHSBYP=1	V_{SS}	-	0.3 x V_{DD}	V
V_{EHSH}	OSC_IN input pin high level voltage	EHSBYP=1	0.7 x V_{DD}		V_{DD}	V
D_{CEHS}	OSC IN input signal duty cycle	EHSBYP=1	45		55	%
O_{AEHS}	Oscillator allowance for EHS crystal,C_L=10pf, EHS=24MHz	EHSCTL[5:0]=11		60		Ω
	Oscillator allowance for EHS crystal,C_L=10pf, EHS=32MHz	EHSCTL[5:0]=27		60		Ω
C_P(4)	Integrated effective load capacitance			2		pF

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
t_{EHS}(5)	Start-up time	f_{EHS} =4MHz, 24MHz, High drive(EHSCTL[5:0]=0x28), C_L =10pF			3.2	μs
		f_{EHS} =32MHz, High drive(EHSCTL[5:0]=0x3F), C_L =10pF			1.9	μs
I_{DD}	EHS current consumption	f_{EHS} =4MHz, 24MHz, High drive(EHSCTL[5:0]=0x28), C_L =10pF		950		μA
		f_{EHS} =4MHz, 24MHz, Normal drive(EHSCTL[5:0]=0xB), C_L =10pF		350		μA
		f_{EHS} =32MHz, High drive(EHSCTL[5:0]=0x3F), C_L =10pF		1488		μA
		f_{EHS} =32MHz, Normal drive(EHSCTL[5:0]=0x1B), C_L =10pF		716		μA

(1) Data based on characterization results, not tested in production.

(2) To improve EMI on the HFXT oscillator, observe the following guidelines.

- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(3) The 24-MHz crystal used for lab characterization is the CRY-ABM8X-3P2X2P5X0P6

(4) Includes parasitic bond and package capacitance (approximately 2 pF per pin).

(5) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. Recommended values supported are 14 pF, 16 pF, and 18 pF. The maximum shunt capacitance is 7 pF.

6.17 Internal Low-speed Clock (ILS) (1)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
f_{ILS}	Internal low-speed oscillator (calibrated)	Measured at LSCO		32768		Hz
	ILS absolute calibrated tolerance	T_A= 25C	-3		3	%
D_{CILS}	ILS duty cycle		45		55	%
t_{ILS}	Start-up time	Time between enable to ready signal		60		μs
I_{DD}	ILS current consumption			276		nA

(1) Data based on characterization results.

6.18 Internal High-speed Clock (IHS)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
f_{IHS}	Internal high-speed oscillator (calibrated)			8		MHz
	IHS absolute calibrated tolerance	V_{DD}= 3.0V, T_A=25℃ (1)	-1		1	%
		V_{DD} =3.0V, T_A= -40℃ to 105℃	-1.5		1.5	%
		V_{DD} = 2.2V to 3.6V, T_A= -40℃ to 105℃ (1)	-2.5		2.5	%
D_{CIHS}(2)	IHS duty cycle		45		55	%
t_{IHS}(2)	Start-up time	Time between enable to ready signal		4		μs
I_{DD}(2)	IHS current consumption			118		μA

(1) Guaranteed by test in production.
(2) Guaranteed by characterization results.

6.19 PLL Characteristics (1)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
f_{PLL_IN}	PLL input clock		4		32	MHz
DC_{PLL}	PLL input clock duty cycle		45		55	%
f_{PLL_OUT}	PLL multiplier output clock P	VCO=312MHz,ODIV=2			156	MHz
	PLL multiplier output clock Q	VCO=180Mhz, ADC48M Divider=4,			45	MHz
t_{LOCK}	PLL lock time	EHS=24Mhz,INDIV=2, FBDIV=26 VCO=312		261		μs
		IHS=8MHz, INDIV=1, FBDIV=39		390		μs
J_{itter}	RMS cycle-to-cycle jitter			7.5		ps
I_{DD}	PLL current consumption	f_{PLL_OUT} =156MHz		320		uA
		f_{PLL_OUT} =120MHz		280		uA
		f_{PLL_OUT} =96MHz		250		uA

(1) Guaranteed by characterization.

6.20 ADC Characteristics (1)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
V_{ADC}	ADC supply voltage		1.71		3.6	V
V_{ax}	Analog input voltage range		0		V_{DDA}	V
f_S	Sample rate				2.5	MSPS
V_{REF+}	V_{REF+}	External reference	2.4		V_{DDA}	V
V_{REF-}	V_{REF-}	External reference		V_{SSA}		V

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
C_P	Parasitic input capacitance			2		pF
R_{ON}	Sampling switch resistance			500		Ω
C_h	Sampling capacitor			5		pF
R_S	Nominal source impedance			50		Ω
f_{STAB}	Power-up time			1.0		μs
$T_{temperature}$	Internal temperature sensor		-2		2	℃

(1) Guaranteed by design.

6.21 ADC Characteristics (1)

Symbol	Parameter	Conditions		MIN	TYP	MAX	UNIT
f_{ADC}	ADC clock frequency			1		45	MHz
I_{DD}	ADC consumption from the V_{DDA} supply	f_S= 1Msps			371		μA
		f_S= 2.5Msps			855		μA
E_T	Total unadjusted error	Internal reference	Single end, V_{DDA}=2.4V~3.6V, sampling rate =1Msps	-1.8		1.8	%
		Internal reference	Single end, V_{DDA}<2.4V, sampling rate =1Msps	-1.6		1.6	%
		Internal reference	Single end, V_{DDA}=2.4V~3.6V, sampling rate =2.5Msps	-1.8		1.8	%
		Internal reference	Differential end, V_{DDA}=2.4V~3.6V, sampling rate =1Msps	-1		1	%
		Internal reference	Differential end, V_{DDA}<2.4V, sampling rate =1Msps	-0.9		0.9	%
		Internal reference	Differential end, V_{DDA}=2.4V~3.6V, sampling rate =1Msps	-1		1	%
		External reference	Single end, V_{DDA}=2.4V~3.6V, sampling rate =1Msps	-6		6	LSB
		External reference	Single end, V_{DDA}<2.4V, sampling rate =1Msps	-6		6	LSB

Symbol	Parameter	Conditions		MIN	TYP	MAX	UNIT
		External reference	Single end, V_{DDA}=2.4V~3.6V, sampling rate =2.5Msps	-6		6	LSB
		External reference	Differential end, V_{DDA}=2.4V~3.6V, sampling rate =1Msps	-5		5	LSB
		External reference	Differential end, VDDA<2.4V, sampling rate =1Msps	-5		5	LSB
		External reference	Differential end, VDDA=2.4V~3.6V, sampling rate =2.5Msps	-5		5	LSB
E_O	Offset error (Internal reference)	Internal reference	Single end, VDDA=2.4V~3.6V, sampling rate =1Msps	-3		3	LSB
		Internal reference	Single end, VDDA<2.4V, sampling rate =1Msps	-3		3	LSB
		Internal reference	Single end, VDDA=2.4V~3.6V, sampling rate =2.5Msps	-3		3	LSB
		Internal reference	Differential end, VDDA=2.4V~3.6V, sampling rate =1Msps	-2		2	LSB
		Internal reference	Differential end, VDDA<2.4V, sampling rate =1Msps	-2		2	LSB
		Internal reference	Differential end, VDDA=2.4V~3.6V, sampling rate =2.5Msps	-2		2	LSB
	Offset error (External reference)	External reference	Single end, VDDA=2.4V~3.6V, sampling rate =1Msps	-4		4	LSB
		External reference	Single end, VDDA<2.4V, sampling rate =1Msps	-6		6	LSB
		External reference	Single end, VDDA=2.4V~3.6V, sampling rate =2.5Msps	-4		4	LSB
		External reference	Differential end, VDDA=2.4V~3.6V, sampling rate =1Msps	-2		2	LSB
		External reference	Differential end, VDDA<2.4V, sampling rate =1Msps	-2		2	LSB

Symbol	Parameter	Conditions		MIN	TYP	MAX	UNIT
		External reference	Differential end, VDDA=2.4V~3.6V, sampling rate =2.5Msps	-3		3	LSB
E_G	Gain error (Internal reference)	Internal reference	Single end, VDDA=2.4V~3.6V, sampling rate =1Msps	-5		5	LSB
		Internal reference	Single end, VDDA<2.4V, sampling rate =1Msps	-5		5	LSB
		Internal reference	Single end, VDDA=2.4V~3.6V, sampling rate =2.5Msps	-5		5	LSB
		Internal reference	Differential end, V_{DDA}=2.4V~3.6V,Sampling rate = 1Msps	-3		3	LSB
		Internal reference	Differential end, VDDA<2.4V, sampling rate =1Msps	-3		3	LSB
		Internal reference	Differential end, VDDA=2.4V~3.6V, sampling rate =2.5Msps	-3		3	LSB
	Gain error (External reference)	External reference	Single end, V_{DDA}=2.4V~3.6V,Sampling rate = 1Msps	-6		6	LSB
		External reference	Single end, VDDA<2.4V, sampling rate =1Msps	-6		6	LSB
		External reference	Single end, VDDA=2.4V~3.6V, sampling rate =2.5Msps	-8		8	LSB
		External reference	Differential end, V_{DDA}=2.4V~3.6V,Sampling rate = 1Msps	-6		6	LSB
		External reference	Differential end, VDDA<2.4V, sampling rate =1Msps	-6		6	LSB
		External reference	Differential end, VDDA=2.4V~3.6V, sampling rate =2.5Msps	-8		8	LSB
DNL	Differential nonlinearity	Internal reference	Single end, V_{DDA}=2.4V~3.6V,Sampling rate = 1Msps	-1.5		1.5	LSB
		Internal reference	Single end, VDDA<2.4V, sampling rate =1Msps	-1.5		1.5	LSB
		Internal reference	Single end, VDDA=2.4V~3.6V, sampling rate =2.5Msps	-1.5		1.5	LSB

Symbol	Parameter	Conditions		MIN	TYP	MAX	UNIT
		Internal reference	Differential end, VDDA=2.4V~3.6V, sampling rate =2.5Msps	-1		1	LSB
		Internal reference	Differential end, VDDA<2.4V, sampling rate =1Msps	-1		1	LSB
		Internal reference	Differential end, VDDA=2.4V~3.6V, sampling rate =2.5Msps	-1		1	LSB
		External reference	Single end, V_{DDA}=2.4V~3.6V,Sampling rate = 1Msps	-1		1.5	LSB
		External reference	Single end, VDDA<2.4V, sampling rate =1Msps	-1		2.0	LSB
		External reference	Single end, VDDA=2.4V~3.6V, sampling rate =2.5Msps	-1		1.8	LSB
		External reference	Differential end, V_{DDA}=2.4V~3.6V,Sampling rate = 1Msps	-1		1	LSB
		External reference	Differential end, VDDA<2.4V, sampling rate =1Msps	-1		1.2	LSB
		External reference	Differential end, VDDA=2.4V~3.6V, sampling rate =2.5Msps	-1		1.2	LSB
INL	Integral nonlinearity	Internal reference	Single end, V_{DDA}=2.4V~3.6V,Sampling rate = 1Msps	-2		2	LSB
		Internal reference	Single end, VDDA=2.4V~3.6V, sampling rate =2.5Msps	-2		2	LSB
		Internal reference	Single end, VDDA<2.4V, sampling rate =1Msps	-2		2	LSB
		Internal reference	Differential end, V_{DDA}=2.4V~3.6V,Sampling rate = 1Msps	-2		2	LSB
		Internal reference	Differential end, VDDA<2.4V, sampling rate =1Msps	-2		2	LSB
		Internal reference	Differential end, VDDA=2.4V~3.6V, sampling rate =2.5Msps	-2		2	LSB

Symbol	Parameter	Conditions		MIN	TYP	MAX	UNIT
		External reference	Single end, V_{DDA}=2.4V~3.6V,Sampling rate = 1Msps	-1.8		1.8	LSB
		External reference	Single end, VDDA<2.4V, sampling rate =1Msps	-2.2		2.2	LSB
		External reference	Single end, VDDA=2.4V~3.6V, sampling rate =2.5Msps	-2.4		2.4	LSB
		External reference	Differential end, V_{DDA}=2.4V~3.6V,Sampling rate = 1Msps	-1.5		1.5	LSB
		External reference	Differential end, VDDA<2.4V, sampling rate =1Msps	-1.5		1.5	LSB
		External reference	Differential end, VDDA=2.4V~3.6V, sampling rate =2.5Msps	-2		2	LSB
ENOB(1)	Effective Numbers of Bits	Internal reference	Single end, V_{DDA}=1.71V~3.6V, sampling rate =1Msps/ 2.5Msps	10	10.8		LSB
		Internal reference	Differential end, V_{DDA}=1.71V~3.6V, sampling rate =1Msps/ 2.5Msps	11.2	11.4		LSB
		External reference	Single end, V_{DDA}=1.71V~3.6V, sampling rate =1Msps/ 2.5Msps	10.5	11		LSB
		External reference	Differential end, V_{DDA}=1.71V~3.6V, sampling rate =1Msps/ 2.5Msps	11.2	11.5		LSB
SINAD(1)	Signal-to-(Noise and Distortion) ratio	Internal reference	Single end, V_{DDA}=1.71V~3.6V, sampling rate =1Msps/ 2.5Msps	62	66.3		dB
		Internal reference	Differential end, V_{DDA}=1.71V~3.6V, sampling rate =1Msps/ 2.5Msps	69	71		dB
		External reference	Single end, V_{DDA}=1.71V~3.6V, sampling rate =1Msps/ 2.5Msps	65	67.9		dB

Symbol	Parameter	Conditions		MIN	TYP	MAX	UNIT
		External reference	Differential end, V_{DDA}=1.71V~3.6V, sampling rate =1Msps/ 2.5Msps	69	71.2		dB
SNR(1)	Signal-to-Noise ratio	Internal reference	Single end, V_{DDA}=1.71V~3.6V, sampling rate =1Msps/ 2.5Msps	62	66.6		dB
		Internal reference	Differential end, V_{DDA}=1.71V~3.6V, sampling rate =1Msps/ 2.5Msps	69	71.2		dB
		External reference	Single end, V_{DDA}=1.71V~3.6V, sampling rate =1Msps/ 2.5Msps	66	68.1		dB
		External reference	Differential end, V_{DDA}=1.71V~3.6V, sampling rate =1Msps/ 2.5Msps	69	71.5		dB
THD(1)	Total harmonic distortion	Internal reference	Single end, V_{DDA}=1.71V~3.6V, sampling rate =1Msps/ 2.5Msps		-80.1	-70	dB
		Internal reference	Differential end, V_{DDA}=1.71V~3.6V, sampling rate =1Msps/ 2.5Msps		-84.7	-78	dB
		External reference	Single end, V_{DDA}=1.71V~3.6V, sampling rate =1Msps/ 2.5Msps		-81.6	-68	dB
		External reference	Differential end, V_{DDA}=1.71V~3.6V, sampling rate =1Msps/ 2.5Msps		-85	-79	dB

(1) Guaranteed by characterization results.

6.22 DAC Characteristics

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
V_{DDA}	Operation voltage		1.71		3.6	V
C_L	Capacitive load				50	pF
t_{SU}(1)	Settling time	Full scale, C_L = 50 pF, R_L ≥5 kΩ , ±1 LSB		2.2		us

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
I_{DD}(1)	DAC consumption from V_{DDA}	DAC output buffer on, no load, middle code (0x800)		272		uA
SNR(1)	Signal-to-noise ratio	DAC output buffer ON C_L ≤ 50 pF, R_L ≥ 5 kΩ, Fout 1 kHz, BW 500 kHz, External reference		63		dB
THD(1)	Total harmonic distortion	DAC output buffer ON C_L ≤ 50 pF, R_L ≥ 5 kΩ, Fout 1 kHz, External reference		-71		dB
V_{OUT}	DAC output voltage range	CL = 50 pF, R_L ≥5 kΩ, code =0x0(1)	0.0		0.01	V
		C_L = 50 pF, R_L ≥5 kΩ, code= 0x0FFF(2)	V_{DDA}-0.1		V_{DDA}	V
INL	Integral nonlinearity	External reference, V_{REF+}=V_{DDA}(2)	-6		6	LSB
		Internal reference(1)	-10		10	LSB
DNL	Differential nonlinearity	External reference, V_{DDA}≥3.0V, V_{REF+}=V_{DDA}(2)	-1		1	LSB
		External reference, V_{DDA}<3.0V, V_{REF+}=V_{DDA}(2)	-1		1.3	LSB
		Internal reference(1)	-10		10	LSB
E_G(1)	Gain error	External reference, V_{REF+}=V_{DDA}	-0.5		0.5	%
		Internal reference	-0.5		0.5	%
E_O(1)	Offset error after calibration	External reference, V_{REF+}=V_{DDA}	-6		6.0	mV
		Internal reference	-8		8	mV

(1) Guaranteed by characterization results.
(2) Guaranteed by test in production.

6.23 VREFBUF Characteristics

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
V_{REFBUF_OUT} (2)	V_{REFBUF} voltage output	V_{RS} = 00, V_{DDA}=1.71V~3.6V	1.455	1.5	1.545	V
		V_{RS} = 01, V_{DDA}=2.25V~3.6V	1.94	2	2.06	V
		V_{RS} = 10, V_{DDA}=2.75V~3.6V	2.425	2.5	2.575	V
		V_{RS} = 00, I_{load}=5mA, V_{DDA}=1.75V~3.6V	1.455	1.5	1.545	V
		V_{RS} = 01, I_{load}=5mA, V_{DDA}=2.25V~3.6V	1.94	2	2.06	V
		V_{RS} = 10, I_{load}=5mA, V_{DDA}=2.75V~3.6V	2.425	2.5	2.575	V
t_{SU} (2)	Start up time	C_L=1uF		150		us
C_L (1)	Load capacitor		0.5	1	1.5	μF
PSRR	Power supply rejection	DC(3)		55		dB
		V_{RS} = 10, f=100kHz, R_L=5kohm, V_{DDA}=2.75V~3.0V(2)		31		dB
I_{LOAD} (3)	Static load current				5	mA

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
I_q (3)	Quiescent current	V_{RS} = 10, I_{load}=5mA, V_{DDA}=3.0V		47		uA

(1) Guaranteed by design.

(2) Guaranteed by test in production.

(3) Guaranteed by characterization results.

6.24 OA Characteristics

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
V_{DDA}	OA operation voltage		1.71		3.6	V
V_{OS}(4)	Input offset voltage	Buffer mode, V_{CM}=0.1V_{DDA} to 0.9V_{DDA}	-8		8	mV
V_{CM}(2)	Input voltage range		0.1V_{DDA}		0.9V_{DDA}	
CMRR(4)	Common-mode rejection ratio	V_{CM}=0.1V_{DDA}, 0.5V_{DDA} and 0.9V_{DDA}		56		dB
PSRR(3)	Power supply rejection ratio	Buffer mode,V_{CM}=0.1V_{DDA}, 0.5V_{DDA} and 0.9V_{DDA}		70		dB
GE(1)(3)	Gain error at non-inverting mode	Gain≤9, 100mV ≤ Output dynamic range ≤ V_{DDA}- 100mV		±0.5		%
		Gain=17/26/33, 500mV ≤ Output dynamic range ≤ V_{DDA}- 500mV		±0.5		%
		Gain=65, 1000mV ≤ Output dynamic range ≤ V_{DDA}- 500mV		±0.5		%
	Gain error at inverting mode	Gain≤16, 100mV ≤ Output dynamic range ≤ V_{DDA}- 100mV		±1		%
		Gain=25/32, 500mV ≤ Output dynamic range ≤ V_{DDA}- 500mV		±1		%
		Gain=64, 1000mV ≤ Output dynamic range ≤ V_{DDA}- 500mV		±1		%
V_{out}(3)	Voltage output swing from supply rails	OA work as follower mode, I_{load}=500uA		50	100	mV
t_{SU}(2)	Startup time	V_{OUT} from 0 to 1V, C_L = 50 pF		1		μs
I_{DD}(3)	OA consumption from V_{DDA}			860		μA
SR(3)	Positive slew rate	C_L = 50 pF, V_{IN} = V_{DDA}/2		8		V/μs
C_L(2)	Capacitive load				50	pF
G_{BW}(3)	Gain bandwidth	GP mode, close loop gain=10x, 100mV ≤ Output dynamic range ≤ V_{DDA} - 100mV		19.0		MHz
φ_M(3)	Phase margin	Buffer mode, C_L = 50 pF, R_L = 2 kΩ, V_{CM} =V_{DDA}/2		46.0		deg
THD(3)	Total harmonic distortion	Buffer mode, C_L = 50 pF, R_L = 2 kΩ, V_{CM} =V_{DDA}/2, f_{IN}=1Khz, V_{PP}=800mV		-45.0		dB

(1) Gain error = ΔVout/ΔVin.

(2) Guaranteed by design.

(3) Guaranteed by characterization results.

(4) Guaranteed by test in production.

6.25 CMP Characteristics

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
V_{DDA}	Operation voltage		1.71		3.6	V
V_{IN}	Comparator input voltage		0		V_{DDA}	V
R_{IN}	Input channel series resistance (1) (2)				5	kΩ
$V_{OS,RUN}$(3)	Input offset voltage at run mode		-10		10	mV
$V_{OS,STOP}$(3)	Input offset voltage at stop mode		-10		10	mV
$V_{HYST,RUN}$(3)	Comparator input hysteresis at run mode	HYST=001, V_{IN}=1/2V_{DDA}		5	9.8	mV
		HYST=010, V_{IN}=1/2V_{DDA}		10	14.5	mV
		HYST=011, V_{IN}==1/2V_{DDA}		15	20.5	mV
		HYST=100, V $_{IN}$=1/2V_{DDA}		20	29.8	mV
		HYST=101, V_{IN}=1/2V_{DDA}		25	38.1	mV
		HYST=110, V_{IN}=1/2V_{DDA}		30	48.8	mV
$V_{HYST,STOP}$(3)	Comparator input hysteresis at stop mode	HYST=001, V_{IN}=1/2V_{DDA}		5	9.8	mV
		HYST=010, V_{IN}=1/2V_{DDA}		10	14.5	mV
		HYST=011, V_{IN}=1/2V_{DDA}		15	20.5	mV
		HYST=100, V_{IN}=1/2V_{DDA}		20	29.8	mV
		HYST=101, V_{IN}=1/2V_{DDA}		25	38.1	mV
		HYST=110, V_{IN}=1/2V_{DDA}		30	48.8	mV
$t_{D,RUN}$(3)	Propagation delay, response time at run mode	|V_{INP}-V_{INN}| =200mV		330		ns
$t_{D,STOP}$(3)	Propagation delay, response time at stop mode	|V_{INP}-V_{INN}| =200mV		375		ns
t_{SU}(3)	Comparator start up time				5	us
I_{DD}(3)	Comparator consumption from V_{DDA}, DAC6 is disabled			12.5		uA
t_{SUD}(3)	Settling to 1LSB after full-scale output change				1	us
DNL(3)	Integrated 6-bit DAC static DNL		-1		1	LSB
INL(3)	Integrated 6-bit DAC static INL		-1		1	LSB

(1) Guaranteed by Design.

(2) Test result includes additional resistance of whole analog test path.

(3) Guaranteed by characterization results.

6.26 TPSensor® Characteristics (1)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
V_{DDA}	TPSensor® operation voltage		1.71		3.6	V
$C_{ELECTRODE}$	Maximum capacitance of all external electrodes				200	pF
C_{DETECT}	Detected accuracy range			5	10	pF
f_{CAPCLK}	TPSensor® oscillator frequency(calibrated)		9.2	10	10.8	MHz
SNR	Ratio of counts of finger to noise		5.0			ratio

(1) Guaranteed by Design.

6.27 Power on Sequencing

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
V_{POR+}(1)	Power-up level	Active mode			1.71	V
V_{POR-}(2)	Power-down level	Active mode	1.458			V
		Low power	1.44			V
$V_{PORHYST}$(2)	POR hysteresis			100		mV
V_{SVS1}	Rising edge(2)			2.05		V
	Falling edge(1)			1.95		V
V_{SVS2}	Rising edge(2)			2.25		V
	Falling edge(1)			2.15		V
$V_{SVSHYST}$(2)	SVS hysteresis			115		mV
I_{SVS}(3)	SVS consumption from V_{DDA}	Active mode		5		μA
		Low power mode		60		nA

(1) Guranteed by test in production

(2) Guaranteed by characterization results

(3) Guaranteed by design.

6.28 Wakeup Time from Low-power Modes and Reset (1) (2)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$T_{WUSLEEPH}$	Wakeup time from High power Sleep mode to Run mode			7	12	Nb of CPU cycles
$T_{WUSLEEPL}$	Wakeup time from Low power Sleep mode to Run mode			7	12	Nb of CPU cycles
T_{WUSTOP}	Wakeup time from Stop mode to Run mode			30	50	μs
$T_{WUSTANDBY1}$	Wakeup time from Standby1 mode to Run mode			90	122	μs
$T_{WUSTANDBY2}$	Wakeup time from Standby2 mode to Run mode			100	130	

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$T_{WUSHUTDOWN}$	Wakeup time from Shutdown mode to Run mode			100	130	
T_{WURST}	Wakeup time from RST to Run mode			100		μs
T_{WUPO}	Power on time			1.0		ms

(1) $T_{WUSLEEPH}$ and $T_{WUSLEEPL}$ are guaranteed by design, others are guaranteed by characterization results.

(2) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.

6.29 NRST Pin Characteristics (1) (2)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
V_{IL_NRST}(1)	NRST input low level voltage				0.3 x VDD	V
V_{IH_NRST}(1)	NRST input high level voltage		0.7 x VDD			V
V_{NRST_HYST}	NRST Schmitt trigger voltage hysteresis			200		mV
R_{NRST}(1)(2)	Weak pull-up equivalent resistor		25	40	55	kΩ
V_{NRST_FILT}	NRST input filtered pulse				70	ns
V_{NRST_NFILT}	NRST input not filtered pulse		350			ns
f_{HOLD_RST}(1)	Reset low pulse length to be hold		20			us

(1) Guaranteed by design.

(2) The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

6.30 IO_WKUP (1)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
t_{SP_WKUP}	The pulse width of the glitch that the input filter must suppress				20	ns
	The pulse width to wake up		350			ns

(1) Guaranteed by characterization results.

6.31 GPIO Input Output Characteristics

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
V_{IL}(1) (6)	GPIO input low level voltage				0.3 x V_{DD}	V
V_{IH}(1) (6)	GPIO input high level voltage		0.7 x V_{DD}			V
V_{IO_HYST}(1)	GPIO Schmitt trigger voltage hysteresis			200		mV
$R_{PULL\ UP}$(2) (6)	Pull up resistor	For pullup: V_{IN} = V_{SS},	20.0	40	55	kΩ
$R_{PULL\ DOWN}$(2) (6)	Pull down resistor (except NRST)	For pulldown: V_{IN} = V_{DD}	20.0	40	55	kΩ
C_{IO}(2)	GPIO pin capacitance			5		pF

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
I_{IO_IDD} (1)(7)	High-impedance leakage current except FTC			70		nA
	High-impedance leakage current for FTC			32		uA
	Push-Pull leakage current except FTA, FTC			3.5		uA
	Push-Pull leakage current for FTA			126		uA
	Push-Pull leakage current for FTC			64		nA
I_{IL}(6)	Input Low leakage current, T_A=25℃		-30		30	nA
I_{IH}(6)	Input High leakage current, T_A=25℃		-30		30	nA
V_{OL}(2) (5) (6)	Low-level output voltage except FTC,HD	V_{DD} ≥ 2.7V, IMAX = 20mA			0.4	V
		V_{DD} < 2.7V, IMAX = 10mA			0.4	V
	Low-level output voltage except FTC	V_{DD} ≥ 2.7V, IMAX = 10mA			0.4	V
		V_{DD} < 2.7V, IMAX = 5mA			0.4	V
	Low-level output voltage for FTC,HD	V_{DD} < 2.7V, IMAX = 10mA			0.4	V
		V_{DD} ≥ 2.7V, IMAX = 20mA			0.4	V
	Low-level output voltage for FTC	V_{DD} ≥ 2.7V, IMAX = 10mA			0.4	V
		V_{DD} < 2.7V, IMAX = 5mA			0.4	V
V_{OH}(2) (5) (6)	High-level output voltage except FTC,HD	V_{DD} ≥ 2.7V, IMAX = -20mA	V_{DD}-0.4			V
		V_{DD} < 2.7V, IMAX = -10mA	V_{DD}-0.4			V
	High-level output voltage except FTC	V_{DD} ≥ 2.7V, IMAX = -10mA	V_{DD}-0.4			V
		V_{DD} < 2.7V, IMAX = -5mA	V_{DD}-0.4			V
	High-level output voltage for FTC (4)	V_{DD} ≥ 2.7V, IMAX = -5mA	V_{DD}-0.4			V
		V_{DD} < 2.7V, IMAX = -2.5mA	V_{DD}-0.4			V

(1) Guaranteed by characterization results.

(2) Guaranteed by design.

(3) This value represents the pad leakage of the I/O itself, The leakage current is measured with V_{SS} or V_{DD} applied to the corresponding pins, unless otherwise noted. The port pin is selected for input and the pullup or pulldown resistor is disabled.

(4) These pins can be configured to opendrain mode after power on, meanwhile it can support high drive of 20mA

(5) The maximum total current, I_{MAX} of high and low level output, for all outputs combined should not exceed ±150 mA to hold the maximum voltage drop specified.

(6) Guaranteed by test in production.

6.32 GPIO AC Characteristics (1) (4)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
f_{IO_00}	Clock frequency except FTC, OSPEEDx = 00	V_{DD} ≥2.7V,C_L = 20pF			24	MHz
		V_{DD} < 2.7V,C_L = 20pF			12	MHz
f_{R_00}	Output rise time except FTC, OSPEEDx = 00	V_{DD} ≥2.7V,C_L = 20pF			6	ns
		V_{DD} < 2.7V,C_L = 20pF			12	ns
f_{F_00}	Output fall time except FTC, OSPEEDx = 00	V_{DD} ≥ 2.7V,C_L = 20pF			6	ns
		V_{DD} < 2.7V,C_L = 20pF			12	ns
f_{IO_11}	Clock frequency except FTC, OSPEEDx = 11	V_{DD} ≥2.7V,C_L = 20pF			120	MHz
		V_{DD} < 2.7V,C_L = 20pF			60	MHz
f_{R_11}	Output rise time except FTC, OSPEEDx = 11	V_{DD} ≥ 2.7V,C_L = 20pF			2	ns
		V_{DD} < 2.7V,C_L = 20pF			4	ns
f_{F_11}	Output fall time except FTC, OSPEEDx = 11	V_{DD} ≥ 2.7V,C_L = 20pF			2	ns
		V_{DD} < 2.7V,C_L = 20pF			4	ns
f_{IO_FTC}	Clock frequency for FTC, OSPEEDx= 00	V_{DD} ≥ 2.7V,C_L = 20pF			24	MHz
		V_{DD} < 2.7V,C_L = 20pF			12	MHz
f_{R_FTC}	Output rise time for FTC, OSPEEDx = 00	V_{DD} ≥ 2.7V,C_L = 20pF			6	ns
		V_{DD} < 2.7V,C_L = 20pF			12	ns
f_{F_FTC}	Output fall time for FTC, OSPEEDx = 00	V_{DD} >=2.7V,C_L = 20pF			6	ns
		V_{DD} < 2.7V,C_L = 20pF			12	ns
f_{IO_FTC}	Clock frequency for FTC, OSPEEDx = 11	V_{DD} ≥ 2.7V,C_L = 20pF			48	MHz
		V_{DD} < 2.7V,C_L = 20pF			24	MHz
f_{R_FTC}	Output rise time for FTC, OSPEEDx = 11	V_{DD} ≥ 2.7V,C_L = 20pF			4.5	ns
		V_{DD} < 2.7V,C_L = 20pF			9	ns
f_{F_FTC}	Output fall time for FTC, OSPEEDx = 11	V_{DD} ≥ 2.7V,C_L = 20pF			4.5	ns
		V_{DD} < 2.7V,C_L = 20pF			9	ns
f_{IO_FM+} (2)	Clock frequency for FM+	C_L = 50pF,external pull up resistance = 1kohm			1	MHz
f_{F_FM+} (2)	Output fall time for FM+	C_L = 50pF,external pull up resistance = 1kohm			50	ns
f_{FILT_FM+} (3)	Analog filter on FM+ pin				50	ns

(1) The port can output frequencies at least up to the specified limit and might support higher frequencies.

(2) The fall time is defined between 70% and 30% of the output waveform accordingly to I2C specification.

(3) There is analog filter up to 50ns as I2C specification. Defualt is disabled and can be enabled on fast mode/fast mode+ if reqired.

(4) Guaranteed by characterization results.

6.33 EXTI Characteristics (1)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
f_{EXTI}	Pulse length to event controller		20			ns

(1) Guaranteed by characterization results.

6.34 I2C Characteristics (1)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$t_{SCL(H)}$	SCL clock high time	Standard mode/SMBus	4		-	μs
$t_{SCL(L)}$	SCL clock low time	Standard mode/SMBus	4.7		-	μs
$t_{SU(SDA)}$	SDA setup time	Standard mode/SMBus	250		-	μs
$t_{h(SDA)}$	SDA data hold time	Standard mode/SMBus	0		-	μs
t_r	SDA/SCL rise time	Standard mode/SMBus	-		1000	μs
t_f	SDA/SCL fall time	Standard mode/SMBus	-		300	μs
$t_{h(STA)}$	Start condition hold time	Standard mode/SMBus	4			μs
$t_{su(STA)}$	Repeated start condition setup time	Standard mode/SMBus	4.7			μs
$t_{su(STO)}$	Stop condition setup time	Standard mode/SMBus	4			μs
$t_{SCL(H)}$	SCL clock high time	Fast mode	0.6			μs
$t_{SCL(L)}$	SCL clock low time	Fast mode	1.3			μs
$t_{SU(SDA)}$	SDA setup time	Fast mode	100		-	μs
$t_{h(SDA)}$	SDA data hold time	Fast mode	0		-	μs
t_r	SDA/SCL rise time	Fast mode	-		300	μs
t_f	SDA/SCL fall time	Fast mode	-		300	μs
$t_{h(STA)}$	Start condition hold time	Fast mode	0.6			μs
$t_{su(STA)}$	Repeated start condition setup time	Fast mode	0.6			μs
$t_{su(STO)}$	Stop condition setup time	Fast mode	0.6			μs
$t_{SCL(H)}$	SCL clock high time	Fast mode plus	0.2		-	μs
$t_{SCL(L)}$	SCL clock low time	Fast mode plus	0.5		-	μs
$t_{SU(SDA)}$	SDA setup time	Fast mode plus	50		-	μs
$t_{h(SDA)}$	SDA data hold time	Fast mode plus	0		-	μs
t_r	SDA/SCL rise time	Fast mode plus	-		120	μs
t_f	SDA/SCL fall time	Fast mode plus	-		120	μs
$t_{h(STA)}$	Start condition hold time	Fast mode plus	0.26			μs
$t_{su(STA)}$	Repeated start condition setup time	Fast mode plus	0.26			μs

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$t_{su(STO)}$	Stop condition setup time	Fast mode plus	0.26			μs

(1) Guaranteed by characterization results.

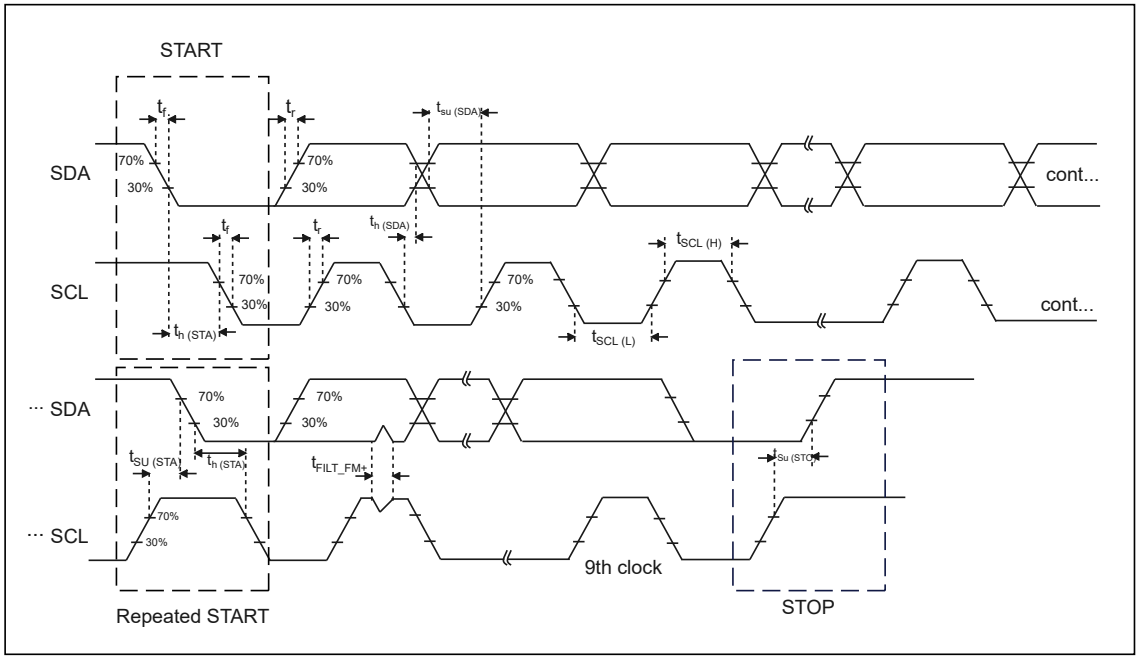


Figure 5. I2C Timing Diagram

6.35 SPI Characteristics (1)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
f_{SCK}	SPI clock frequency	Full duplex Master/Slave mode, V_{CORE} = 1.1V high power mode		20		MHz
		Master transimitter mode, V_{CORE} = 1.1V low power mode		70		MHz
		Master receiver mode, V_{CORE} = 1.1V low power mode		50		MHz
		Slave transimitter , V_{CORE} = 1.1V low power mode		30		MHz
		Slave receiver, V_{CORE} = 1.1V low power mode		65		MHz
$t_{su(NSS)}$	NSS setup time	Slave mode	4* t_{sck}			
$t_{h(NSS)}$	NSS hold time	Slave mode	2* t_{sck}			
$t_{sck(H)}$	SCK clock high time	Master mode	t_{sck}/2 - 1	t_{sck}/2	t_{sck}/2 + 1	ns
$t_{sck(L)}$	SCK clock low time	Master mode	t_{sck}/2 - 1	t_{sck}/2	t_{sck}/2 + 1	ns
$t_{v(MO)}$	Data output valid time	Master mode, C_L = 20 pF		2	8	ns
$t_{su(MI)}$	Data input setup time	Master mode, C_L = 20 pF	6	-	-	ns
$t_{H(MI)}$	Data input hold time	Master mode, C_L = 20 pF	8	-	-	ns
$t_{A(SO)}$	Data output access time	Slave mode, C_L = 20 pF	10	-	32	ns

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$t_{DIS(SO)}$	Data output disable time	Slave mode, C_L = 20 pF	12	-	20	ns
$t_{V(SO)}$	Data output valid time	Slave mode, C_L = 20 pF	11	17	21	ns
$t_{SU(SI)}$	Data input setup time	Slave mode, C_L = 20 pF	5	-	-	ns
$t_{H(SI)}$	Data input hold time	Slave mode, C_L = 20 pF	2	-	-	ns

(1) Guaranteed by characterization results.

(2) tsck = tspi_ker_ck × baudrate prescaler.

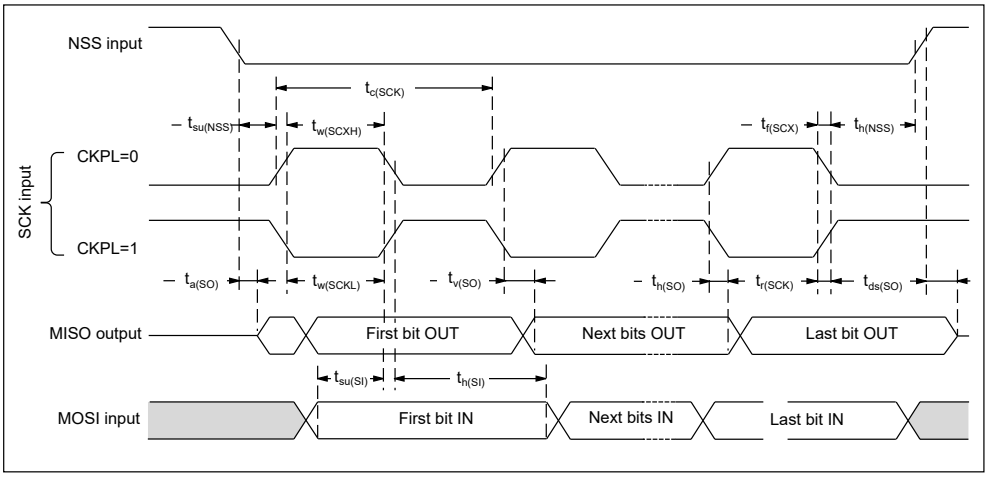


Figure 6. SPI Timing Diagram - Slave Mode

(1) Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

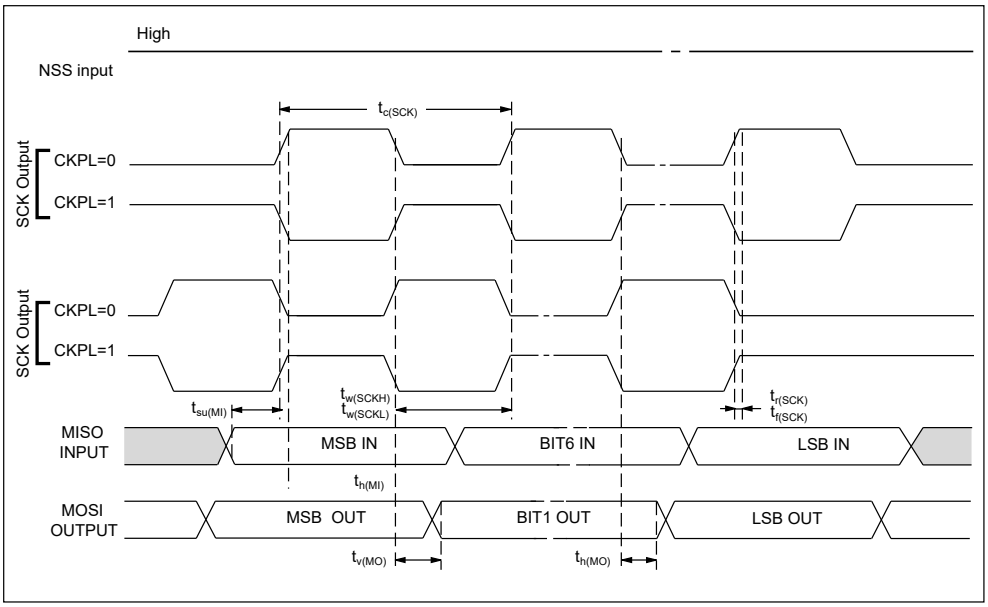


Figure 7. SPI Timing Diagram - Master Mode

(1) Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

6.36 QSPI in SDR Mode (1)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$F_{(QCK)}$	Quad SPI clock frequency	C_{LOAD} = 20 pF, V_{CORE}=1.1V	-	78		MHz
$t_{w(CKH)}$	Quad SPI clock high and low time	PRESCALER [5:0] n =2, 4, 6, 8…	(n/2)*$t_{(CK)}$/(n+1) - 0.5	-	(n/2)*$t_{(CK)}$/(n+1) + 1	ns
$t_{w(CKL)}$		PRESCALER [5:0] n =2, 4, 6, 8…	(n/2+1)*$t_{(CK)}$/ (n+1) - 1	-	(n/2+1)*$t_{(CK)}$/(n+1) +0.5	ns
$t_{s(IN)}$	Data input setup time		1	-	-	ns
$t_{h(IN)}$	Data input hold time		5	-	-	ns
$t_{v(OUT)}$	Data output valid time		-	1	3	ns
$t_{h(OUT)}$	Data output hold time		1	-	-	ns

(1) Guaranteed by characterization results.

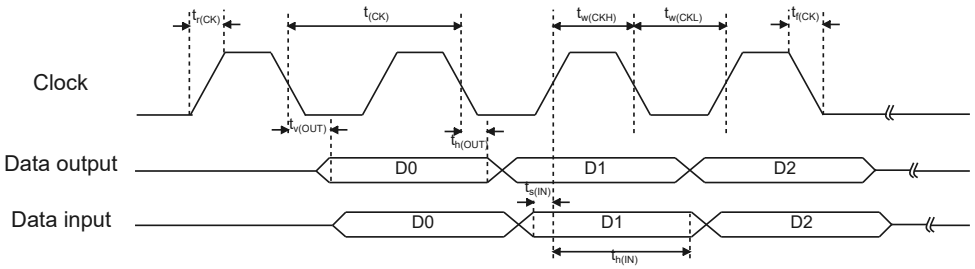


Figure 8. QSPI in SDR Mode Timing Diagram

6.37 QSPI in DDR Mode (1)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$F_{(QCK)}$	Quad SPI clock frequency	C_{L}OAD = 20 pF, V_{CORE}=1.1V	-	78		MHz
$t_{w(CKH)}$	Quad SPI clock high and low time	PRESCALER [5:0] n =2,4, 6, 8…	(n/2)*$t_{(CK)}$/(n+1)	-	(n/2)*$t_{(CK)}$/(n+1) + 1	ns
$t_{w(CKL)}$		PRESCALER [5:0] n =2,4, 6, 8…	(n/2+1)*$t_{(CK)}$/(n+1) - 1	-	(n/2+1)*$t_{(CK)}$/(n+1)	ns
$t_{sr(IN)}$	Data input setup time on rising edge		2	-	-	ns
$t_{sf(IN)}$	Data input setup time on falling edge		2	-	-	ns
$t_{hr(IN)}$	Data input hold time on rising edge		4	-	-	ns

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$t_{hf(IN)}$	Data input hold time on falling edge		3	-	-	ns

(1) Guaranteed by characterization results.

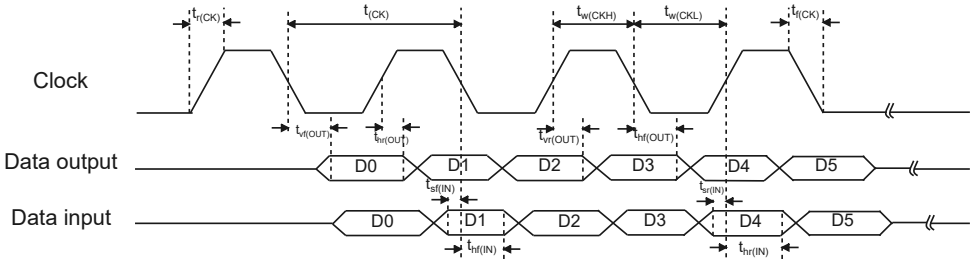


Figure 9. QSPI in DDR Mode Timing Diagram

6.38 Timer Characteristics (1)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$t_{res(TIM)}$	Timer resolution time	-	1		-	$t_{TIMxCLK}$
f_{EXT}	Timer external clock frequency	-	0		$f_{TIMxCLK}/2$	MHz
R_{esTIM}	Timer resolution	Timer with 16-bit counter	-		16	bit
		Timer with 32-bit counter	-		32	bit
t_{MAX_COUNT}	Maximum possible count	Timer with 16-bit counter	-		65536	$t_{TIMxCLK}$
		Timer with 32-bit counter	-		65536 × 65536	$t_{TIMxCLK}$
f_{ENC}	Encoder frequency on input pins	-	0		$f_{TIMxCLK}/4$	MHz
$t_{W(INDEX)}$	Index pulse width on ETR input	-	2		-	Tck
$t_{W(TI1, TI2)}$	Min pulse width on inputs except directional clock x1	-	2		-	Tck
	Min pulse width on inputs in directional clock x1	-	3		-	Tck

(1) Guaranteed by design.

6.39 Flash Characteristics (1)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
T_{prog_page}	One page (2 Kbytes) programming time	V_{DD} = 3V		15		ms

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
t_{ME}	Mass erase time	V_{DD} = 3V		9		ms
t_{RET}	Data retention duration	V_{DD} = 3V, 25°C		10		years
N_{endu}	Endurance	T_A = - 40 to +105 °C	10			kcycles
I_{DD}	Average supply current from V_{DD} during program			2	4	mA
	Average supply current from V_{DD} during erase			4	6	mA
	Average supply current from V_{DD} during mass erase or bank erase			4	6	mA

(1) Guaranteed by design.

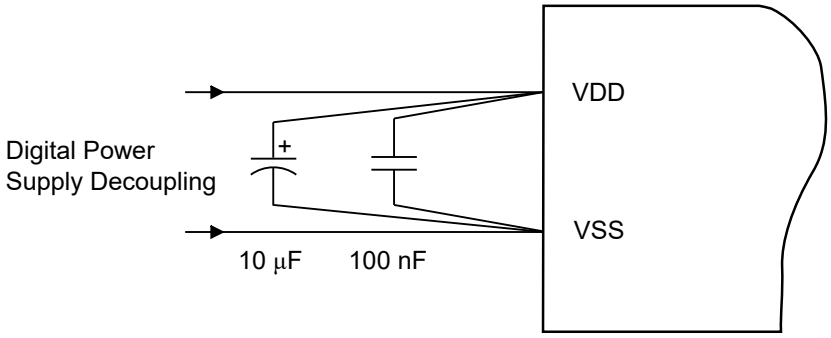
7 Applications Implementation and Layout

> Note
>
> Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Power Supply Decoupling and Bulk Capacitors

It is recommended to connect a combined 10 µF and 100 nF low-ESR ceramic decoupling capacitor to the VDD pin. Higher-value capacitors can be used but can impact supply rail ramp-up time.

Ensure the decoupling capacitors are positioned as near as possible to the pins they decouple, ideally within a few millimeters.



7.2 External Oscillator

The TSP325M5A devices are compatible with an External Low-Speed (ELS) 32 kHz crystal, connected via OSCL_IN and OSCL_OUT pins, and an External High-Speed (EHS) crystal (ranging from 4 to 32 MHz), interfaced through OSCH_IN and OSCH_OUT pins. External bypass capacitors for the crystal oscillator pins are required.

Moreover, it's feasible to input digital clock signals that align with the oscillator's specifications into the OSCL_IN and OSCH_IN pins, provided the corresponding ELS or EHS bypass mode is enabled. Under these circumstances, the related OSCL_OUT and OSCH_OUT pins can serve alternative functions. If not utilized, these pins should be terminated in line with the recommendations for unused pins.

7.3 Reset (NRST)

The NRST pin can be configured as a reset function (default) or as output function.

In reset mode, the NRST pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

7.4 Unused Pins

All unused pins are recommended to connect to ground to minimize decoupling noise.

7.5 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See TPS32xx family 32KHz crystal oscillator for recommended layout guidelines.
- Proper bypass capacitors on V_{DD}, V_{DDA}, and reference pins if used.

- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital witching signals such as PWM or JTAG signals away from the oscillator circuit and ADC signals.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge.

7.6 Do's and Don'ts

During power-up, power-down, and device operation, it is important to ensure that the voltage difference between V_{DD} and V_{DDA} does not exceed the limits specified in Absolute Maximum Ratings. Exceeding these limits can result in unexpected device malfunction.

7.7 Peripheral- and Interface-Specific Design Information

7.7.1 Analog-to-Digital Converter (ADC)

As with any high-resolution ADC, appropriate printed-circuit-board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. This current can generate small unwanted offset voltages that can add to or subtract from the reference or inputvoltages of the ADC. The offset/gain calibration is recommended to reduce this gain/offset error.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. 3PEAK recommends a noise-free design using separate analog and digitalground planes with a single-point connection to achieve high accuracy.

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected inthe general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10-μF capacitor buffers the reference pin and filters low-frequency ripple, and the 100-nF bypass capacitor filtershigh-frequency noise.

8 Device and Documentation Support

8.1 Getting Started

For more information on TPS32 mixed-signal industrial microcontrollers, evaluation boards, embedded software, and development tools that are available to help with your development, visit the 3PEAK website.

8.2 Device Nomenclature

Figure 10 provides the description of TPS325M5A Series device nomenclature.

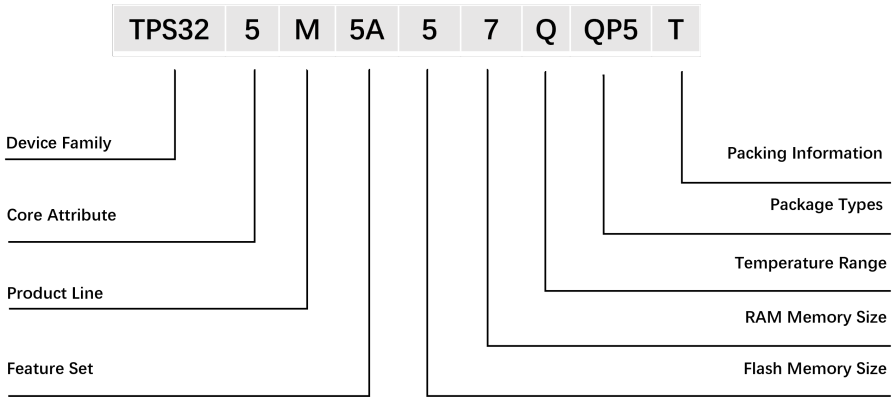


Figure 10. TPS325M5A Device Nomenclature

Part Number Field Description	Values	Interpretation
Device Family	TPS32	3PEAK 32-bit Microcontrollers
Core Attribute	5	32-bit STAR-MC1 core based on Arm® v8-M architecture, compatible with CortexR-M33 instruction set
Product Line	B	Base Line
	M	Mainstream Line
Feature Set	5A	Optimized for HMI Application TPSensor® Rich Analog Integration (high resolution ADC, DAC, OA)
Flash Memory Size	5	512 KB
	6	1024 KB
	7	2048 KB
RAM Memory Size	5	144 KB
	6	208 KB
	7	336 KB
Temperature Range	I	Industrial -40~85℃
	Q	Extend Industrial -40~105℃
Package Types	FSD	QFN88 (0.4mm pitch)
	QP5	LQFP64 (0.5mm pitch)
	QP6	LQFP80 (0.5mm pitch)
	QP7	LQFP100 (0.5mm pitch)
Packing Information	R	Tape & Reel
	T	Tray

Part Number Field Description	Values	Interpretation
	U	Tube

8.3 Tools and Software

Hardware Evaluation Boards	
TPS325M51-A Prime Board	TPS325M51-A Prime Board is perfectly appropriate for fast prototyping with TPS325M5 and TPS325M0 Series feature sets. The prime board is easy to use with user guide, design files, development tools, and comprehensive software code examples. Prime Boards can be flexibly used as standalone, with expansion boards for more functionalities, or even with various ARDUINO® shields.
Serial Communication V1 Expansion Board	Serial Communication V1 Expansion Board provides the opportunity to explore additional serial communication functionality. The expansion board can work with prime boards with standard expansion connectors. Comprehensive documentation, software libraries, and code examples are provided to harness the board's full potential.
Embedded Software	
Peripheral Driver Library	TPS32 Peripheral Driver Library offers abstracted APIs for developers simply manipulating the function calls of TPS32 microcontroller hardware. It is accessible on 3PEAK and GitHub websites. The comprehensible API documentation is available online.
Development Tools	
ARM Keil Microcontroller Development Kit	Keil MDK is the complete software development environment for a range of Arm Cortex-M based microcontroller devices.MDK includes the µVision IDE and debugger, Arm C/C++ compiler, and essential middleware components.
IAR Embedded Workbench® IDE	IAR Embedded Workbench IDE for ARM is an integrated development environment generating fast, compact code and provides comprehensive debugging functions with various debug probes support. Effectively add-on static and runtime code analysis tools are also included.
TPS32 Programmer Tool	TPS32 Programmer is a user-friendly GUI tool for TPS32 on-chip non-volatile memories programming (read, write, erase, verify, and option bytes configuration). It supports both the debug port interface (DAP-Link) and the bootloader interface (UART). This tool can be downloaded from the 3PEAK website.
TPSensor® Designer	TPSensor® Designer is a GUI environment that provides developers with a simple and intuitive way to develop applications with outstanding TPSensor ® Capacitive Sensing Technology. It can be leveraged to configure hardware channels, sensing modes(self-capacitance and mutual-capacitance), and elements(e.g. buttons, wheels, sliders…etc), generate adapted code automatically, and tune the data with real-time graphic view. This tool can be downloaded from 3PEAK website.
SEGGER J-Link	J-Link debug probes are the most popular choice for optimizing the debugging and flash programming experience. Benefit from record-breaking flash loaders, up to 4 MB/s RAM download speed and the ability to set an unlimited number of breakpoints in the flash memory of MCUs.
Gang Programmer	Through close collaboration with several leading suppliers, a diverse range of programming solutions for 3PEAK TPS32 devices can be provided. For more details on these programming solutions, please visit the 3PEAK website.

8.4 Documentation Support

The following documents describe the TSP325M5A series microcontrollers.

Errata

TPS325M Errata Sheet

TRM

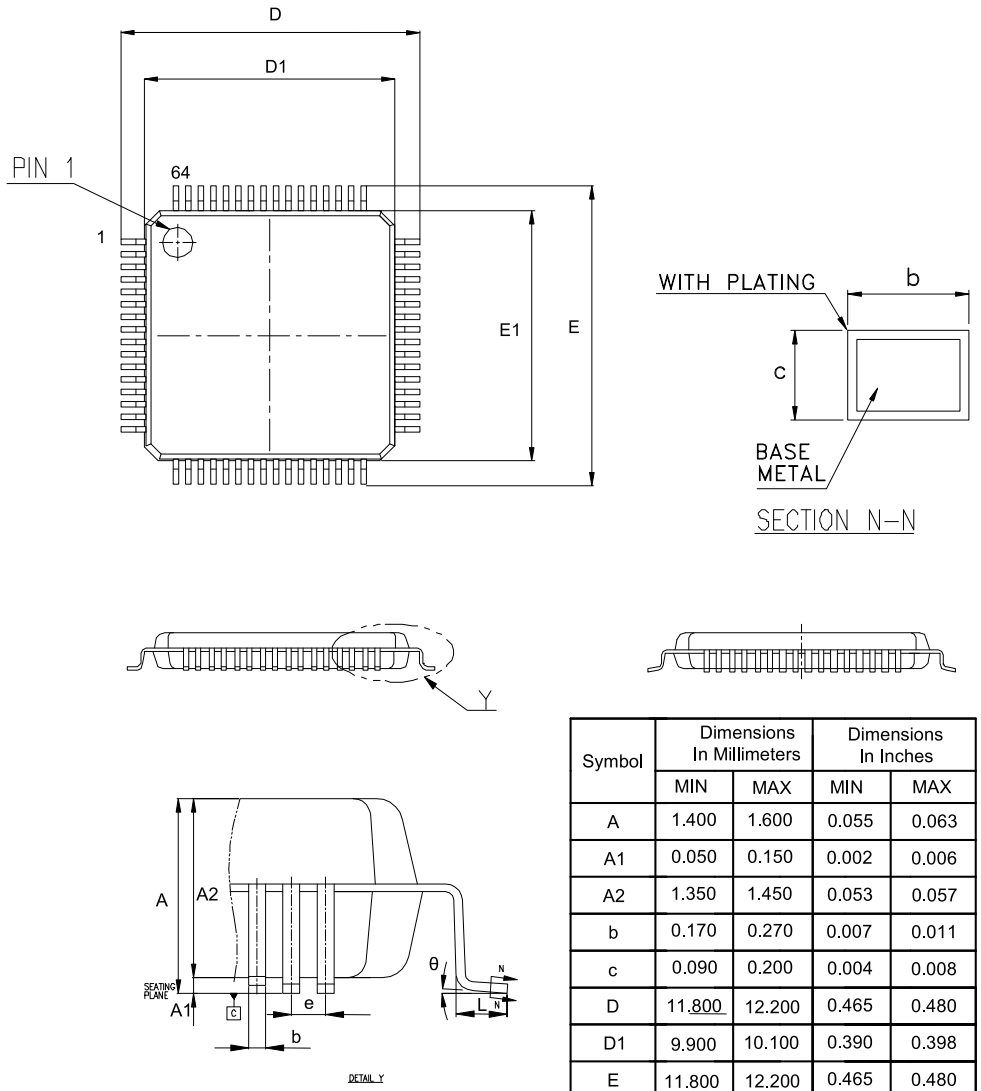
TPS325M Technical Reference Manual

Detailed description of all modules and peripherals available in this device family.

9 Package Information

9.1 LQFP10x10-64 Outline Dimensions

Package Outline Dimensions QP5(LQFP10X10-64-A)



NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.400	1.600	0.055	0.063
A1	0.050	0.150	0.002	0.006
A2	1.350	1.450	0.053	0.057
b	0.170	0.270	0.007	0.011
c	0.090	0.200	0.004	0.008
D	11.800	12.200	0.465	0.480
D1	9.900	10.100	0.390	0.398
E	11.800	12.200	0.465	0.480
E1	9.900	10.100	0.390	0.398
e	0.500 BSC		0.020 BSC	
L	0.450	0.750	0.018	0.030
θ	0	7°	0	7°

10 Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPS325M5A57Q-QP5T	−40 to 105°C	LQFP10X10-64-A	TPS325M5A57QP5	MSL3	Tray,1600	Green

(1) **Green**: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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